

**MOS**  
MEMORY

April 1987





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**TOSHIBA**

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**MOS MEMORY PRODUCTS**

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**DATA BOOK**

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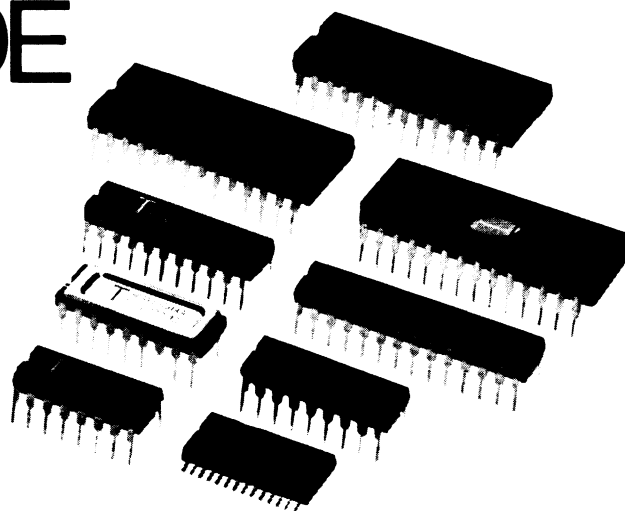
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# MEMORY PRODUCT GUIDE





## 1. Dynamic RAM

Capacity	Type No.	Organi- zation	Access Time, Max(ns)		Cycle Time Min.(ns)	Process	Power Dissipation, Max.(mW)		Pins	Operating Mode
			t <sub>RAC</sub>	t <sub>CAC</sub>			Active	Standby		
256K Bit	TMM41256P/T-12	262,144×1	120	60	220	NMOS	330	28	16/18	Page
	TMM41256P/T-15		150	75	260		275			
	*TMM41256AP/AT/AZ-10	262,144×1	100	50	190	NMOS	440	28	16/18/16	Page
	*TMM41256AP/AT/AZ-12		120	60	220		396			
	*TMM41256AP/AT/AZ-15		150	75	260		358			
	TMM41257P/T-12	262,144×1	120	60	220	NMOS	385	28	16/18	Nibble
	TMM41257P/T-15		150	75	260		330			
	*TMM41257AP/AT/AZ-10	262,144×1	100	50	190	NMOS	440	28	16/18/16	Nibble
	*TMM41257AP/AT/AZ-12		120	60	220		396			
	*TMM41257AP/AT/AZ-15		150	75	260		358			
TMM41464P-12	65,536×4	120	60	220	NMOS	385	28	18	Page	
TMM41464P-15		150	75	260		330				
1M Bit	TC511000P/J/Z-85	1,048,576×1	85	25	165	CMOS	385	5.5	18/26/20	Fast Page
	TC511000P/J/Z-10		100	25	190		330			
	TC511000P/J/Z-12		120	30	220		275			
	TC511001P/J/Z-85	1,048,576×1	85	30	165	CMOS	385	5.5	18/26/20	Nibble
	TC511001P/J/Z-10		100	35	190		330			
	TC511001P/J/Z-12		120	40	220		275			
	TC511002P/J/Z-85	1,048,576×1	85	25	165	CMOS	385	5.5	18/26/20	Static Column
	TC511002P/J/Z-10		100	25	190		330			
	TC511002P/J/Z-12		120	30	220		275			
	TC514256P/J/Z-85	262,144×4	85	30	165	CMOS	413	5.5	20/26/20	Fast Page
	TC514256P/J/Z-10		100	30	190		358			
	TC514256P/J/Z-12		120	35	220		303			
	TC514258P/J/Z-85	262,144×4	85	30	165	CMOS	413	5.5	20/26/20	Static Column
	TC514258P/J/Z-10		100	30	190		358			
TC514258P/J/Z-12	120		35	220	303					

NOTE: PACKAGE TYPE P: PLASTIC DIP T: PLCC J: SOJ Z: ZIP

\*NEW PRODUCT

## 2. Dynamic RAM HYBRID MODULE

Capacity	Type No.	Organi- zation	Access Time, Max(ns)		Cycle Time Min.(ns)	Dram Units	Power Dissipation, Max.(mW)		Pins	Module
			t <sub>RAC</sub>	t <sub>CAC</sub>			Active	Standby		
8M Bit	*THM81000S-10	1,048,576×8	100	25	190	TC511000J	2,640	44	30	SIMM
	*THM81000S-12		120	30	220		2,200			
	*THM81000L-10	1,048,576×8	100	25	190	TC511000J	2,640	44	30	SIP
	*THM81000L-12		120	30	220		2,200			
9M Bit	*THM91000S-10	1,048,576×9	100	25	190	TC511000J	2,970	49.5	30	SIMM
	*THM91000S-12		120	30	220		2,475			
	*THM91000L-10	1,048,576×9	100	25	190	TC511000J	2,970	49.5	30	SIP
	*THM91000L-12		120	30	220		2,475			

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## 3. STANDARD APPLICATION Static RAM

Capacity	Type No.	Organization	Access Time Max(ns)	Cycle Time Min(ns)	Process	Power Dissipation Max.(mW)		Pins	Package Width (inch)
						Active	Standby		
16K Bit	TMM2015BP-90	2,048×8	90	90	NMOS	275	27.5	24	0.3
	TMM2015BP-10		100	100					
	TMM2015BP-12		120	120					
	TMM2015BP-15		150	150					
	TMM2016BP-90	2,048×8	90	90	NMOS	275	27.5	24	0.6
	TMM2016BP-10		100	100					
	TMM2016BP-12		120	120					
	TMM2016BP-15		150	150					
	TC5517CP/CF-15	2,048×8	150	150	CMOS	27.5	0.165	24	0.6(P) 0.45(F)
	TC5517CPL/CFL-15		200	200			0.005		
	TC5517CPL/CFL-20		150	150					
	TC5518CP/CF-15	2,048×8	150	150	CMOS	27.5	0.165	24	
	TC5518CP/CF-20		200	200			0.005		
	TC5518CPL/CFL-15		150	150					
TC5518CPL/CFL-20	200		200						
64K Bit	TMM2063P-10	8,192×8	100	100	NMOS	440	55	28	0.3
	TMM2063P-12		120	120					
	TMM2063P-15		150	150					
	TMM2064P-10	8,192×8	100	100	NMOS	440	55	28	0.6
	TMM2064P-12		120	120					
	TMM2064P-15		150	150					
	TC5563APL-10	8,192×8	100	100	CMOS	27.5	0.55	28	0.3
	TC5563APL-12		120	120			0.165		
	TC5563APL-15		150	150					
	TC5563APL-10L		100	100					
	TC5563APL-12L		120	120					
	TC5563APL-15L	150	150						
	TC5565APL/AFL-10	8,192×8	100	100	CMOS	27.5	0.55	28	0.6(P) 0.45(F)
	TC5565APL/AFL-12		120	120			0.165		
	TC5565APL/AFL-15		150	150					
	TC5565APL/AFL-10L		100	100					
	TC5565APL/AFL-12L		120	120					
	TC5565APL/AFL-15L	150	150						
	*TC5564APL/AFL-12	8,192×8	120	120	CMOS	27.5	0.005	28	0.6(P) 0.45(F)
	*TC5565APL/AFP-15		150	150					
256K Bit	TC55257P-10	32,768×8	100	100	CMOS	27.5	5.5	28	0.6
	TC55257P-12		120	120			0.55		
	TC55257PL-85		85	85					
	TC55257PL-10		100	100					
	TC55257PL-12		120	120					
	*TC55257AP/AF-10	32,768×8	100	100	CMOS	27.5	5.5	28	0.6(P) 0.45(F)
	*TC55257AP/AF-12		120	120			0.55		
	*TC55257APL/AFL-10		100	100					
	*TC55257APL/AFL-12		120	120					

### PSEUDO-STATIC RAM

256K Bit	TC51832P-85	32,768×8	85	135	CMOS	303	5.5	28	.6
	TC51832P-10		100	160		248			
	TC51832P-12		120	190		220			

NOTE: PACKAGE TYPE P: PLASTIC DIP F: FLAT PACKAGE (SOP)

\*NEW PRODUCT



## 4. HIGH SPEED Static RAM

Capacity	Type No.	Organization	Access Time Max (ns)	Cycle Time Min (ns)	Process	Power Dissipation Max.(mW)		P <sub>ins</sub>	Package Width (inch)	
						Active	Standby			
16K Bit	*TMM2018AD/AP-25	2,048 × 8	25	25	NMOS	660	110	24	0.3	
	*TMM2018AD/AP-35		35	35		550				
	*TMM2018AD/AP-45		45	45		440				
	*TMM2068AD/AP-25	4,096 × 4	4,096 × 4	25	25	NMOS	660	110	20	0.3
	*TMM2068AD/AP-35			35	35		550			
	*TMM2068AD/AP-45			45	45		440			
	*TMM2078AD-25	4,096 × 4	4,096 × 4	25	25	NMOS	660	110	22	0.3
	*TMM2078AD-35			35	35		550			
	*TMM2078AD-45			45	45		440			
64K Bit	*TMM2088P-35	8,192 × 8	35	35	NMOS	660	55	28	0.3	
	*TMM2088P-45		45	45						
	*TMM2088P-55		55	55						
72K Bit	*TMM2089C-35	8,192 × 9	35	35	NMOS	660	55	28	0.3	
	*TMM2089C-45		45	45						
	*TMM2089C-55		55	55						
64K Bit	TC5561P-55	65,536 × 1	55	55	CMOS	550	0.55	22	0.3	
	TC5561P-70		70	70						
	TC5562P-45	65,536 × 1	45	45	CMOS	550	11	22	0.3	
	TC5562P-55		55	55						
	*TC55416P-35	16,384 × 4	35	35	CMOS	440	55	22	0.3	
	*TC55416P-45		45	45		330				
	*TC55417P-35	16,384 × 4	35	35	CMOS	440	55	24	0.3	
	*TC55417P-45		45	45		330				

NOTE PACKAGE MATERIAL D CERDIP C CERAMIC DIP P PLASTIC DIP

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## 5. EPROM

Capacity	Type No.	Organi- zation & Process	Access Time Max.(ns)	Cycle Time Min.(ns)	Power Supply (V)	Temperature Range (°C)	Power Dissipation Max.(mW)		Pins	Programming Algorithm
							Active	Standby		
64K Bit	TMM2764AD-15	8,192×8 NMOS	150	150	5V±5%	0~70	525	158	28	I or II
	TMM2764AD-20		200	200		-40~85	630	184		
	TMM2764ADI-15		150	150						
	TMM2764ADI-20		200	200	5V±10%	0~70	660	193		
	TMM2764AD-150		150	150						
	TMM2764AD-200		200	200						
128K Bit	TMM27128AD-15	16,384×8 NMOS	150	150	5V±5%	0~70	525	158	28	I or II
	TMM27128AD-20		200	200		-40~85	630	184		
	TMM27128ADI-15		150	150						
	TMM27128ADI-20		200	200	5V±10%	0~70	660	193		
	TMM27128AD-150		150	150						
	TMM27128AD-200		200	200						
256K Bit	TMM27256AD-15	32,768×8 NMOS	150	150	5V±5%	0~70	525	158	28	I or II
	TMM27256AD-20		200	200		-40~85	630	184		
	TMM27256ADI-15		150	150						
	TMM27256ADI-20		200	200	5V±10%	0~70	660	193		
	TMM27256AD-150		150	150						
	TMM27256AD-200		200	200						
	TC57256D-20	32,768×8 CMOS	200	200	5V±5%	21.0	158	0.525	28	I or II
	TC57256D-25		250	250						
	*TC57256AD-15		150	150	5V±5%	12.5				
	*TC57256AD-20		200	200						
512K Bit	TMM27512D-20	65,536×8 NMOS	200	200	5V±5%	0~70	630	184	28	I or II
	TMM27512D-25		250	250		-40~85	683	210		
	TMM27512DI-20		200	200						
	TMM27512DI-25		250	250	5V±10%	0~70	715	220		
	TMM27512D-200		200	200						
	TMM27512D-250		250	250						
1M Bit	*TC571000D-15	131,072×8 CMOS	150	150	5V±5%	-40~85	158	0.525	32	II
	*TC571000D-20		200	200						
	*TC571001D-15		150	150						
	*TC571001D-20		200	200						

NOTE: PACKAGE MATERIAL D: CERDIP

\*NEW PRODUCT

## 6. ONE TIME PROM

Capacity	Type No.	Organi- zation & Process	Access Time Max.(ns)	Cycle Time Min.(ns)	Power Supply (V)	Temperature Range (°C)	Power Dissipation Max.(mW)		Pins	Programming Algorithm
							Active	Standby		
64K Bit	TMM2464AP/AF	8,192×8 NMOS	200	200	5V+5%	-40~85°C	525	158	28	I or II
128K Bit	TMM24128AP/AF	16,384×8 NMOS	200	200	5V+5%	-40~85°C	525	158	28	I or II
256K Bit	TMM24256AP/AF	32,768×8 NMOS	200	200	5V+5%	-40~85°C	525	158	28	I or II
	*TC54256AP/AF	32,768×8 CMOS	200	200	5V±5%		158	0.525	28	I or II
512K Bit	TMM24512P/F	65,536×8 NMOS	250	250	5V±5%	-40~85°C	630	184	28	I or II

NOTE: PACKAGE TYPE P: PLASTIC DIP F: FLAT PACKAGE (SOP)

\*NEW PRODUCT

## 7. Mask ROM

Capacity	Type No.	Organi- zation	Access Time Max.(ns)	Cycle Time Min.(ns)	Process	Power Dissipation Max.(mW)		Pins
						Active	Standby	
256K Bit	TC53257P/F	32,768×8	200	200	CMOS	138	0.11	28
1M Bit	TC531000AP/AF	131,072×8	200	200	CMOS	138	0.11	28
2M Bit	TC532000P	262,144×8	200	200	CMOS	220	0.11	32
4M Bit	*TC534000P	524,288×8	250	250	CMOS	220	0.11	32

NOTE: PACKAGE TYPE P: PLASTIC DIP F: FLAT PACKAGE

\*NEW PRODUCT

# TOSHIBA

## 1. 256K Bit Dynamic RAM

Organization	256K×1 (page mode)	256K×1 (nibble mode)	64K×4 (page mode)
TOSHIBA	TMM41256AP/AT/AZ	TMM41257AP/AT/AZ	TMM41464AP/AT/AZ
Fujitsu	MB81256	MB81257	MB81464
Hitachi	HM50256	HM50257	HM50464
Mitsubishi	M5M4256	M5M4257	M5M4464
NEC	μPD41256	μPD41257	μPD41464
Oki	MSM41256	MSM41257	MSM41464
TI	TMS4256	TMS4257	TMS4464

## 2. 1M×1 Dynamic RAM

Organization	1MB×1 (Fast page mode)		1MB×1 (Nibble mode)		1MB×1 (Static column mode)				
	SUPPLIER	PART#	PROCESS	PART#	PROCESS	PART#	PROCESS		
TOSHIBA	TC511000		CMOS	TC511001		CMOS	TC511002		CMOS
FUJITSU	MB81C1000		CMOS	MB81C1001		CMOS	MB81C1002		CMOS
HITACHI	HM511000		CMOS	HM511001		CMOS	HM511002		CMOS
MITSUBISHI	M5M4C1000		CMOS	M5M4C1001		CMOS	M5M4C1002		CMOS
NEC	μPD421000		CMOS	μPD421001		CMOS	μPD421002		CMOS
TI	TMS4C1024		CMOS	TMS4C1025		CMOS	TMS4C1027		CMOS
AT&T	M411024PP		CMOS	—			M411024PK		CMOS
NMB	AAA1M101		CMOS	AAA1M102		CMOS	AAA1M100		CMOS
SAMSUNG	KM41C1000		CMOS	KM41C1001		CMOS	KM41C1002		CMOS

## 3. 256K×4 Dynamic RAM

Organization	256K×4 (Fast page mode)		256K×4 (Static column mode)			
	SUPPLIER	PART#	PROCESS	PART#	PROCESS	
TOSHIBA	TC514256		CMOS	TC514258		CMOS
FUJITSU	MB81C4256		CMOS	—		
HITACHI	HM514256		CMOS	HM514258		CMOS
MITSUBISHI	M5M44C256		CMOS	M5M44C258		CMOS
NEC	μPD424256		CMOS	μPD424258		CMOS
TI	TMS44C256		CMOS	TMS44C257		CMOS
SHARP	LH64257		CMOS	LH64256		CMOS

## 4. DRAM HYBRID MODULE

ORGANIZATION	1M×8	1M×9
TOSHIBA	THM81000S/L	THM91000S/L
HITACHI	HB56A18	HB56A19
MITSUBISHI		MH1M09J

## 5. 16K Bit Static RAM 1) NMOS

Organization	2K×8			4K×4
	0.6 inch	0.3 inch		
TOSHIBA	TMM2016BP	TMM2015BP	TMM2018AD/AP	TMM2068AD/AP
Fujitsu	MB8128			MB8168
Hitachi	HM6116	HM6116AS		HM6168
Inmos				IMS1420/1421
Mitsubishi	M58725			M5M2168
Motorola	MCM6116		MCM2016H/18	MCM6168
NEC	μPD4016	μPD4016CX		
Oki	MSM2128			
AMD		AM9128	AM9128	AM2168

## 2) CMOS

Organization	2K×8	
TOSHIBA	TC5517CP/CF	TC5518CP/CF
Fujitsu	MB8416	MB8417/8418
Hitachi	HM6116	HM6117
NEC	μPD446	μPD449
Oki	MSM5128	MSM5129
Mitsubishi	M5M5117	M5M5116/5118
Sharp	LH5117	LH5118

## 6. 64K/72K Bit Static RAM

Organization	8K×8				8K×9	64K×1		
	NMOS		CMOS		NMOS	CMOS		
Package Width	0.3 inch	0.6 inch		0.3 inch		0.3 inch		
TOSHIBA	TMM2063P	TMM2064P	TC5564AP/AF	TC5565APL/AFL	TC5563AP	TMM2088P	TMM2089C	TC5562P
Fujitsu		MB8464		MB8464		MB81C78	MB81C79	HB81C71A
Hitachi	HM6264AS	HM6264		HM6264	HM6264 ASP			HM6287
Mitsubishi			M5M5164	M5M5165		M5M5178	M5M5179	M5M5187
NEC			μPD4464	μPD4364				μPD4361
Oki		MSM5165	MSM5164	MSM5165				
Inmos								IMS1600/1
Motorola						MCM6164		MCM6287
IDT				IDT7164				IDT7187

## 7. 256K Bit Static RAM/Pseudo Static RAM

Organization	32K×8	
	SRAM	PSRAM
TYPE	SRAM	PSRAM
NMOS/CMOS	CMOS	CMOS
Package Width	0.6 inch	0.6 inch
TOSHIBA	TC55257	TC51832P/PL
Fujitsu	HB84256	
Hitachi	HM62256	HM65256
Mitsubishi	M5M5256	
NEC	μPD43256	μPD42832
Sony	CXK58256	
SMOS	SRM20256	
Sharp	LH52256	LH62258

# TOSHIBA

## 8. 64K/128K Bit NMOS EPROM/OTP

Organization	8K×8		16K×8			
	EPROM/OTP	EPROM	OTP	EPROM	OTP	
Pins	28		28		28	
TOSHIBA	TMM2764AD	TMM2464AP/AF		TMM27128AD	TMM24128AP/AF	
AMD	Am2764A			Am27128A		
Fujitsu	MBM2764			MBM27128A		
Hitachi	HN482764	HN482764		HM4827128G	HN4827128	
Intel	i2764A	P2764A		i27128A	P27128A	
Mitsubishi	M5L2764K	M5M2764P		M5L27128K	M5M27128P	
Mostek						
Motorola	—					
NEC	μPD2764	μPD2764C		μPD27128	μPD27128C	
Oki	MSM2764			MSM27218		
TI	TMS2764					

## 9. 256K/512K/1MBIT EPROM/OTP

Organization	32K×8				64K×8		128K×8	
	EPROM		OTP		EPROM	OTP	EPROM	
	NMOS	CMOS	NMOS	CMOS	NMOS		CMOS	
TOSHIBA	TMM27256AD	TC57256D TC57256AD	TMM24256AP/AF	TC54256AP/AF	TMM27512D	TMM24512P/F	TC571000D	TC571001D
AMD	Am27256	AM27C256			Am27512			
Fujitsu	MBM27256	MBM27C256			—	—	MBM27C1000	MBM27C1001
Hitachi	HN27256G	HN27C256G	HN4827256P		HN27512G		HN27C101	HN27C301
Intel	i27256	i27C256	P27256A	P27C256	i27512	P27512	27010	—
Mitsubishi	M5L27256K	M5M27C256	M5M27256P	M5M27C256P	M5L27512		M5M27C100	M5M27C101
NEC	μPD27256	μPD27C256A	μPD27256C	μPD27256C		—	μPD27C100	μPD27C101
Oki	MSM27256	MSM27C256			MSM27512		MSM271000	
NSC	—	NMC27C256	—		NMC27C512		NMC27C1023	
TI	—	TMS27C256			TMS27C512			

## 10. 256K/1MBIT/2MBIT/4MBIT MROM

Organization	32K×8	128K×8	256K×8	512K×8
	CMOS	CMOS		
TOSHIBA	TC53257P/F	TC531000AP/AF	TC532000P	TC534000P
TI	TMS47C256	TMS47C1024		
Fujitsu	MB83256	MB831124	MB832000	
Hitachi	HN613256P	HN62301	HN62302	
Motorola	MCM65256A			
Mitsubishi	—	M5M23C100	—	M5M23C400
NEC	μPD23C256	μPD23C1000	μPD23C2000	
Oki	MSM53256	MSM531000		
RCA	CDM53256			

## MEMORY SELECTION GUIDE (1) — ACCESS TIME VS. CAPACITY.

\*Preliminary

				TC57256-25	TMM27512-25 TMM27512-250 TMM24512	TC571000/1-25		TC534000	
200	TC5517C-20 TC5518C-20	TMM2764A-20 TMM2764A-200 TMM2464A	TMM27128A-20 TMM27128A-200 TMM24128A	TC57256A-20 TMM27256A-20 TMM27256A-200 TC57256-20 TMM24256A TC54256A TC53257	TMM27512-20 TMM27512-200	TC571000/1-20	TC532000		
150	TMM2015B-12/15 TMM2016B-12/15 TC5517C-15 TC5518C-15	TMM2063-12/15 TMM2064-12/15 TC5563A-12/15 TC5564A-12/15 TC5565A-12/15 TMM2764A-15 TMM2764A-150	TMM27128A-15 TMM27128A-150	TMM41256-12/15 TMM41257-12/15 TMM41464-12/15 TMM41256A-12/15 TMM41257A-12/15 TC55257-12 TC55257A-12 TC51832-12 TMM27256A-15 TMM27256A-150		TC511000-12 TC511001-12 TC511002-12 TC514256-12 TC514258-12 TC531000A			
100	TMM2015B-90/10 TMM2016B-90/10	TMM2063-10 TMM2064-10 TMM2064-70 TC5563A-10 TC5565A-10 TC5561-55/70		TMM41256A-10 TMM41257A-10 TC55257-85/10 TC55257A-85/10 TC51832-85/10		TC511000-85/10 TC511001-85/10 TC511002-85/10 TC514256-85/10 TC514258-85/10			
55	TMM2018A-25/35/45 TMM2068A-25/35/45 TMM2078A-25/35/45	TMM2088-35/45/55 TC5562-45/55 TC55416-35/45/55 TC55417-35/45/55	TMM2089-35/45/55						
	16K Bit	64K Bit	72K Bit	128K Bit	256K Bit	512K Bit	1M Bit	2M Bit	4M Bit

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## MEMORY SELECTION GUIDE (2) — TYPE OF MEMORY VS. CAPACITY

\*Preliminary

Memory	Type	Memory Capacity								
		16K Bit	64K Bit	72K Bit	128K Bit	256K Bit	512K Bit	1M Bit	2M Bit	4M Bit
RAM	NMOS Dynamic RAM					TMM41256P/T TMM41257P/T TMM41464P TMM41256AP/A/AZ TMM41257AP/A/AZ				
	CMOS Dynamic RAM							TC511000P/UZ TC511001P/UZ TC511002P/UZ TC514256P/UZ TC514258P/UZ		
	NMOS Static RAM	TMM2015BP TMM2016BP TMM2018AD/AP TMM2068AD/AP TMM2076AD	TMM2063P TMM2064P TMM2088P	TMM2089CP						
	CMOS Static RAM	TC5517CP/CF TC5518CP/CF	TC5564APL/FL TC5563APL TC5565APL/AF/FL TC5561P TC5562P TC55416P TC55417P			TC55257P TC55257AP/AF TC51832P/P/L				
ROM	NMOS EPROM		TMM2764AQ/ADI		TMM27128AD/ADI	TMM27256AD/ADI	TMM27512D/DI			
	CMOS EPROM					TC57256D/AD	TC571000/ID			
	CMOS Mask ROM					TC53257P/F	TC531000AP/AF	TC532000P	TC534000P	
	NMOS OTP		TMM2464P/AF		TMM24128AP/AF	TMM24256AP/AF	TMM24512P/F			
	CMOS OTP					TC54256AP/AF				



## MEMORY SELECTION GUIDE (3) — WORD BY BIT

Word \ Bit	1	4	8	9
2K			TMM2015BP TMM2016BP TMM2018AD TMM2018AP	TC5517CP/CF TC5518CP/CF
4K		TMM2068AD/AP TMM2078AD		
8K			TMM2063P TMM2064P TC5564APL/AFL TC5563APL TC5565APL/AFL TMM2088P	TMM2464AP/AF TMM2764AD/ADI TMM2089C/P
16K		TC55416P TC55417P	TMM24128AP/AF TMM27128AD/ADI	
32K			TC55257P TC55257AP/AF TC51832P/PL TC54256AP/AF TMM24256AP/AF	TMM27256AD/ADI TC53257P/F T57256D/AD
64K	TC5561P TC5562P	TMM41464P	TMM24512P/F TMM27512D/DI	
128K			TC531000AP/AF TC571000ID	
256K	TMM41256P/T TMM41257P/T TMM41256AP/AT/AZ TMM41257AP/AT/AZ	TC514256P/J/Z TC514258P/J/Z	TC532000P	
512K			TC534000P	
1M	TC511000P/J/Z TC511001P/J/Z TC511002P/J/Z		THM81000S/L	THM91000S/L

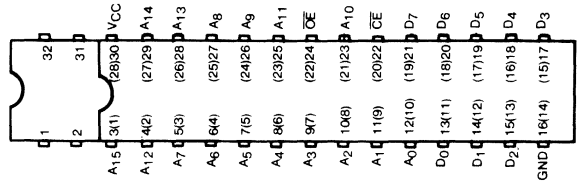
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## MEMORY SELECTION GUIDE (4) — HIGH DENSITY PACKAGE

PACKAGE		PLCC	SQJ	ZIP		SIP/SIMM	SOG	
PIN		18	26/20	16	20/19	30	24	28
Dynamic RAM	256K	TMM41256T TMM41257T TMM41256A1 TMM41257A1		TMM41256A2 TMM41257A2				
	1M		TCS11000J TCS11001J TCS11002J TCS14256J TCS14258J		TCS11000Z TCS11001Z TCS11002Z TCS14256Z TCS14258Z			
	3M/9M					THM81000S/L THM91000S/L		
Static RAM	16K						TCS517CF TCS518CF	
	64K							TC5564AF L TC5565AF L
	256K							TC55257AF
Mask ROM	256K							TC53257F
	1M							TC531000AF
OTP	64K							TMM2464AF
	128K							TMM24128AF
	256K							TMM24256AF TCS4256AF
	512K							TMM24512F

**TOSHIBA BYTE-WIDE MEMORY PIN OUT FOR 28/32 PIN DEVICES**

Capacity	Memory Type	Part Number	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 12	Pin 13	Pin 14	Pin 15	Pin 16	Pin 17	Pin 18	Pin 19	Pin 20	Pin 21	Pin 22	Pin 23	Pin 24	Pin 25	Pin 26	Pin 27	Pin 28	Pin 29	Pin 30	Pin 31	Pin 32		
4M BIT	MROM	TC534000	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
2M BIT	MROM	TC532000	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
1M BIT	MROM	TC531001	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
	EPROM	TC571001																																		
	MROM	TC571000																																		
512K BIT	OTP	TMM24512	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
	EPROM	TMM27512																																		
1M BIT	MROM	TC531000	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	EPROM	TC571000																																		
	MROM	TC571001																																		
512K BIT	EPROM	TMM27512	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
	OTP	TMM24512																																		
2M BIT	MROM	TC532000	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
4M BIT	MROM	TC534000	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓



**TOSHIBA BYTE-WIDE MEMORY PIN OUT FOR 24/28 PIN DEVICES**

Memory Type	Device	1M BIT	512K BIT	256K BIT	128K BIT	72K BIT	64K BIT	16K BIT	16K BIT	64K BIT	72K BIT	128K BIT	256K BIT	512K BIT	1M BIT
MROM	TC531000														
OTP	TMM27512														
	TMM24512														
MROM	TC53257														
	TC54256/TMM24256														
	TC57256/TMM27256														
	TC55257														
OTP	TMM24128A														
	TMM27128A														
H.S. SRAM		TMM2089													
CRAM	TC5564/65														
	TMM2063/64/88														
	TMM2464A														
	TMM2764A														
CRAM	TC5517														
	TC5516/18														
	TMM2018														
H.S. SRAM		TMM2018													
SRAM		TMM2015/16													
SRAM		TMM2015/16													
H.S. SRAM		TMM2018													
CRAM		TC5517													
CRAM		TC5516/18													
EPROM		TMM2764A													
OTP		TMM2464A													
SRAM		TMM2063/64/88													
CRAM		TC5564/65													
H.S. SRAM		TMM2089C													
EPROM	TMM27128A														
	TMM24128A														
CRAM	TC55257														
	TC57256/TMM27256														
	TC54256/TMM24256														
MROM		TC53257													
EPROM	TMM27512														
	TMM24512														
MROM		TC531000													

# Dynamic RAMs



# TOSHIBA MOS MEMORY PRODUCT

262,144 WORD × 1 BIT DYNAMIC RAM  
N-CHANNEL SILICON GATE MOS

TMM41256P/T-12  
TMM41256P/T-15

## DESCRIPTION

The TMM41256P/T is the new generation dynamic RAM organized 262,144 words by 1 bit, it is successor to the industry standard TMM4164AP.

The TMM41256P/T utilizes TOSHIBA's N-channel Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TMM-

41256P T to be packaged in a standard 16 pin plastic DIP and 18 pin plastic leaded chip carrier. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include single power supply of 5V ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

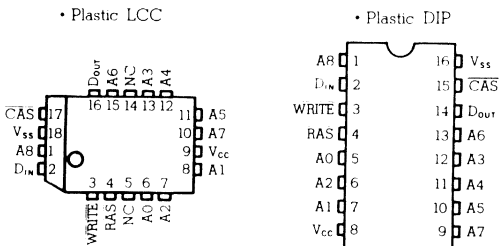
## FEATURES

- 262,144 words by 1 bit organization
- Fast access time and cycle time

DEVICE	t <sub>RAC</sub>	t <sub>CAC</sub>	t <sub>RC</sub>
TMM41256P T-12	120 ns	60 ns	220 ns
TMM41256P T-15	150 ns	75 ns	260 ns

- Single power supply of 5V ±10% with a built-in V<sub>BB</sub> generator
- Low Power:
  - 330mW Operating (MAX.) (TMM41256P/T-12)
  - 275mW Operating (MAX.) (TMM41256P/T-15)
  - 28mW Stand by (MAX.)

## PIN CONNECTION (TOP VIEW)

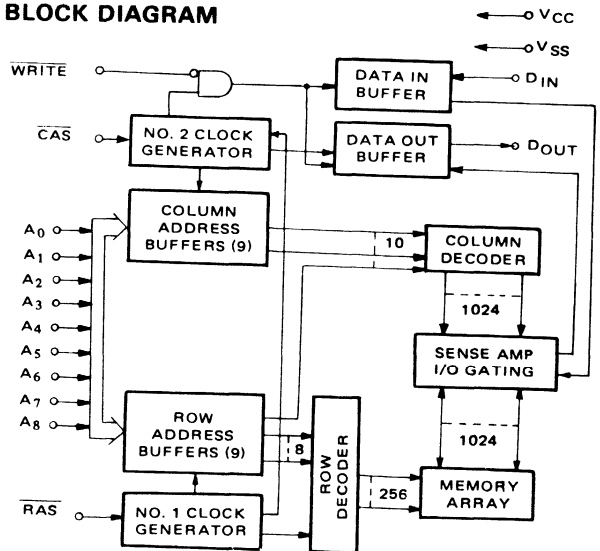


## PIN NAMES

A <sub>0</sub> ~ A <sub>8</sub>	Address Inputs
CAS	Column Address Strobe
D <sub>IN</sub>	Data In
D <sub>OUT</sub>	Data Out
RAS	Row Address Strobe
WRITE	Read/Write Input
V <sub>CC</sub>	Power (+5V)
V <sub>SS</sub>	Ground

- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write,  $\overline{\text{RAS}}$ -only refresh, Hidden refresh, and Page Mode capability.
- All inputs and output TTL compatible
- 256 refresh cycles/4ms
- Package
  - Plastic DIP : TMM41256P
  - Plastic Leaded Chip Carrier : TMM41256T

## BLOCK DIAGRAM



# TMM41256P/T-12

# TMM41256P/T-15

## ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	$V_{IN}, V_{OUT}$	-1 ~ 7	V	1
Power Supply Voltage	$V_{CC}$	-1 ~ 7	V	1
Operating Temperature	$T_{OPR}$	0 ~ 70	°C	1
Storage Temperature	$T_{STG}$	-55 ~ 150	°C	1
Soldering Temperature · Time	$T_{SOLDER}$	260 · 10	°C · sec	1
Power Dissipation	$P_D$	600	mW	1
Short Circuit Output Current	$I_{OUT}$	50	mA	1

## RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
$V_{CC}$	Supply Voltage	4.5	5.0	5.5	V	2
$V_{IH}$	Input High Voltage	2.4	—	6.5	V	2
$V_{IL}$	Input Low Voltage	-1.0	—	0.8	V	2

## DC ELECTRICAL CHARACTERISTICS (VCC = 5V ± 10%, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES	
$I_{CC1}$	OPERATING CURRENT Average Power Supply Operating Current (RAS, CAS Cycling: $t_{RC} = t_{RC \text{ MIN.}}$ )	TMM41256P T-12	—	60	mA	3, 4
		TMM41256P T-15	—	50		
$I_{CC2}$	STANDBY CURRENT Power Supply Standby Current (RAS = CAS = $V_{IH}$ )	—	5	mA		
$I_{CC3}$	REFRESH CURRENT Average Power Supply Current, Refresh Mode (RAS Cycling, CAS = $V_{IH}$ ; $t_{RC} = t_{RC \text{ MIN.}}$ )	TMM41256P T-12	—	45	mA	3
		TMM41256P T-15	—	40		
$I_{CC4}$	PAGE MODE CURRENT Average Power Supply Current, Page Mode (RAS = $V_{IL}$ , CAS Cycling: $t_{PC} = t_{PC \text{ MIN.}}$ )	TMM41256P T-12	—	45	mA	3, 4
		TMM41256P T-15	—	40		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ( $0V \leq V_{IN} \leq 6.5V$ , All Other Pins Not Under Test = 0V)	-10	10	$\mu A$		
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT ( $D_{OUT}$ is disabled, $0V \leq V_{OUT} \leq +5.5V$ )	-10	10	$\mu A$		
$V_{OH}$	OUTPUT LEVEL Output "H" Level Voltage ( $I_{OUT} = -5mA$ )	2.4	—	V		
$V_{OL}$	OUTPUT LEVEL Output "L" Level Voltage ( $I_{OUT} = 4.2mA$ )	—	0.4	V		



# TMM41256P/T-12

# TMM41256P/T-15

## ELECTRIAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V<sub>CC</sub> = 5V ± 10%, T<sub>a</sub> = 0 ~ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TMM41256P T-12		TMM41256P T-15		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t <sub>RC</sub>	Random Read or Write Cycle Time	220	—	260	—	ns	
t <sub>RWC</sub>	Read-Write Cycle Time	240	—	285	—	ns	
t <sub>RMW</sub>	Read-Modify-Write Cycle Time	260	—	310	—	ns	
t <sub>PC</sub>	Page Mode Cycle Time	120	—	145	—	ns	
t <sub>PRWC</sub>	Page Mode Read-Write Cycle Time	140	—	170	—	ns	
t <sub>PRMW</sub>	Page Mode Read-Modify-Write Cycle Time	160	—	195	—	ns	
t <sub>RAC</sub>	Access Time from $\overline{\text{RAS}}$	—	120	—	150	ns	8, 10
t <sub>CAC</sub>	Access Time from $\overline{\text{CAS}}$	—	60	—	75	ns	9, 10
t <sub>OFF</sub>	Output Buffer Turn-Off Delay	0	35	0	40	ns	11
t <sub>t</sub>	Transition Time (Rise and Fall)	3	50	3	50	ns	6
t <sub>RP</sub>	RAS Precharge Time	90	—	100	—	ns	
t <sub>RAS</sub>	RAS Pulse Width	120	10,000	150	10,000	ns	
t <sub>RSH</sub>	RAS Hold Time	60	—	75	—	ns	
t <sub>CSH</sub>	CAS Hold Time	120	—	150	—	ns	
t <sub>CAS</sub>	CAS Pulse Width	60	10,000	75	10,000	ns	
t <sub>PCD</sub>	RAS to CAS Delay Time	25	60	25	75	ns	13
t <sub>CRP</sub>	CAS to RAS Precharge Time	10	—	10	—	ns	
t <sub>CPN</sub>	CAS Precharge Time	25	—	25	—	ns	
t <sub>CP</sub>	CAS Precharge Time (for Page Mode Cycle Only)	50	—	60	—	ns	
t <sub>ASR</sub>	Row Address Set-Up Time	0	—	0	—	ns	
t <sub>RAH</sub>	Row Address Hold Time	15	—	15	—	ns	
t <sub>ASC</sub>	Column Address Set-Up Time	0	—	0	—	ns	
t <sub>CAH</sub>	Column Address Hold Time	25	—	30	—	ns	
t <sub>AR</sub>	Column Address Hold Time Reference to $\overline{\text{RAS}}$	95	—	120	—	ns	
t <sub>RCS</sub>	Read Command Set-Up Time	0	—	0	—	ns	
t <sub>RCH</sub>	Read Command Hold Time Reference to $\overline{\text{CAS}}$	0	—	0	—	ns	12
t <sub>PRH</sub>	Read Command Hold Time Reference to $\overline{\text{RAS}}$	15	—	20	—	ns	12
t <sub>WCH</sub>	Write Command Hold Time	35	—	45	—	ns	
t <sub>WCR</sub>	Write Command Hold Time Reference to $\overline{\text{RAS}}$	95	—	120	—	ns	
t <sub>WP</sub>	Write Command Pulse Width	35	—	45	—	ns	
t <sub>RWL</sub>	Write Command to $\overline{\text{RAS}}$ Lead Time	35	—	45	—	ns	
t <sub>CWL</sub>	Write Command to $\overline{\text{CAS}}$ Lead Time	35	—	45	—	ns	
t <sub>DS</sub>	Data-In Set-Up Time	0	—	0	—	ns	
t <sub>DH</sub>	Data-In Hold Time	35	—	45	—	ns	14
t <sub>DHR</sub>	Data-In Hold Time Reference to $\overline{\text{RAS}}$	95	—	120	—	ns	14
t <sub>REF</sub>	Refresh Period	—	4	—	4	ms	
t <sub>WCS</sub>	Write Command Set-Up Time	-10	—	-10	—	ns	15
t <sub>CWD</sub>	CAS to $\overline{\text{WRITE}}$ Delay	40	—	50	—	ns	15
t <sub>RWD</sub>	RAS to $\overline{\text{WRITE}}$ Delay	100	—	125	—	ns	15

# TMM41256P/T-12

# TMM41256P/T-15

## CAPACITANCE

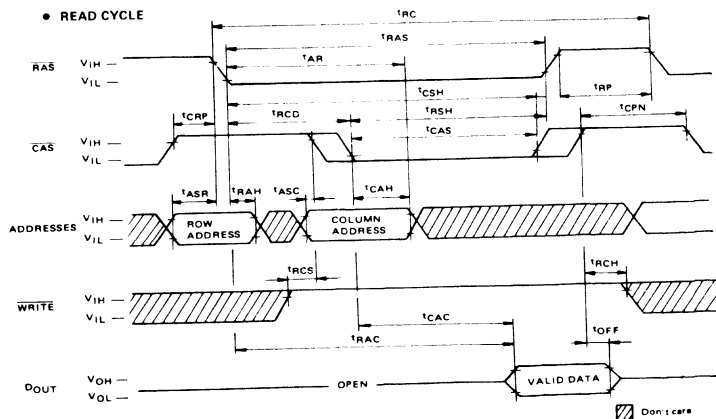
( $V_{CC} = 5V \pm 10\%$ ,  $f = 1\text{MHz}$ ,  $T_a = 0 \sim 70^\circ\text{C}$ )

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
$C_{I1}$	Input Capacitance ( $A_0 \sim A_8, D_{IN}$ )	—	5	pF
$C_{I2}$	Input Capacitance ( $\overline{RAS}, \overline{CAS}, \overline{WRITE}$ )	—	7	pF
$C_O$	Output Capacitance ( $D_{OUT}$ )	—	7	pF

## NOTES

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
- All voltages are referenced to  $V_{SS}$ .
- $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  depend on cycle rate.
- $I_{CC1}$ ,  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
- An initial pause of  $200\mu\text{s}$  is required after power-up followed by any 8  $\overline{RAS}$  cycles before proper device operation is achieved.
- AC measurements assume  $t_T = 5\text{ns}$ .
- $V_{IH}$  (min.) and  $V_{IL}$  (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- Assumes that  $t_{RCD} \leq t_{RCD}(\text{max.})$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds the value shown.
- Assumes that  $t_{RCD} \geq t_{RCD}(\text{max.})$
- Measured with a load equivalent to 2 TTL loads and  $100\text{pF}$ .
- $t_{OFF}(\text{max.})$  defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
- Operation within the  $t_{RCD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
- These parameters are referenced to  $\overline{CAS}$  leading edge in early write cycles and to  $\overline{WRITE}$  leading edge in read-write or read-modify-write cycles.
- $t_{WCS}$ ,  $t_{CWD}$  and  $t_{RWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{CWD} \geq t_{CWD}(\text{min.})$  and  $t_{RWD} \geq t_{RWD}(\text{min.})$ , the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

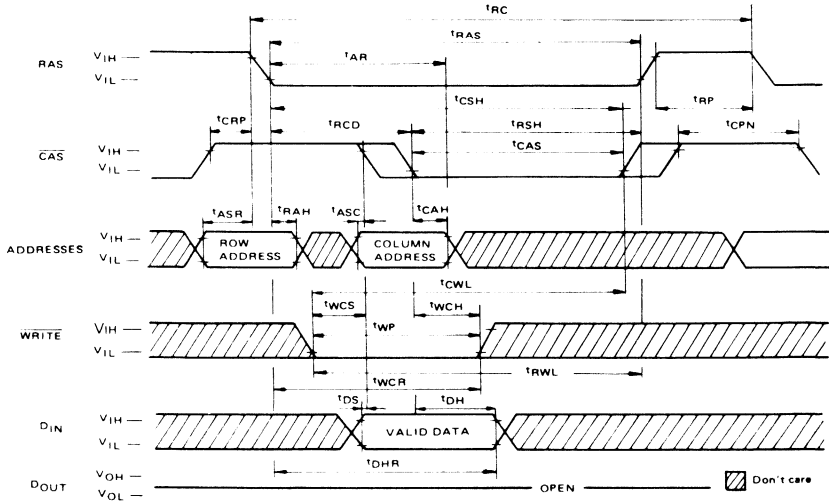
## TIMING WAVEFORMS



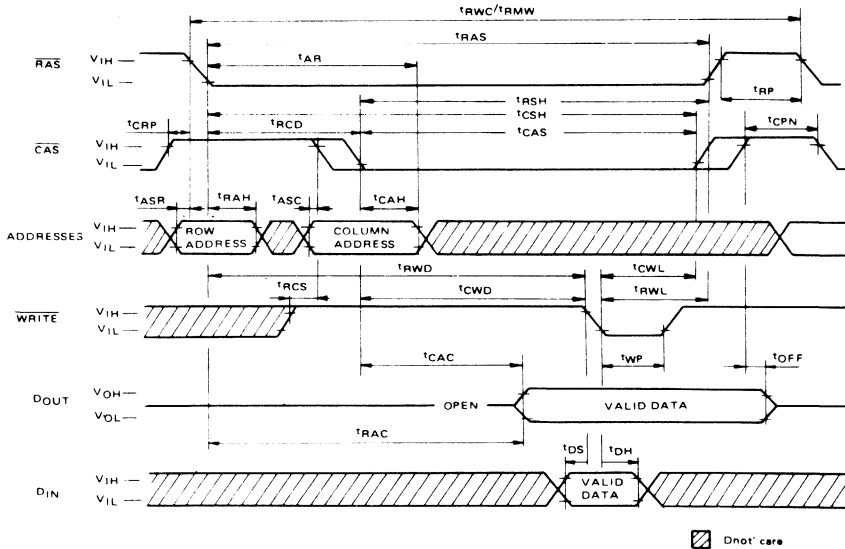
# TMM41256P/T-12

# TMM41256P/T-15

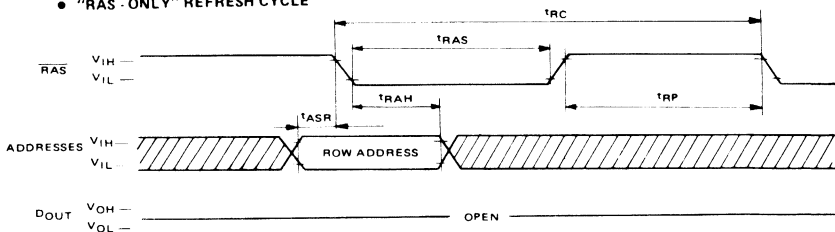
## • WRITE CYCLE (EARLY WRITE)



## • READ-WRITE/READ-MODIFY-WRITE CYCLE



## • "RAS-ONLY" REFRESH CYCLE

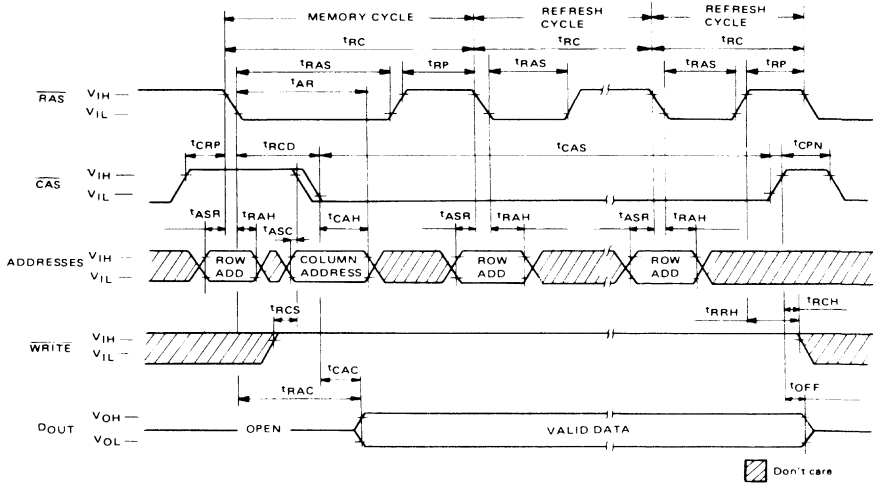


Note:  $\overline{\text{CAS}} = V_{IH}$ ,  $\overline{\text{WRITE}} = \text{Don't care}$ ,  $A_8 = \text{Don't care}$

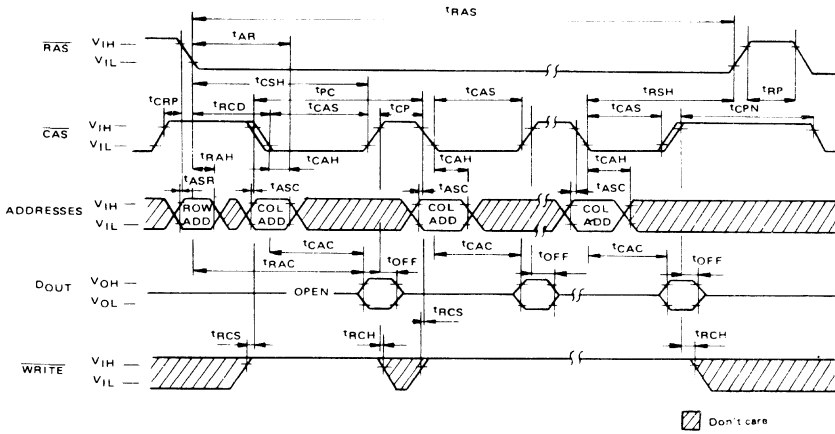
# TMM41256P/T-12

# TMM41256P/T-15

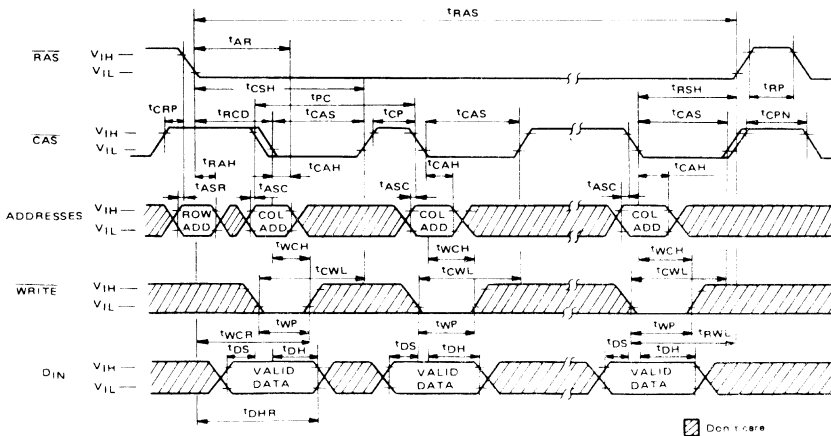
## • HIDDEN REFRESH CYCLE



## • PAGE MODE READ CYCLE

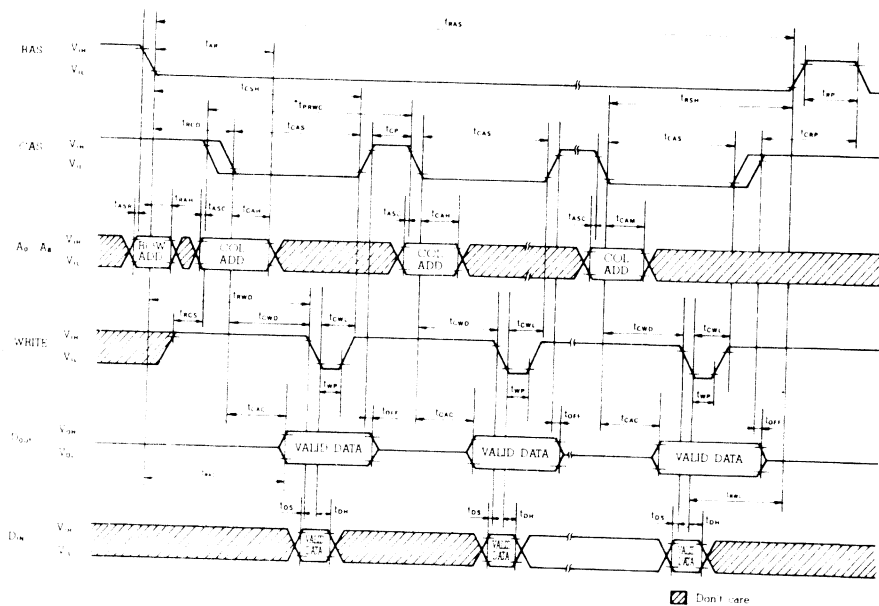


## • PAGE MODE WRITE CYCLE



# TMM41256P/T-12 TMM41256P/T-15

• PAGE MODE READ-WRITE READ MODIFY WRITE CYCLE



# TMM41256P/T-12

# TMM41256P/T-15

## APPLICATION INFORMATION

### ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TMM41256P/T are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ( $\overline{RAS}$ ), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe ( $\overline{CAS}$ ), subsequently latches the 9 column address bits into the chip. Each of these signals,  $\overline{RAS}$  and  $\overline{CAS}$ , triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the  $\overline{CAS}$  clock sequence are inhibited until the occurrence of a delayed signal derived from the  $\overline{RAS}$  clock chain. This "gated  $\overline{CAS}$ " feature allows the  $\overline{CAS}$  clock to be externally activated as soon as the Row Address Hold Time specification ( $t_{RAH}$ ) has been satisfied and the address inputs have been changed from Row address to Column address information.

### DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of  $\overline{WRITE}$  and  $\overline{CAS}$  while  $\overline{RAS}$  is active. The later of the signals ( $\overline{WRITE}$  or  $\overline{CAS}$ ) to make its negative transition is the strobe for the Data In ( $D_{IN}$ ) register. This permits several options in the write cycle timing. In a write cycle, if the  $\overline{WRITE}$  input is brought low (active) prior to  $\overline{CAS}$ , the  $D_{IN}$  is strobed by  $\overline{CAS}$  and the set-up and hold times are referenced to  $\overline{CAS}$ . If the input data is not available at  $\overline{CAS}$  time or if it is desired that the cycle be a read-write cycle, the  $\overline{WRITE}$  signal will be delayed until after  $\overline{CAS}$  has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of  $\overline{WRITE}$  rather than  $\overline{CAS}$ . (To illustrate this feature,  $D_{IN}$  is referenced to  $\overline{WRITE}$  in the timing diagrams depicting the read-write and page mode write cycles while the "early write" cycle diagram shows  $D_{IN}$  referenced to  $\overline{CAS}$ ).

Data is retrieved from the memory in a read

cycle by maintaining  $\overline{WRITE}$  in the inactive or high state throughout the portion of the memory cycle in which  $\overline{CAS}$  is active (low). Data read from the selected cell will be available at the output within the specified access time.

### DATA OUTPUT CONTROL

The normal condition of the Data Output ( $D_{OUT}$ ) of the TMM41256P/T is the high impedance (open circuit) state. This is to say, anytime  $\overline{CAS}$  is at a high level, the  $D_{OUT}$  pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle.  $D_{OUT}$  will remain valid from access time until  $\overline{CAS}$  is taken back to the inactive (high level) condition.

### PAGE MODE

The "Page-Mode" feature of the TMM41256P/T allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the  $\overline{RAS}$  signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page Mode" of operation will not dissipate the power associated with the negative going edge of  $\overline{RAS}$ . Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

### REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address ( $A_0 \sim A_7$ ) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with " $\overline{RAS}$  - only" cycles,  $\overline{RAS}$  only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the  $I_{CC3}$  specification.

### HIDDEN REFRESH

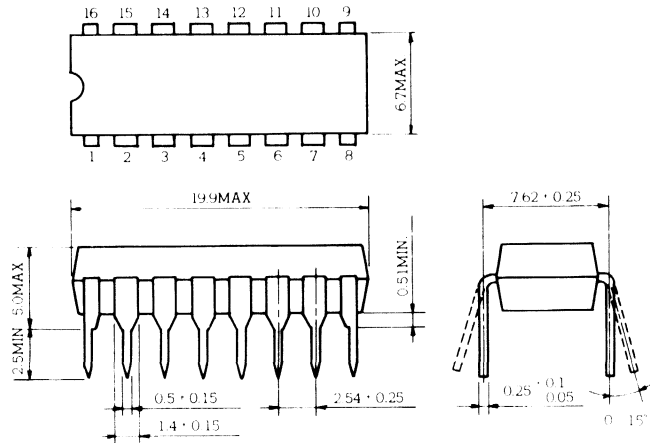
An optional feature of the TMM41256P/T is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding  $\overline{CAS}$  at  $V_{IL}$  and taking  $\overline{RAS}$  high and after a specified precharge period ( $t_{PP}$ ), executing a " $\overline{RAS}$  - only" refresh cycle, but with  $\overline{CAS}$  held low

# TMM41256P/T-12 TMM41256P/T-15

## OUTLINE DRAWINGS

### ● Plastic DIP

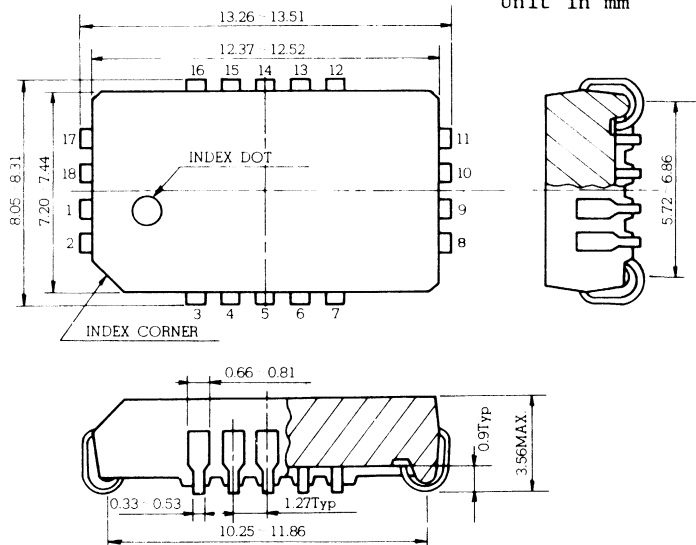
Unit in mm



Note : Each lead pitch is 2.54 mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 16 leads. All dimensions are in millimeters.

### ● Plastic LCC

Unit in mm



Note : Each lead pitch is 1.27mm.

# TMM41256P/T-12

# TMM41256P/T-15

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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# TOSHIBA MOS MEMORY PRODUCT

## TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

### DESCRIPTION

The TMM41256AP/AT/AZ is the N-channel dynamic RAM organized 262,144 words by 1 bit. Multiplexed address inputs permit the TMM41256AP/AT/AZ to be packaged in a standard 16 pin plastic DIP, 18 pin PLCC and 16 pin ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. The double layered MOS technology with polycide and poly Si permits the TMM41256AP/AT/AZ high speed operation. Also, the advanced circuit techniques have realized low power dissipation. System oriented features include single power supply of  $5V \pm 10\%$  tolerance, direct interfacing capability with high performance logic families such as schottky TTL. In addition to the  $\overline{\text{RAS}}$  only refresh mode, a  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  automatic refresh is available. Another special feature of TMM41256AP/AT/AZ is page mode, allowing the user to access at a high data rate.

### FEATURES

- 262,144 words by 1 bit organization
- Fast access time and cycle time

	TMM41256AP/AT/AZ-10/-12/-15
$\overline{\text{RAS}}$ Access Time	100ns/120ns/150ns
$\overline{\text{CAS}}$ Access Time	50ns/ 60ns/ 75ns
Cycle Time	190ns/220ns/260ns

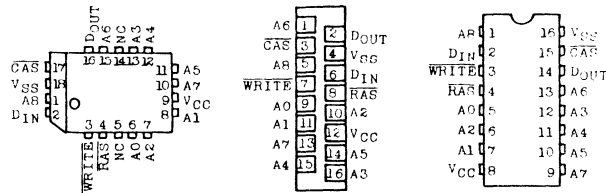
- Single power supply of  $5V \pm 10\%$  with a built-in  $V_{\text{BB}}$  generator
- Low Power:
  - 440mW MAX. Operating (TMM41256AP/AT/AZ-10)
  - 385mW MAX. Operating (TMM41256AP/AT/AZ-12)
  - 330mW MAX. Operating (TMM41256AP/AT/AZ-15)
  - 28mW MAX. Standby

- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write,  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh,  $\overline{\text{RAS}}$ -only refresh, Hidden refresh, and Page Mode capability
- All inputs and output TTL compatible
- 256 refresh cycles/4ms
- Package

Plastic DIP : TMM41256AP  
Plastic Leaded Chip Carrier: TMM41256AT  
Plastic ZIP : TMM41256AZ

### PIN CONNECTION (TOP VIEW)

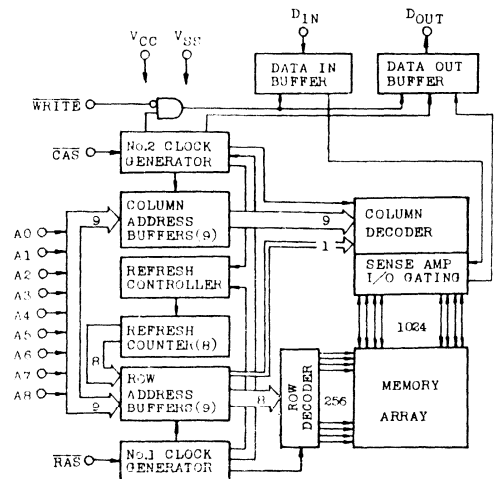
- Plastic LCC
- Plastic ZIP
- Plastic DIP



### PIN NAMES

A0 ~ A8	Address Inputs
CAS	Column Address Strobe
DIN	Data In
DOUT	Data Out
$\overline{\text{RAS}}$	Row Address Strobe
WRITE	Read/Write Input
VCC	Power (+5V)
VSS	Ground

### BLOCK DIAGRAM



# TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

## ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	V <sub>IN</sub> , V <sub>OUT</sub>	-1 ~ 7	V	1
Power Supply Voltage	V <sub>CC</sub>	-1 ~ 7	V	
Operating Temperature	T <sub>OPR</sub>	0 ~ 70	°C	
Storage Temperature	T <sub>STG</sub>	-55 ~ 150	°C	
Soldering Temperature • Time	T <sub>SOLDER</sub>	260 • 10	°C • sec	
Power Dissipation	P <sub>D</sub>	600	mW	
Short Circuit Output Current	I <sub>OUT</sub>	50	mA	

## RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V	2
V <sub>IH</sub>	Input High Voltage	2.4	-	6.5	V	
V <sub>IL</sub>	Input Low Voltage	-1.0	-	0.8	V	

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5V±10%, T<sub>a</sub> = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES	
I <sub>CC1</sub>	OPERATING CURRENT Average Power Supply Operating Current ( $\overline{RAS}$ , $\overline{CAS}$ Cycling: $t_{RC}=t_{RC\ MIN.}$ )	TMM41256AP/AT/AZ-10	-	80	mA	3,4
		TMM41256AP/AT/AZ-12	-	72	mA	
		TMM41256AP/AT/AZ-15	-	65	mA	
I <sub>CC2</sub>	STANDBY CURRENT Power Supply Standby Current ( $\overline{RAS}=\overline{CAS}=V_{IH}$ )	-	5	mA		
I <sub>CC3</sub>	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Refresh Mode ( $\overline{RAS}$ Cycling, $\overline{CAS}=V_{IH}$ : $t_{RC}=t_{RC\ MIN.}$ )	TMM41256AP/AT/AZ-10	-	70	mA	3
		TMM41256AP/AT/AZ-12	-	62	mA	
		TMM41256AP/AT/AZ-15	-	55	mA	
I <sub>CC4</sub>	PAGE MODE CURRENT Average Power Supply Current, Page Mode ( $\overline{RAS}=V_{IL}$ , $\overline{CAS}$ Cycling: $t_{PC}=t_{PC\ MIN.}$ )	TMM41256AP/AT/AZ-10	-	60	mA	3,4
		TMM41256AP/AT/AZ-12	-	55	mA	
		TMM41256AP/AT/AZ-15	-	50	mA	
I <sub>CC5</sub>	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Mode ( $\overline{RAS}$ , $\overline{CAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$ : $t_{RC}=t_{RC\ MIN.}$ )	TMM41256AP/AT/AZ-10	-	70	mA	3
		TMM41256AP/AT/AZ-12	-	62	mA	
		TMM41256AP/AT/AZ-15	-	55	mA	
I <sub>I(L)</sub>	INPUT LEAKAGE CURRENT Input Leakage Current, any input ( $0V \leq V_{IN} \leq 6.5V$ , ALL Other Pins Not Under Test = 0V)	-10	10	μA		
I <sub>O(L)</sub>	OUTPUT LEAKAGE CURRENT (D <sub>OUT</sub> is disabled, $0V \leq V_{OUT} \leq +5.5V$ )	-10	10	μA		
V <sub>OH</sub>	OUTPUT LEVEL Output "H" Level Voltage (I <sub>OUT</sub> = -5mA)	2.4	-	V		
V <sub>OL</sub>	OUTPUT LEVEL Output "L" Level Voltage (I <sub>OUT</sub> = 4.2mA)	-	0.4	V		

# TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM41256AP/ AT/AZ-10		TMM41256AP/ AT/AZ-12		TMM41256AP/ AT/AZ-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$t_{RC}$	Random Read or Write Cycle Time	190	-	220	-	260	-	ns	
$t_{RWC}$	Read-Write Cycle Time	200	-	240	-	265	-	ns	
$t_{RMW}$	Read-Modify-Write Cycle Time	220	-	260	-	310	-	ns	
$t_{PC}$	Page Mode Cycle Time	100	-	120	-	145	-	ns	
$t_{PRWC}$	Page Mode Read-Write Cycle Time	110	-	140	-	170	-	ns	
$t_{PRMW}$	Page Mode Read-Modify Write Cycle Time	130	-	160	-	195	-	ns	
$t_{RAC}$	Access Time from $\overline{RAS}$	-	100	-	120	-	150	ns	8,10
$t_{CAC}$	Access Time from $\overline{CAS}$	-	50	-	60	-	75	ns	9,10
$t_{OFF}$	Output Buffer Turn-Off Delay	5	25	5	30	5	35	ns	11
$t_T$	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
$t_{RP}$	$\overline{RAS}$ Precharge Time	80	-	90	-	100	-	ns	
$t_{RAS}$	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000	150	10,000	ns	
$t_{RSH}$	$\overline{RAS}$ Hold Time	50	-	60	-	75	-	ns	
$t_{CSH}$	$\overline{CAS}$ Hold Time	100	-	120	-	150	-	ns	
$t_{CAS}$	$\overline{CAS}$ Puls	50	10,000	60	10,000	75	10,000	ns	
$t_{RCD}$	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	50	25	60	25	75	ns	13
$t_{CRP}$	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
$t_{CPN}$	$\overline{CAS}$ Precharge Time	15	-	20	-	25	-	ns	
$t_{CP}$	Page Mode $\overline{CAS}$ Precharge Time	40	-	50	-	60	-	ns	
$t_{ASR}$	Row Address Set-Up Time	0	-	0	-	0	-	ns	
$t_{RAH}$	Row Address Hold Time	15	-	15	-	15	-	ns	
$t_{ASC}$	Column Address Set-Up Time	0	-	0	-	0	-	ns	
$t_{CAH}$	Column Address Hold Time	20	-	25	-	30	-	ns	
$t_{AR}$	Column Address Hold Time Reference to $\overline{RAS}$	70	-	85	-	105	-	ns	
$t_{RCS}$	Read Command Set-Up Time	0	-	0	-	0	-	ns	
$t_{RCH}$	Read Command Hold Time Reference to $\overline{CAS}$	0	-	0	-	0	-	ns	
$t_{RRH}$	Read Command Hold Time Reference to $\overline{RAS}$	10	-	15	-	20	-	ns	
$t_{WCH}$	Write Command Hold Time	20	-	25	-	30	-	ns	

**TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12  
TMM41256AP/AT/AZ-15**

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TMM41526AP/ AT/AZ-10		TMM41526AP/ AT/AZ-12		TMM41526AP/ AT/AZ-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t <sub>WCR</sub>	Write Command Hold Time Reference to $\overline{\text{RAS}}$	70	-	85	-	105	-	ns	
t <sub>WP</sub>	Write Command Pulse Width	20	-	25	-	30	-	ns	
t <sub>RWL</sub>	Write Command to $\overline{\text{RAS}}$ Lead Time	25	-	35	-	45	-	ns	
t <sub>CWL</sub>	Write Command to $\overline{\text{CAS}}$ Lead Time	25	-	35	-	45	-	ns	
t <sub>DS</sub>	Data-In Set-Up Time	0	-	0	-	0	-	ns	14
t <sub>DH</sub>	Data-In Hold Time	20	-	25	-	30	-	ns	14
t <sub>DHR</sub>	Data-In Hold Time Reference to $\overline{\text{RAS}}$	70	-	85	-	105	-	ns	
t <sub>REF</sub>	Refresh Period	-	4	-	4	-	4	ms	
t <sub>WCS</sub>	Write Command Set-Up Time	0	-	0	-	0	-	ns	15
t <sub>CWD</sub>	$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ Delay	30	-	40	-	50	-	ns	15
t <sub>RWD</sub>	$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ Delay	80	-	100	-	125	-	ns	15
t <sub>CSR</sub>	$\overline{\text{CAS}}$ Set-Up Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	10	-	10	-	10	-	ns	
t <sub>CHR</sub>	$\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	30	-	30	-	30	-	ns	
t <sub>RPC</sub>	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	0	-	0	-	0	-	ns	
t <sub>CPT</sub>	$\overline{\text{CAS}}$ Precharge Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Counter Test)	40	-	50	-	60	-	ns	

CAPACITANCE ( $T_{CC}=5V\pm 10\%$ ,  $f=1\text{MHz}$ ,  $T_a=0\sim 70^\circ\text{C}$ )

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
C <sub>I1</sub>	Input Capacitance ( $A_0$ , $A_8$ , $D_{IN}$ )	-	5	pF
C <sub>I2</sub>	Input Capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WRITE}}$ )	-	7	
C <sub>O</sub>	Output Capacitance ( $D_{OUT}$ )	-	7	

# TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

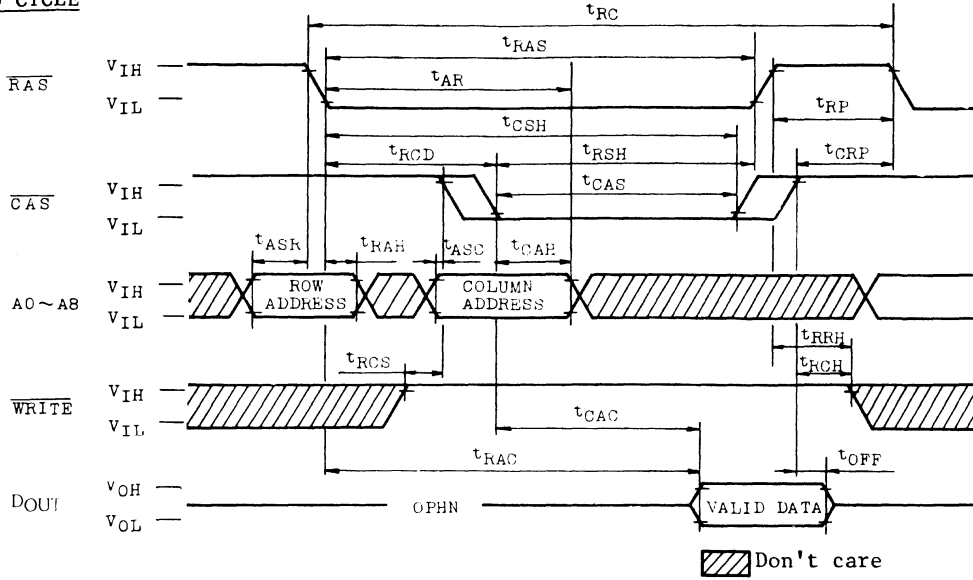
## NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to  $V_{SS}$ .
3.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ ,  $I_{CC5}$  depend on cycle rate.
4.  $I_{CC1}$ ,  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200 $\mu$ s is required after power-up followed by any 8  $\overline{RAS}$  cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS Before RAS initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
6. AC measurement assume  $t_f=5$ ns.
7.  $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
8. Assumes that  $t_{RCD} \leq t_{RCD}(\text{max.})$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds the value shown.
9. Assume that  $t_{RCD} \leq t_{RCD}(\text{max.})$
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11.  $t_{OFF}(\text{max.})$  defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
13. Operation within the  $t_{RCD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
14. These parameters are referenced to  $\overline{CAS}$  leading edge in early write cycles and to  $\overline{WRITE}$  leading edge in read-write or read-modify-write cycles.
15.  $t_{WCS}$ ,  $t_{CWD}$  and  $t_{RWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If  $t_{CWD} \geq t_{CWD}(\text{min.})$  and  $t_{RWD} \geq t_{RWD}(\text{min.})$ , the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

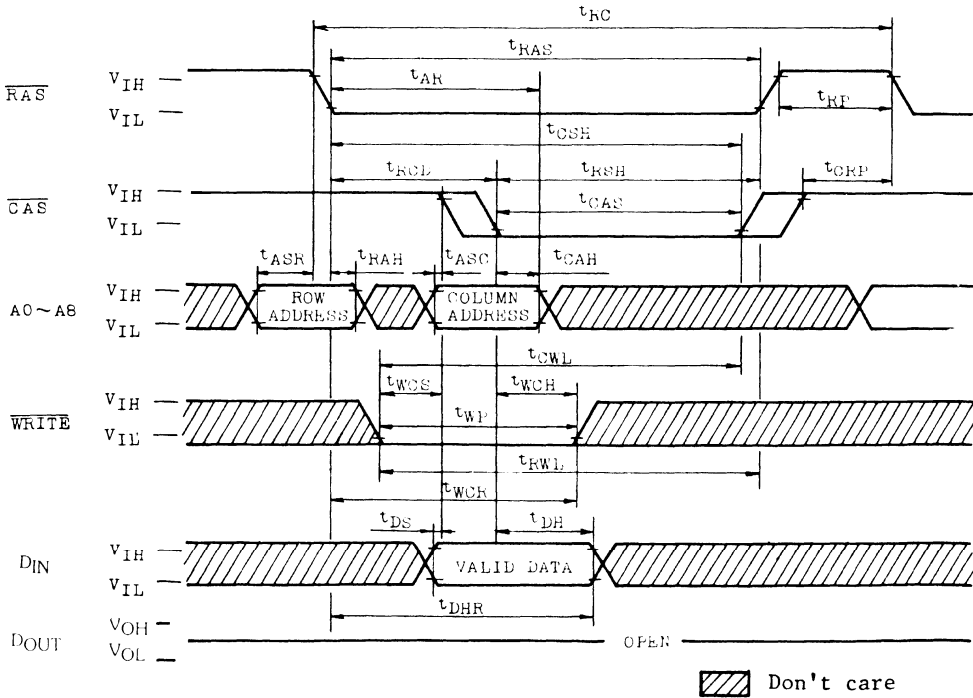
# TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

## TIMING WAVEFORMS

### READ CYCLE

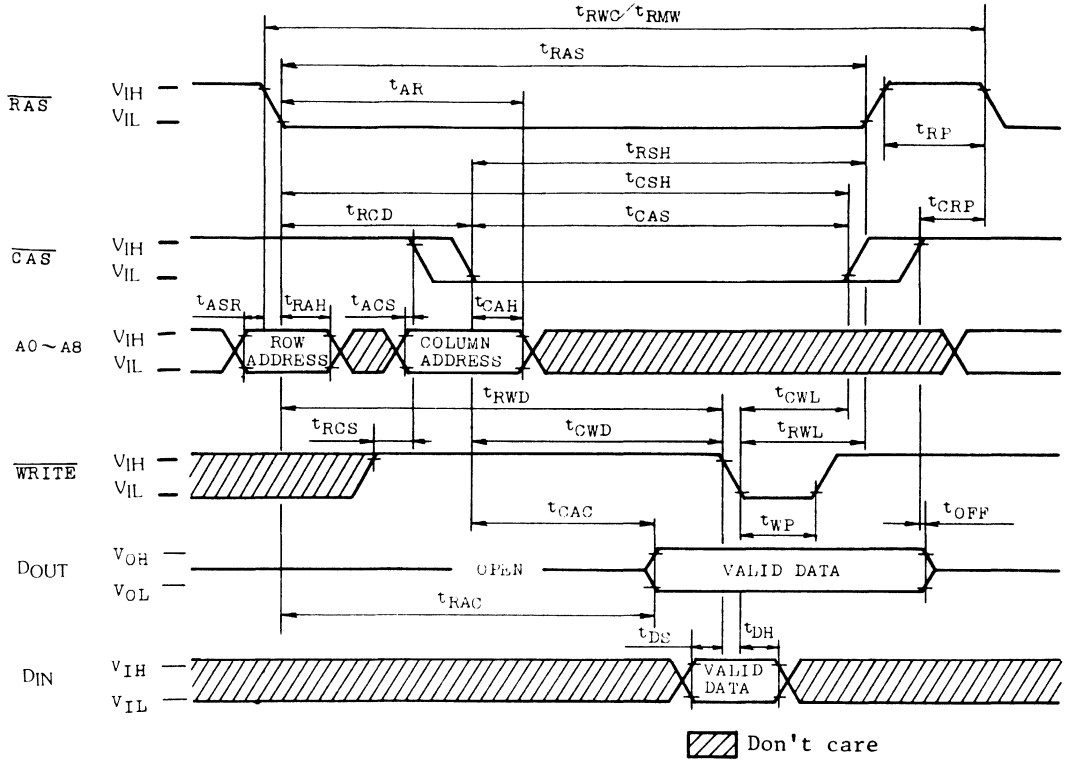


### WRITE CYCLE (EARLY WRITE)



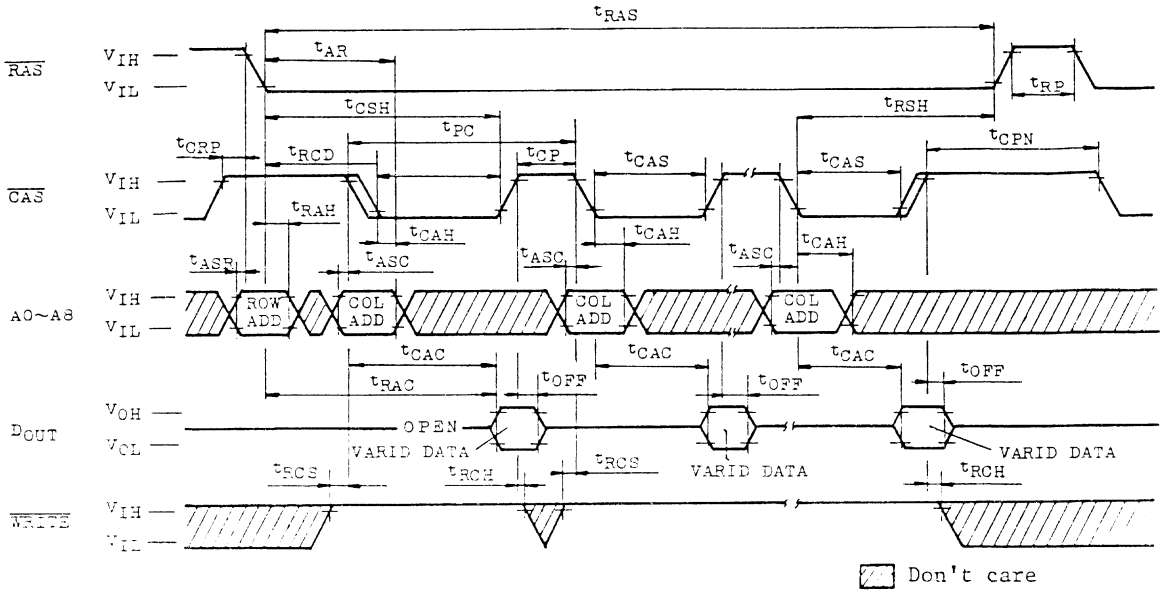
# TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

## READ-WRITE/READ-MODIFY-WRITE CYCLE

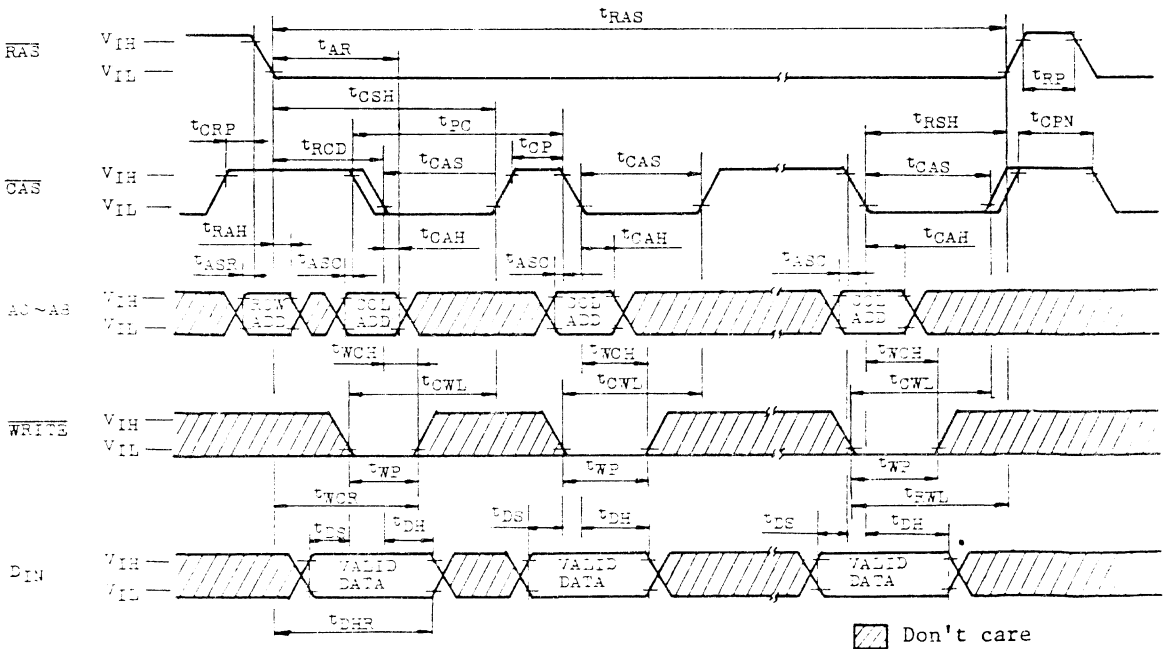


# TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

## PAGE MODE READ CYCLE



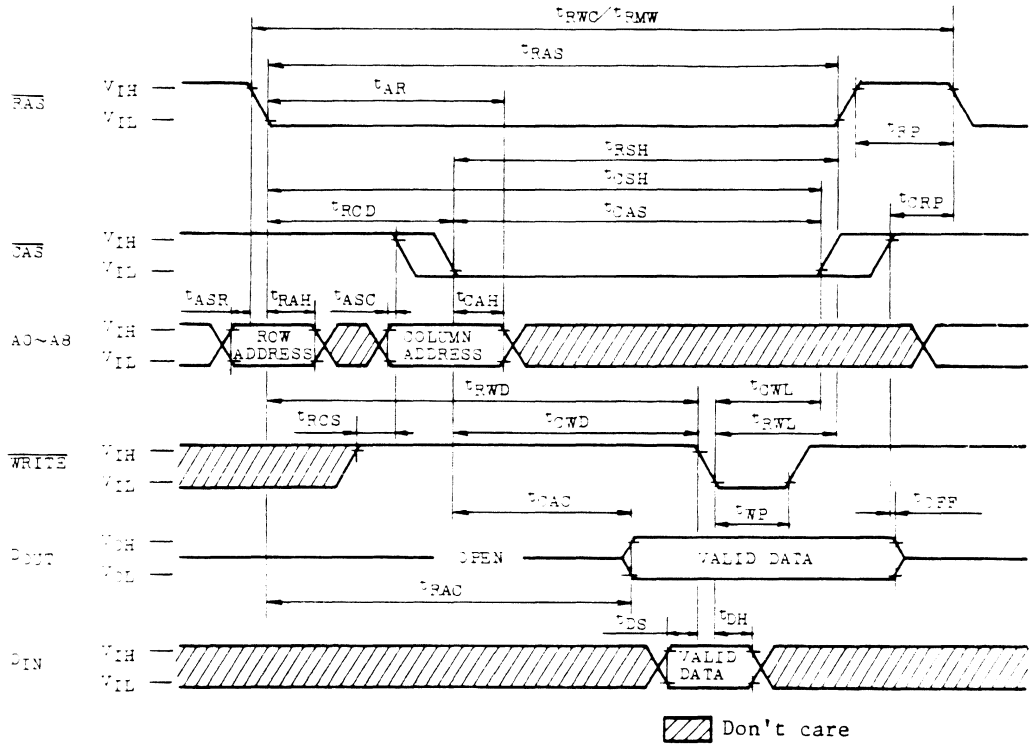
## PAGE MODE WRITE CYCLE (EARLY WRITE)





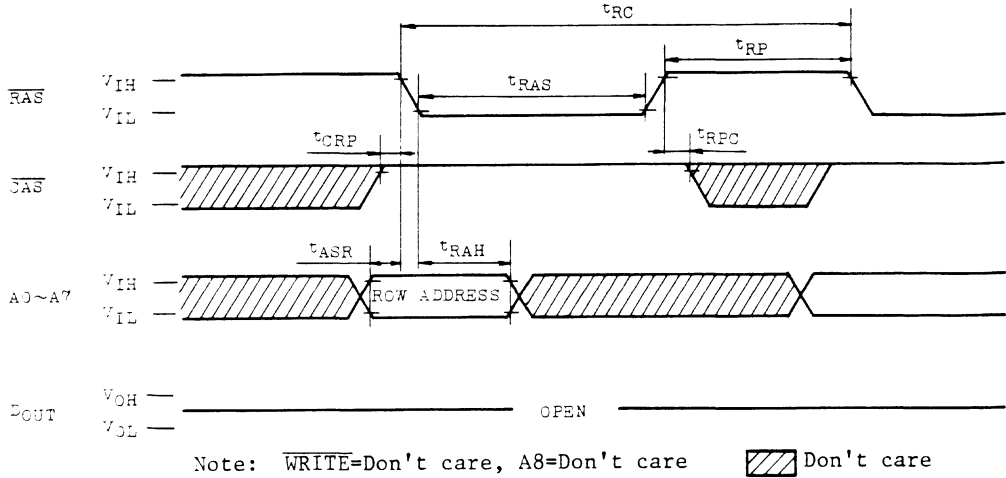
# TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

## READ-WRITE/READ-MODIFY-WRITE CYCLE

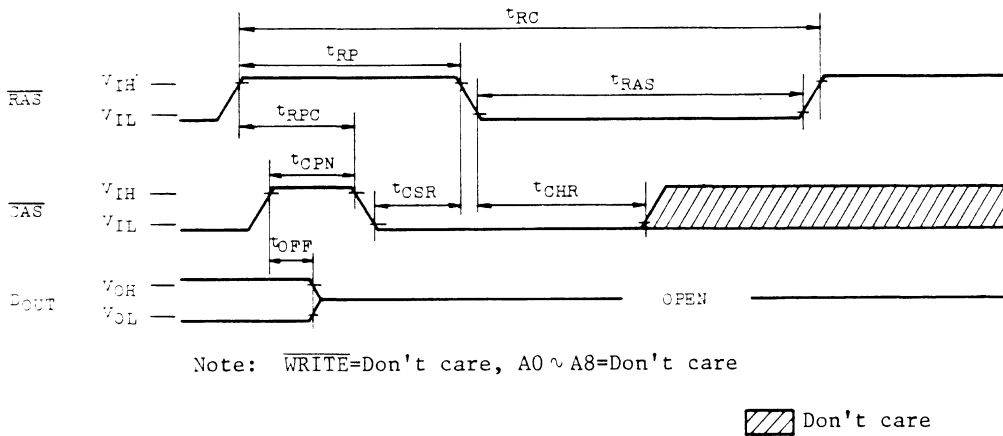


# TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

## RAS ONLY REFRESH CYCLE

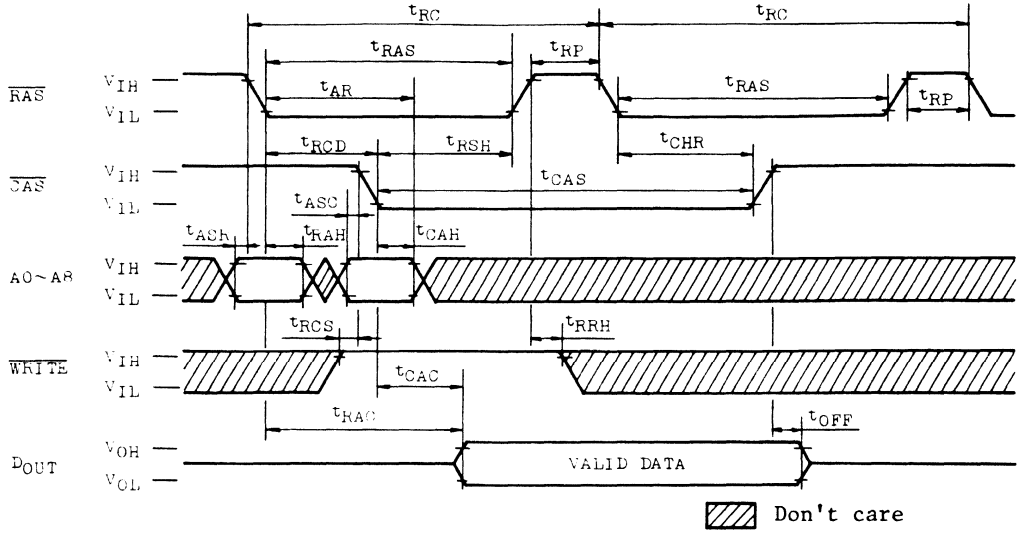


## CAS BEFORE RAS REFRESH CYCLE

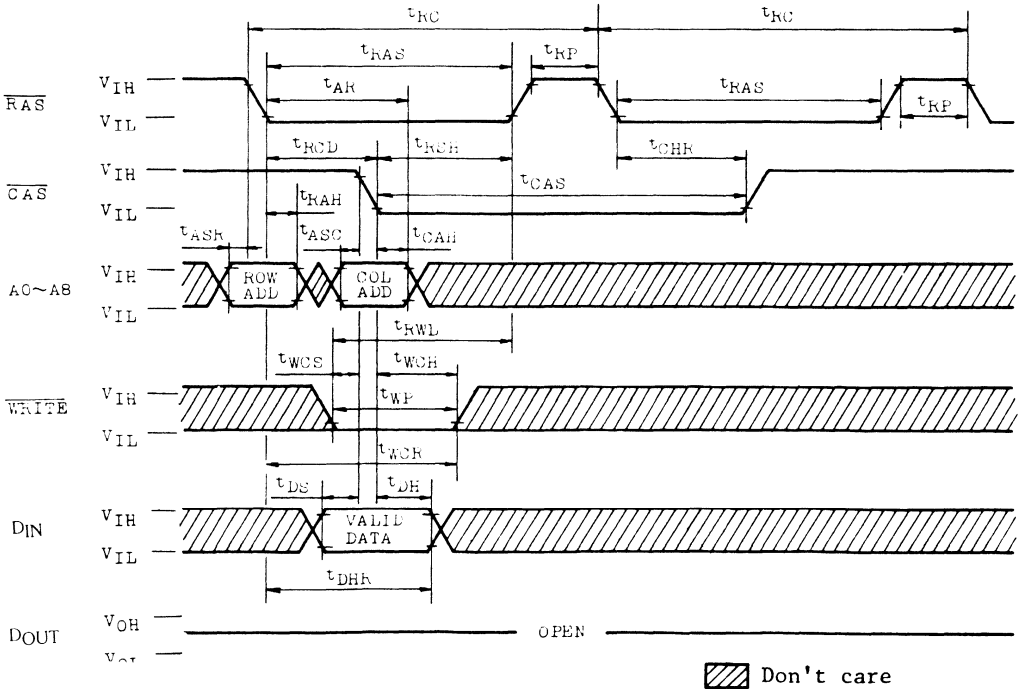


# TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

## HIDDEN REFRESH CYCLE (READ)

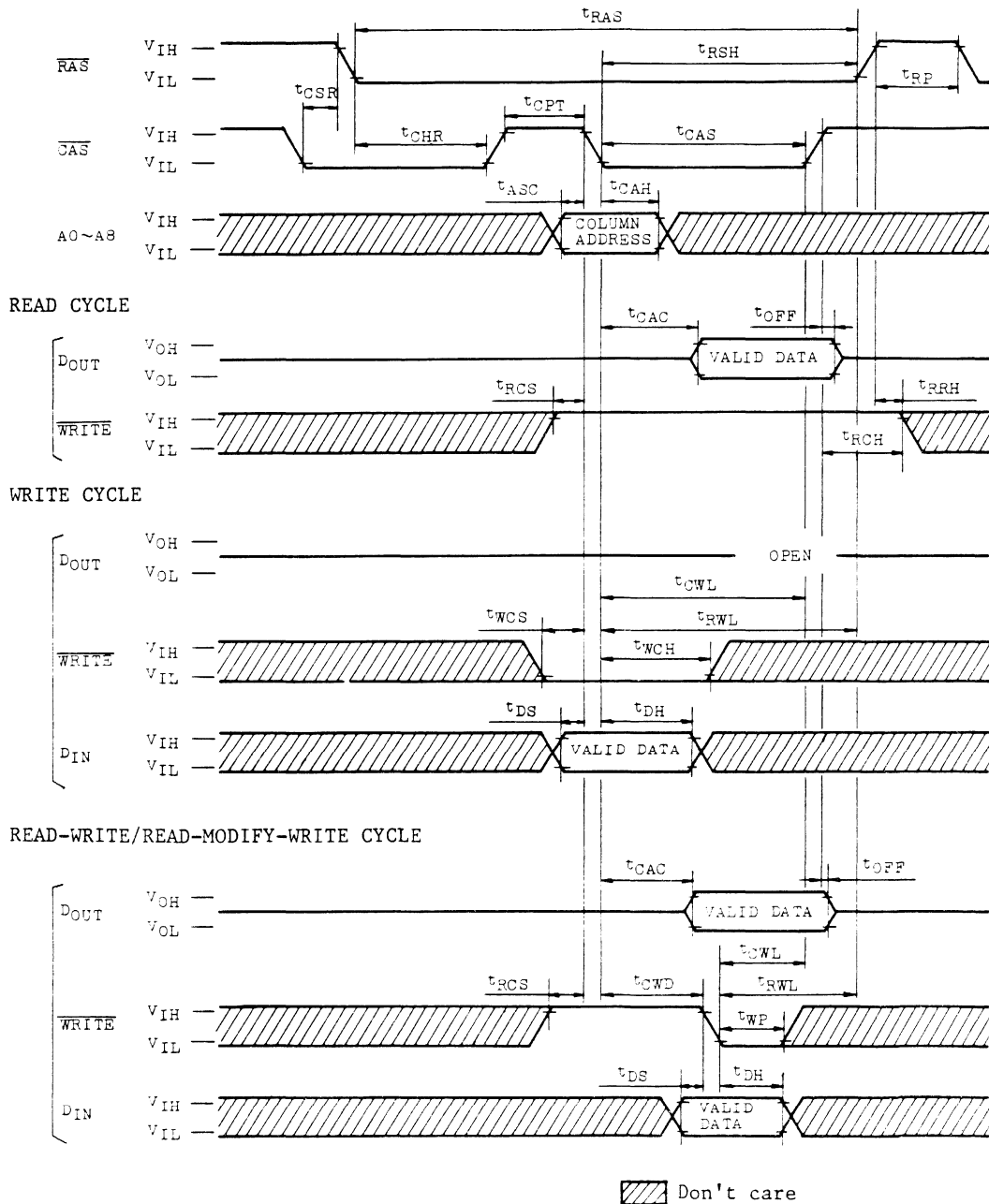


## HIDDEN REFRESH CYCLE (WRITE)



# TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

## CAS BEFORE RAS REFRESH CYCLE TEST CYCLE



# TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

## APPLICATION INFORMATION

### ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TMM41256AP/AT/AZ are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ( $\overline{RAS}$ ), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe ( $\overline{CAS}$ ), subsequently latches the 9 column address bits into the chip. Each of these signals,  $\overline{RAS}$ , and  $\overline{CAS}$ , triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the  $\overline{CAS}$  clock sequence are inhibited until the occurrence of a delayed signal derived from the  $\overline{RAS}$  clock chain. This "gated  $\overline{CAS}$ " feature allows the  $\overline{CAS}$  clock to be externally activated as soon as the Row address Hold Time specification ( $t_{RAH}$ ) has been satisfied and the address inputs have been changed from Row address to Column address information.

### DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of  $\overline{WRITE}$  and  $\overline{CAS}$  while  $\overline{RAS}$  is active. The later of the signals ( $\overline{WRITE}$  or  $\overline{CAS}$ ) to make its negative transition is the strobe for the Data In ( $D_{IN}$ ) register. This permits several options in the write cycle timing. In a write cycle, if the  $\overline{WRITE}$  input is brought low (active) prior to  $\overline{CAS}$ , the  $D_{IN}$  is strobed by  $\overline{CAS}$  and the set-up and hold times are referenced to  $\overline{CAS}$ . If the input data is not available at  $\overline{CAS}$  time or if it is desired that the cycle be a read-write cycle, the  $\overline{WRITE}$  signal will be delayed until after  $\overline{CAS}$  has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of  $\overline{WRITE}$  rather than  $\overline{CAS}$ . (To illustrate this feature,  $D_{IN}$  is referenced to  $\overline{WRITE}$  in the timing diagrams depicting the read-write and page mode write cycles while the "early write" cycle diagram shows  $D_{IN}$  referenced to  $\overline{CAS}$ ).

Data is retrieved from the memory in a read cycle by maintaining  $\overline{WRITE}$  in the inactive or high state throughout the portion of the memory cycle in which  $\overline{CAS}$  is active (low). Data read from the selected cell will be available at the output within the specified access time.

# TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

## DATA OUTPUT CONTROL

The normal condition of the Data Output (D<sub>OUT</sub>) of the TMM41256AP/AT/AZ is the high impedance (open circuit) state. This is to say, anytime  $\overline{\text{CAS}}$  is at a high level, the D<sub>OUT</sub> pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D<sub>OUT</sub> will remain valid from access time until  $\overline{\text{CAS}}$  is taken back to the inactive (high level) condition.

## PAGE MODE

The "Page-Mode" feature of the TMM41256AP/AT/AZ allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the  $\overline{\text{RAS}}$  signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page Mode" of operation will not dissipate the power associated with the negative going edge of  $\overline{\text{RAS}}$ . Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

## RAS ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address (A0-A7) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with " $\overline{\text{RAS}}$ -only" cycles,  $\overline{\text{RAS}}$  only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I<sub>CC3</sub> specification.

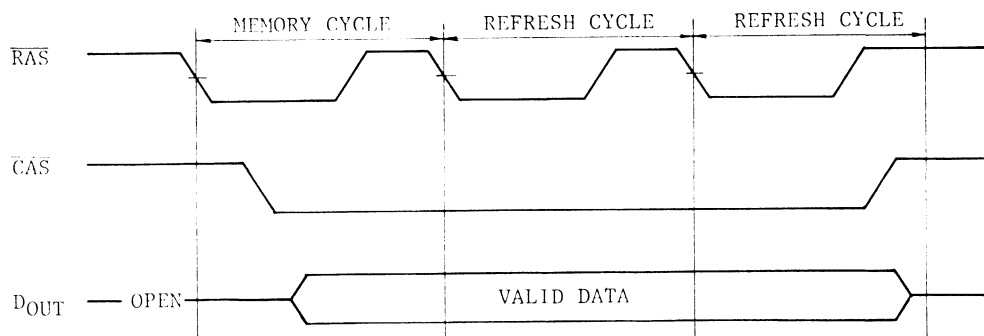
# TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

## $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH

$\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refreshing available on the TMM41256AP/AT/AZ offers an alternate refresh method. If  $\overline{\text{CAS}}$  is held on low for the specified period ( $t_{\text{CSR}}$ ) before  $\overline{\text{RAS}}$  goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh operation.

## HIDDEN REFRESH

An optional feature of the TMM41256AP/AT/AZ is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding  $\overline{\text{CAS}}$  at  $V_{\text{IL}}$  and taking  $\overline{\text{RAS}}$  high and after a specified precharge period ( $t_{\text{RP}}$ ), executing a  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

# TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

## $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TMM41256AP/AT/AZ can be tested by  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  cycles as initialization cycles. The test procedure is as follows.

- ① Write "0" into all the memory cells at normal write mode.
- ② Select one certain column address and read "0" out and write "1" in each cell by performing  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 256 times.
- ③ Check "1" out of 256 bits at normal read mode, which was written at ②.
- ④ Using the same column as ②, read "1" out and write "0" in each cell performing  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH COUNTER TEST. Repeat this operation 256 times.
- ⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.
- ⑥ Perform the above ① to ⑤ the complement data.

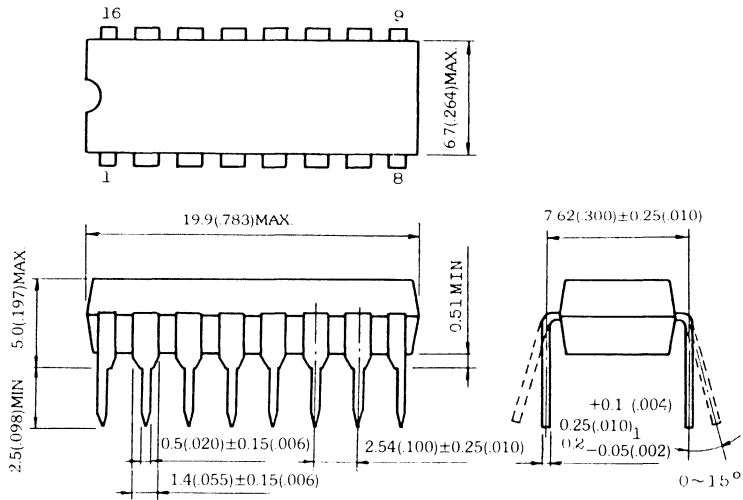


# TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

## OUTLINE DRAWINGS

- Plastic DIP

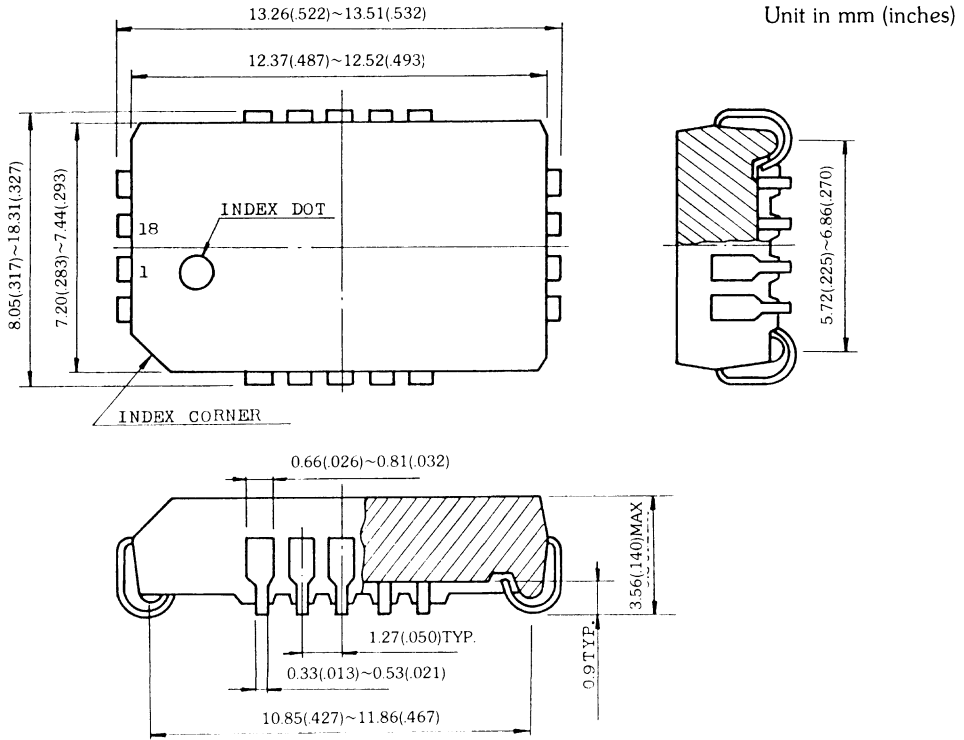
Unit in mm (inches)



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.16 leads. All dimensions are in millimeters.

# TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

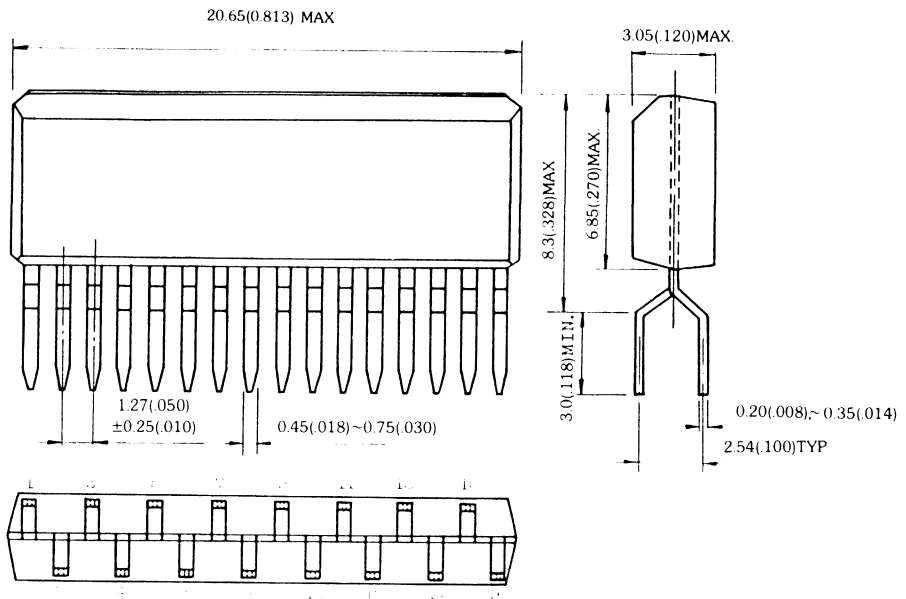
- Plastic LCC



Note: Each lead pitch is 1.27mm. All dimensions are in millimeters.

# TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15

Unit in mm (inches)



Note: Each lead pitch is 1.27mm. All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.



# TOSHIBA MOS MEMORY PRODUCT

**262,144 WORD × 1 BIT DYNAMIC RAM**  
 SILICON MONOLITHIC  
 N-CHANNEL SILICON GATE MOS

## TMM41257P/T-12 TMM41257P/T-15

### DESCRIPTION

The TMM41257P/T is the N-channel dynamic RAM organized 262,144 words by 1 bit. Multiplexed address inputs permit the TMM41257P/T to be packaged in a standard 16 pin plastic DIP and 18 pin plastic leaded chip carrier. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. The double layered MOS technology with polycide and poly Si permits the TMM41257P/T high speed operation. Also, the advanced circuit techniques have realized low power dissipation. System oriented features include single power supply of  $5V \pm 10\%$  tolerance, direct interfacing capability with high performance logic families such as schottky TTL. In addition to the  $\overline{RAS}$  only refresh mode, a  $\overline{CAS}$  before  $\overline{RAS}$  automatic refresh is available. Another special feature of TMM41257P/T is nibble mode, allowing the user to serially access 4 bits of data at a high data rate.

### FEATURES

- 262,144 words by 1 bit organization
- Fast access time and cycle time
- Low Power:
  - 385mW MAX. Operating (TMM41257P/T-12)
  - 330mW MAX. Operating (TMM41257P/T-15)
  - 28mW MAX. Standby
- Output unclashed at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write,  $\overline{CAS}$  before  $\overline{RAS}$  refresh,  $\overline{RAS}$ -only refresh, Hidden refresh, and Nibble Mode capability
- All inputs and output TTL compatible
- 256 refresh cycles/4ms
- Package
  - Plastic DIP :TMM41257P
  - Plastic Leaded Chip Carrier :TMM41257T

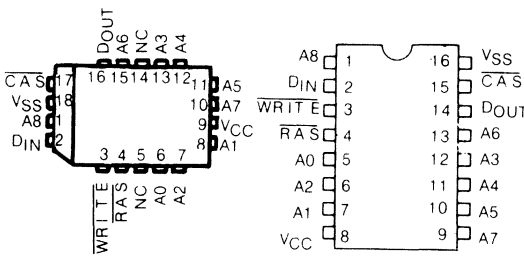
	TMM41257P/T-12	TMM41257P/T-15
RAS Access Time	120ns	150ns
CAS Access Time	60ns	75ns
Cycle Time	220ns	260ns
Nibble Mode Access Time	30ns	40ns
Nibble Mode Cycle Time	55ns	70ns

- Single power supply of  $5V \pm 10\%$  with a built-in  $V_{BB}$  generator

### PIN CONNECTION (TOP VIEW)

• Plastic LCC

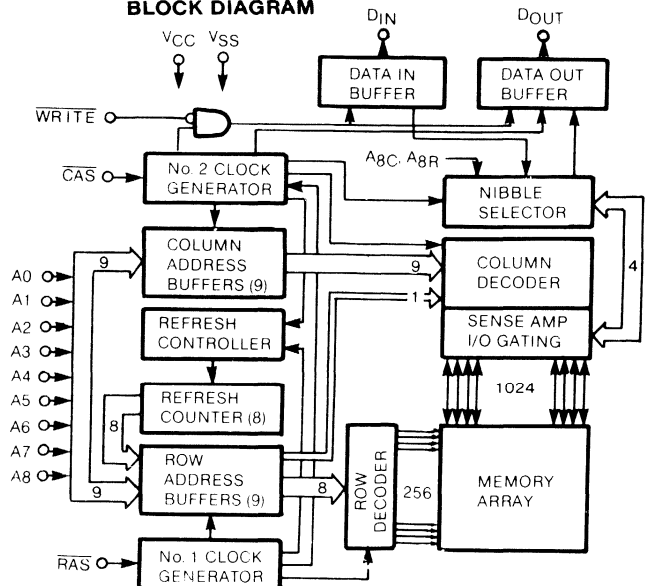
• Plastic DIP



### PIN NAMES

A0 ~ A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
$D_{IN}$	Data In
$D_{OUT}$	Data Out
$\overline{RAS}$	Row Address Strobe
WRITE	Read/Write Input
$V_{CC}$	Power (+5V)
$V_{SS}$	Ground

### BLOCK DIAGRAM



# TMM41257P/T-12

# TMM41257P/T-15

## ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	$V_{IN}, V_{OUT}$	-1~7	V	1
Power Supply Voltage	$V_{CC}$	-1~7	V	1
Operating Temperature	$T_{OPR}$	0~70	°C	1
Storage Temperature	$T_{STG}$	-55~150	°C	1
Soldering Temperature - Time	$T_{SOLDER}$	260 · 10	°C · sec	1
Power Dissipation	PD	600	mW	1
Short Circuit Output Current	$I_{OUT}$	50	mA	1

## RECOMMENDED DC OPERATING CONDITIONS ( $T_a=0\sim70^{\circ}\text{C}$ )

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
$V_{CC}$	Supply Voltage	4.5	5.0	5.5	V	2
$V_{IH}$	Input High Voltage	2.4		6.5	V	2
$V_{IL}$	Input Low Voltage	-1.0		0.8	V	2

## DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V\pm10\%$ , $T_a=0\sim70^{\circ}\text{C}$ )

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES	
$I_{CC1}$	OPERATING CURRENT Average Power Supply Operating Current ( $\overline{RAS}, \overline{CAS}$ Cycling: $t_{RC}=t_{RC}$ MIN.)	TMM41257P/T-12	-	70	mA	3,4
		TMM41257P/T-15	-	60		
$I_{CC2}$	STANDBY CURRENT Power Supply Standby Current ( $\overline{RAS}=\overline{CAS}=V_{IH}$ )	-	5	mA		
$I_{CC3}$	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ( $\overline{RAS}$ Cycling, $\overline{CAS}=V_{IH}$ ; $t_{RC}=t_{RC}$ MIN.)	TMM41257P/T-12	-	60	mA	3
		TMM41257P/T-15	-	50		
$I_{CC4}$	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ( $\overline{RAS}=V_{IL}$ , $\overline{CAS}$ Cycling: $t_{NC}=t_{NC}$ MIN.)	TMM41257P/T-12	-	40	mA	3,4
		TMM41257P/T-15	-	30		
$I_{CC5}$	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ( $\overline{RAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$ ; $t_{RC}=t_{RC}$ MIN.)	TMM41257P/T-12	-	60	mA	3
		TMM41257P/T-15	-	50		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ( $0V\leq V_{IN}\leq 6.5V$ , All Other Pins Not Under Test = 0V)	-10	10	$\mu\text{A}$		
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT ( $D_{OUT}$ is disabled, $0V\leq V_{OUT}\leq +5.5V$ )	-10	10	$\mu\text{A}$		
$V_{OH}$	OUTPUT LEVEL Output "H" Level Voltage ( $I_{OUT}=-5\text{mA}$ )	2.4		V		
$V_{OL}$	OUTPUT LEVEL Output "L" Level Voltage ( $I_{OUT}=4.2\text{mA}$ )		0.4	V		

# TMM41257P/T-12

# TMM41257P/T-15

## ELECTRIAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V<sub>CC</sub> = 5V ± 10%, T<sub>a</sub> = 0 ~ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TMM41257P/T-12		TMM41257P/T-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t <sub>RC</sub>	Random Read or Write Cycle Time	220	—	260	—	ns	
t <sub>RWC</sub>	Read-Write Cycle Time	240	—	285	—	ns	
t <sub>RMW</sub>	Read-Modify-Write Cycle Time	260	—	310	—	ns	
t <sub>RAC</sub>	Access Time from $\overline{\text{RAS}}$	—	120	—	150	ns	8, 10
t <sub>CAC</sub>	Access Time from CAS	—	60	—	75	ns	9, 10
t <sub>OFF</sub>	Output Buffer Turn Off Delay	5	30	5	35	ns	11
t <sub>I</sub>	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t <sub>RP</sub>	RAS Precharge Time	90	—	100	—	ns	
t <sub>RAS</sub>	RAS Pulse Width	120	10,000	150	10,000	ns	
t <sub>RSH</sub>	RAS Hold Time	60	—	75	—	ns	
t <sub>CSH</sub>	CAS Hold Time	120	—	150	—	ns	
t <sub>CAS</sub>	CAS Pulse Width	60	10,000	75	10,000	ns	
t <sub>RLD</sub>	RAS to CAS Delay Time	25	60	25	75	ns	13
t <sub>CHP</sub>	CAS to RAS Precharge Time	10	—	10	—	ns	
t <sub>CPN</sub>	CAS Precharge Time	20	—	25	—	ns	
t <sub>ASH</sub>	Row Address Set-Up Time	0	—	0	—	ns	
t <sub>RAH</sub>	Row Address Hold Time	15	—	15	—	ns	
t <sub>ASC</sub>	Column Address Set-Up Time	0	—	0	—	ns	
t <sub>CAH</sub>	Column Address Hold Time	25	—	30	—	ns	
t <sub>AR</sub>	Column Address Hold Time Reference to $\overline{\text{RAS}}$	85	—	105	—	ns	
t <sub>RCS</sub>	Read Command Set-Up Time	0	—	0	—	ns	
t <sub>RCH</sub>	Read Command Hold Time Reference to $\overline{\text{CAS}}$	0	—	0	—	ns	12
t <sub>RRH</sub>	Read Command Hold Time Reference to $\overline{\text{RAS}}$	15	—	20	—	ns	12
t <sub>WCH</sub>	Write Command Hold Time	25	—	30	—	ns	
t <sub>WCR</sub>	Write Command Hold Time Reference to $\overline{\text{RAS}}$	85	—	105	—	ns	
t <sub>WP</sub>	Write Command Pulse Width	25	—	30	—	ns	
t <sub>RWL</sub>	Write Command to $\overline{\text{RAS}}$ Lead Time	35	—	45	—	ns	
t <sub>CWL</sub>	Write Command to $\overline{\text{CAS}}$ Lead Time	35	—	45	—	ns	
t <sub>DS</sub>	Data-In Set-Up Time	0	—	0	—	ns	14
t <sub>DH</sub>	Data-In Hold Time	25	—	30	—	ns	14
t <sub>DHR</sub>	Data-In Hold Time Reference to $\overline{\text{RAS}}$	85	—	105	—	ns	
t <sub>RF</sub>	Refresh Period	—	4	—	4	ms	
t <sub>WCS</sub>	Write Command Set-Up Time	0	—	0	—	ns	15
t <sub>CWD</sub>	CAS to $\overline{\text{WRITE}}$ Delay	40	—	50	—	ns	15
t <sub>RWD</sub>	RAS to $\overline{\text{WRITE}}$ Delay	100	—	125	—	ns	15
t <sub>CSR</sub>	CAS Set-Up Time (CAS before RAS)	10	—	10	—	ns	
t <sub>CHR</sub>	CAS Hold Time (CAS before RAS)	30	—	30	—	ns	
t <sub>RPC</sub>	RAS Precharge to CAS Active Time	0	—	0	—	ns	
t <sub>CPT</sub>	CAS Precharge Time (CAS before RAS Counter Test)	50	—	60	—	ns	
t <sub>NC</sub>	Nibble Mode Cycle Time	55	—	70	—	ns	
t <sub>NRWC</sub>	Nibble Mode Read-Write/ Read-Modify-Write Cycle Time	85	—	105	—	ns	
t <sub>NCAC</sub>	Nibble Mode Access Time	—	30	—	40	ns	10
t <sub>NCAS</sub>	Nibble Mode Pulse Width	30	—	40	—	ns	
t <sub>NCP</sub>	Nibble Mode CAS Precharge Time	15	—	20	—	ns	
t <sub>NRSH</sub>	Nibble Mode $\overline{\text{RAS}}$ Hold Time (Read)	25	—	30	—	ns	
t <sub>NWRSH</sub>	Nibble Mode $\overline{\text{RAS}}$ Hold Time (Write)	45	—	50	—	ns	
t <sub>NCWD</sub>	Nibble Mode CAS to $\overline{\text{WRITE}}$ Delay Time	30	—	40	—	ns	
t <sub>NCWL</sub>	Nibble Mode $\overline{\text{WRITE}}$ Command to $\overline{\text{CAS}}$ Read Time	25	—	30	—	ns	

# TMM41257P/T-12

# TMM41257P/T-15

## CAPACITANCE ( $V_{CC}=5V\pm 10\%$ , $f=1\text{MHz}$ , $T_a=0\sim 70^\circ\text{C}$ )

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
C <sub>I1</sub>	Input Capacitance (A <sub>0</sub> -A <sub>8</sub> , D <sub>IN</sub> )	-	5	pF
C <sub>I2</sub>	Input Capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WRITE}}$ )	-	7	pF
C <sub>O</sub>	Output Capacitance (D <sub>OUT</sub> )	-	7	pF

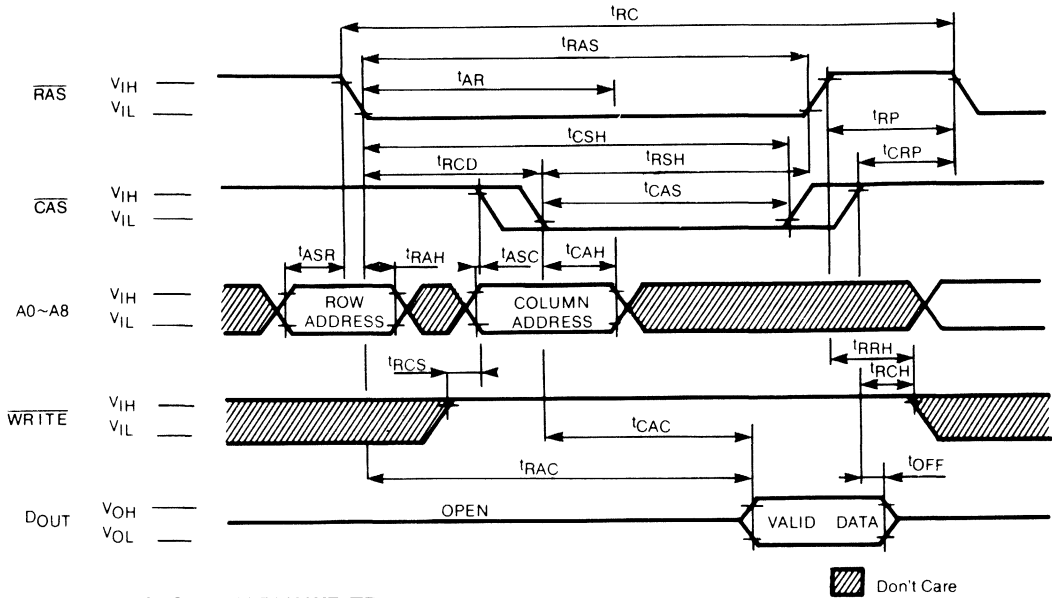
### NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V<sub>SS</sub>.
3. I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub>, I<sub>CC5</sub> depend on cycle rate.
4. i<sub>CC1</sub>, I<sub>CC4</sub> depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200 $\mu$ s is required after power-up followed by any 8  $\overline{\text{RAS}}$  cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{\text{CAS}}$  Before  $\overline{\text{RAS}}$  initialization cycles instead of 8  $\overline{\text{RAS}}$  cycles are required.
6. AC measurements assume  $t_T=5\text{ns}$ .
7. V<sub>IH</sub>(min.) and V<sub>IL</sub>(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V<sub>IH</sub> and V<sub>IL</sub>.
8. Assumes that  $t_{\text{RCD}}\leq t_{\text{RCD}}(\text{max.})$ . If  $t_{\text{RCD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{RAC}}$  will increase by the amount that  $t_{\text{RCD}}$  exceeds the value shown.
9. Assumes that  $t_{\text{RCD}}\geq t_{\text{RCD}}(\text{max.})$ .
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t<sub>OFF</sub>(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either t<sub>RCH</sub> or t<sub>RRH</sub> must be satisfied for a read cycle.
13. Operation within the t<sub>RCD</sub>(max.) limit insures that t<sub>RAC</sub>(max.) can be met. t<sub>RCD</sub>(max.) is specified as a reference point only: If t<sub>RCD</sub> is greater than the specified t<sub>RCD</sub>(max.) limit, then access time is controlled exclusively by t<sub>CAC</sub>.
14. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early write cycles and to  $\overline{\text{WRITE}}$  leading edge in read-write or read-modify-write cycles.
15. t<sub>WCS</sub>, t<sub>CWD</sub> and t<sub>RWD</sub> are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{\text{WCS}}\geq t_{\text{WCS}}(\text{min.})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If  $t_{\text{CWD}}\geq t_{\text{CWD}}(\text{min.})$  and  $t_{\text{RWD}}\geq t_{\text{RWD}}(\text{min.})$ , the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

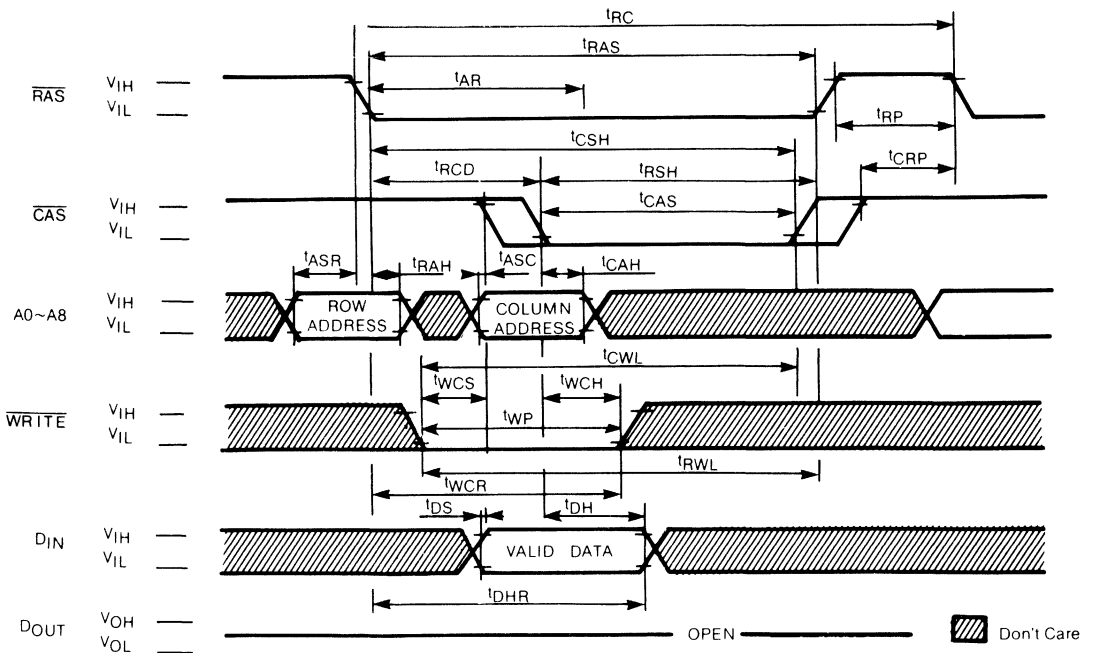


**TIMING WAVEFORMS**

● **READ CYCLE**



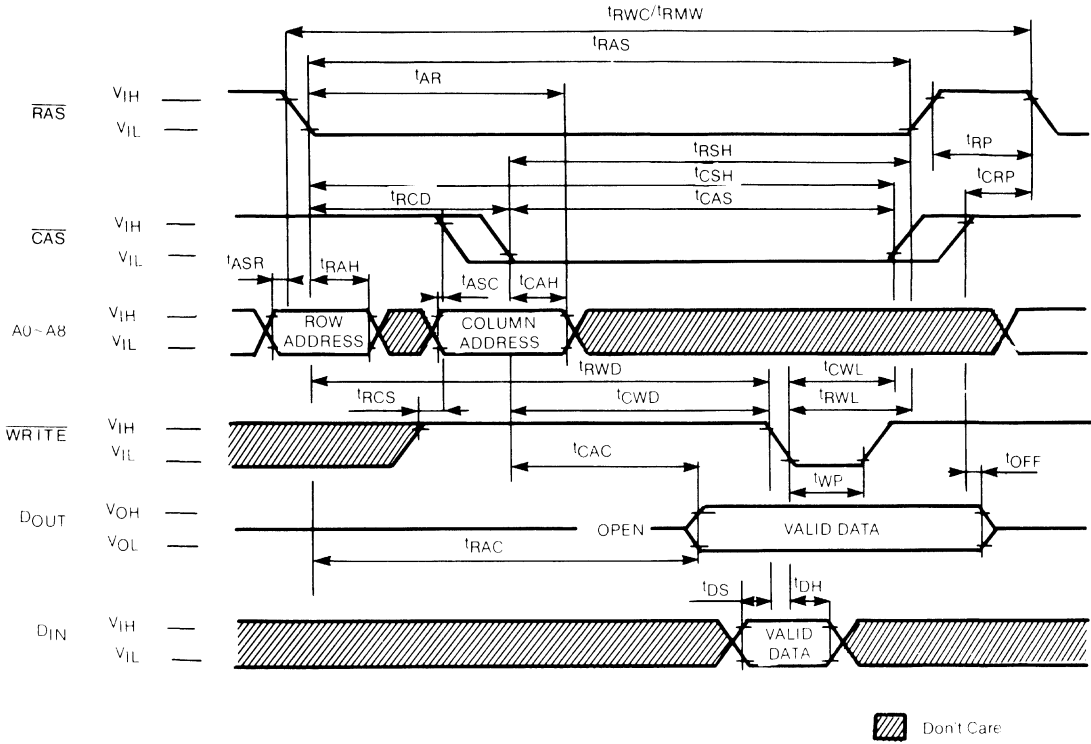
● **WRITE CYCLE (EARLY WRITE)**



# TMM41257P/T-12

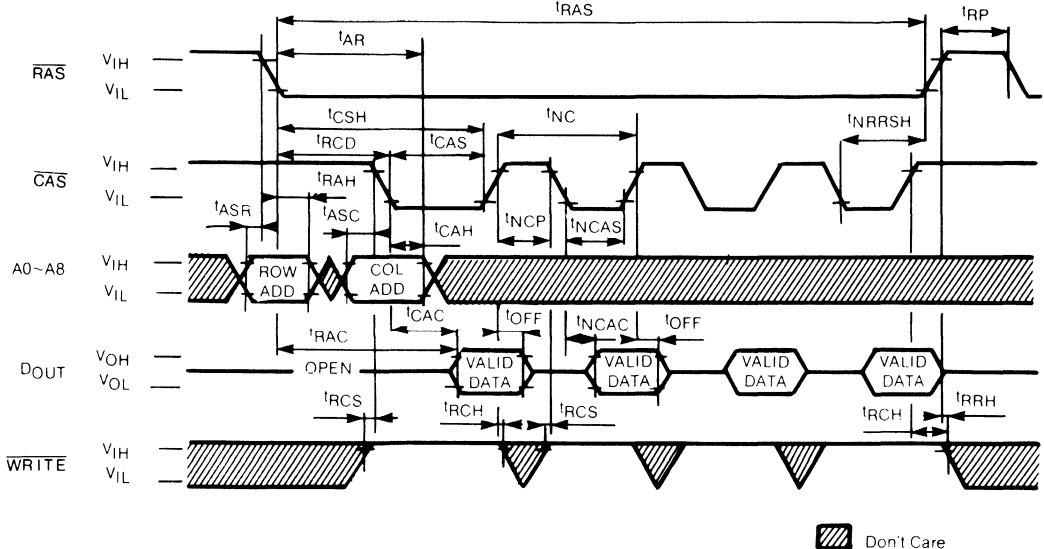
# TMM41257P/T-15

## • READ-WRITE/READ-MODIFY-WRITE CYCLE

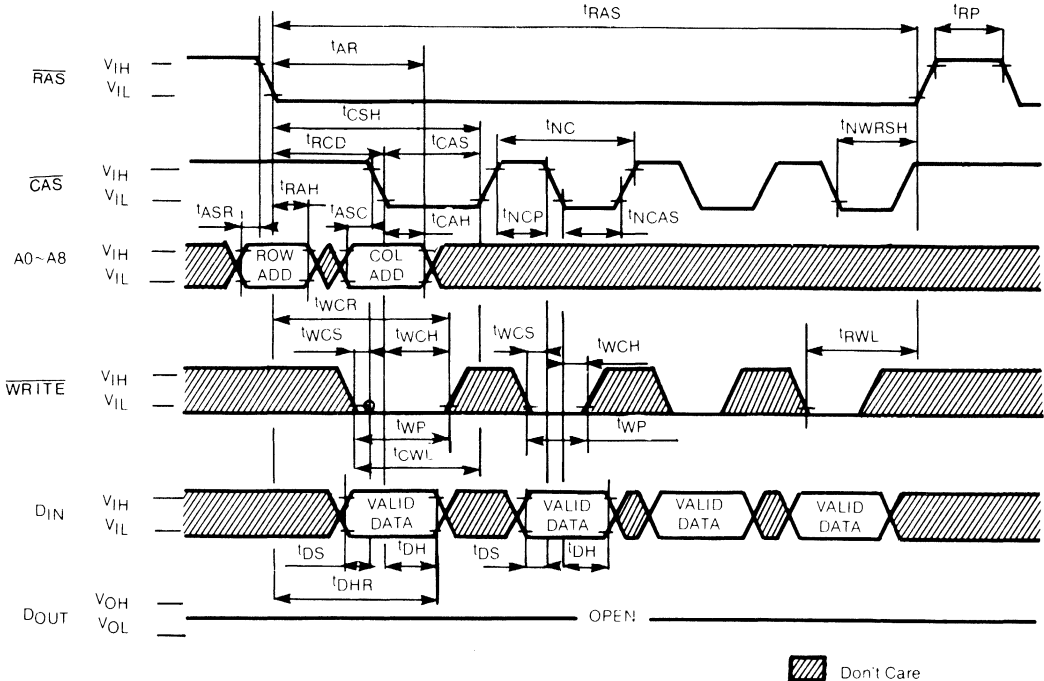


**TMM41257P/T-12**  
**TMM41257P/T-15**

● **NIBBLE MODE READ CYCLE**



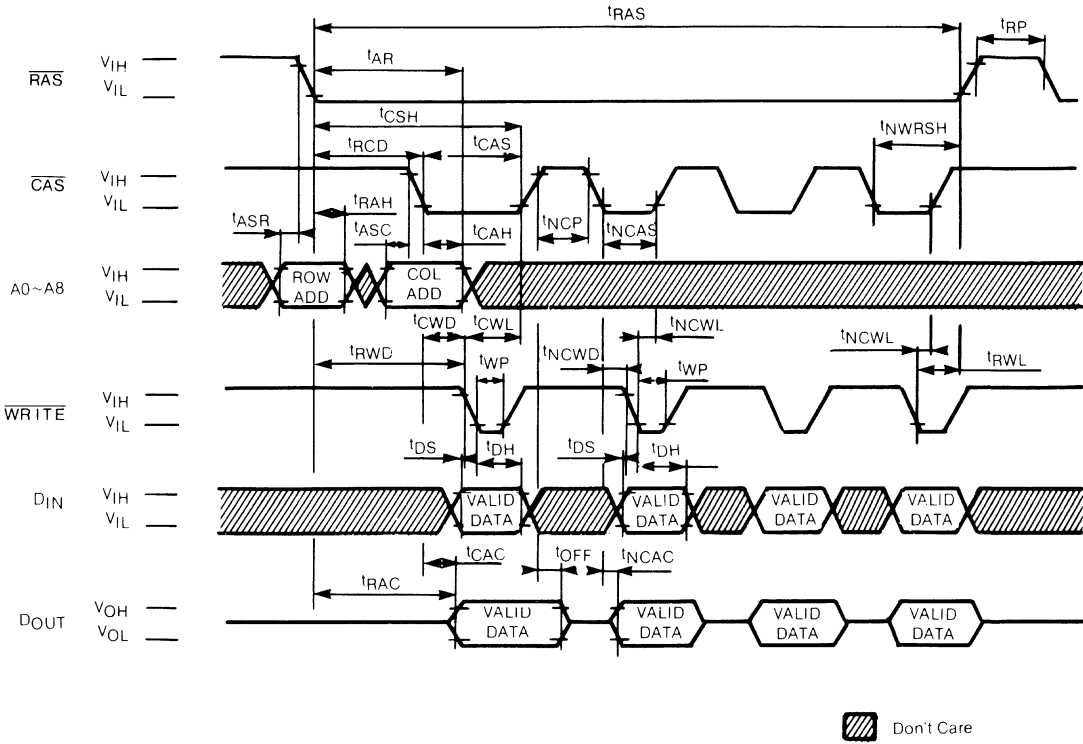
● **NIBBLE MODE WRITE CYCLE**



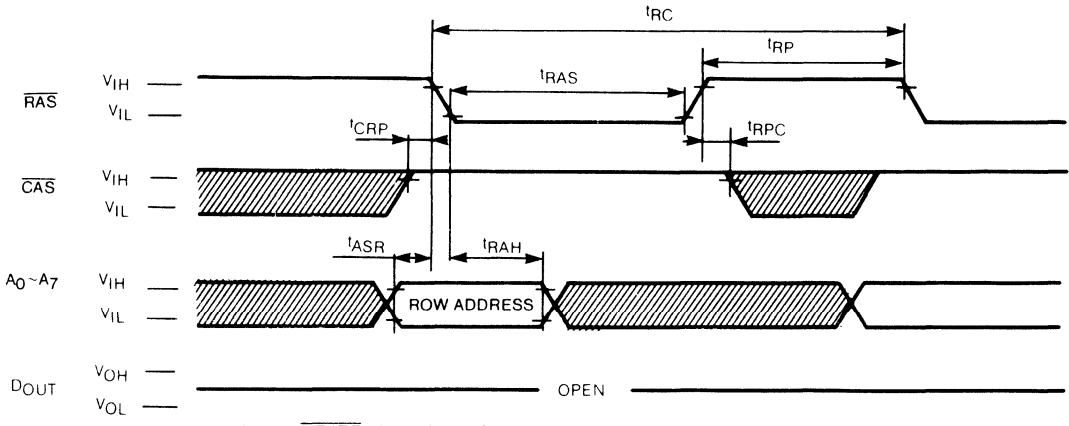
# TMM41257P/T-12

# TMM41257P/T-15

## ● NIBBLE MODE READ-WRITE/READ-MODIFY-WRITE CYCLE



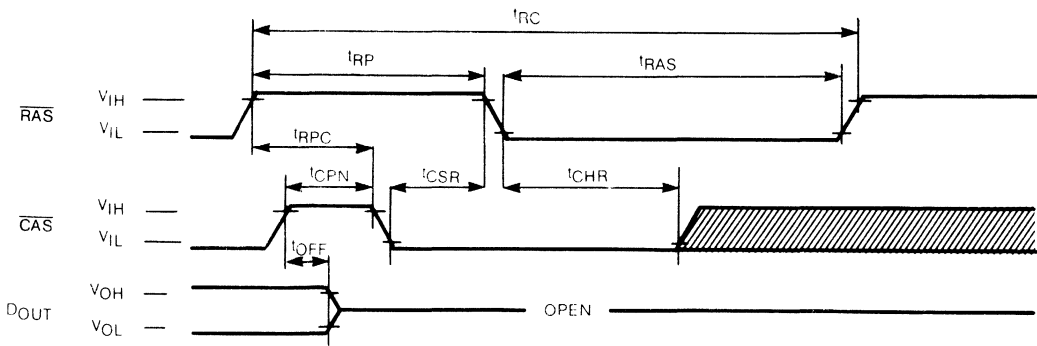
●  **$\overline{\text{RAS}}$  ONLY REFRESH CYCLE**



Note:  $\overline{\text{WRITE}}$  = Don't Care, A8 = Don't Care

Don't Care

● **CAS BEFORE RAS CYCLE**



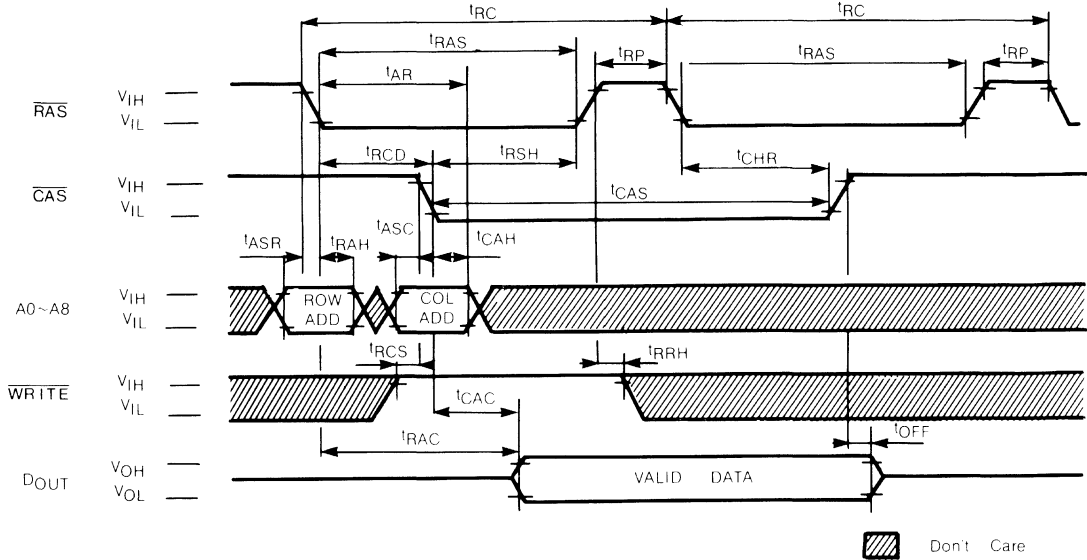
Note:  $\overline{\text{WRITE}}$  = Don't Care, A0~A8 = Don't Care

Don't Care

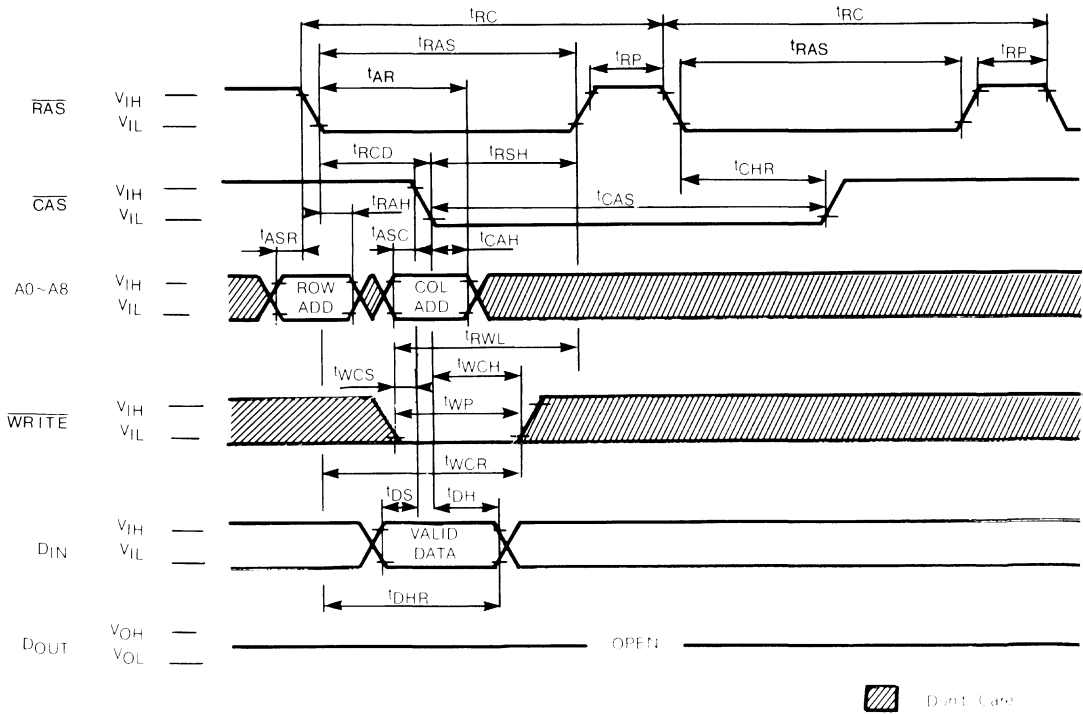
# TMM41257P/T-12

# TMM41257P/T-15

## ● HIDDEN REFRESH CYCLE (READ)

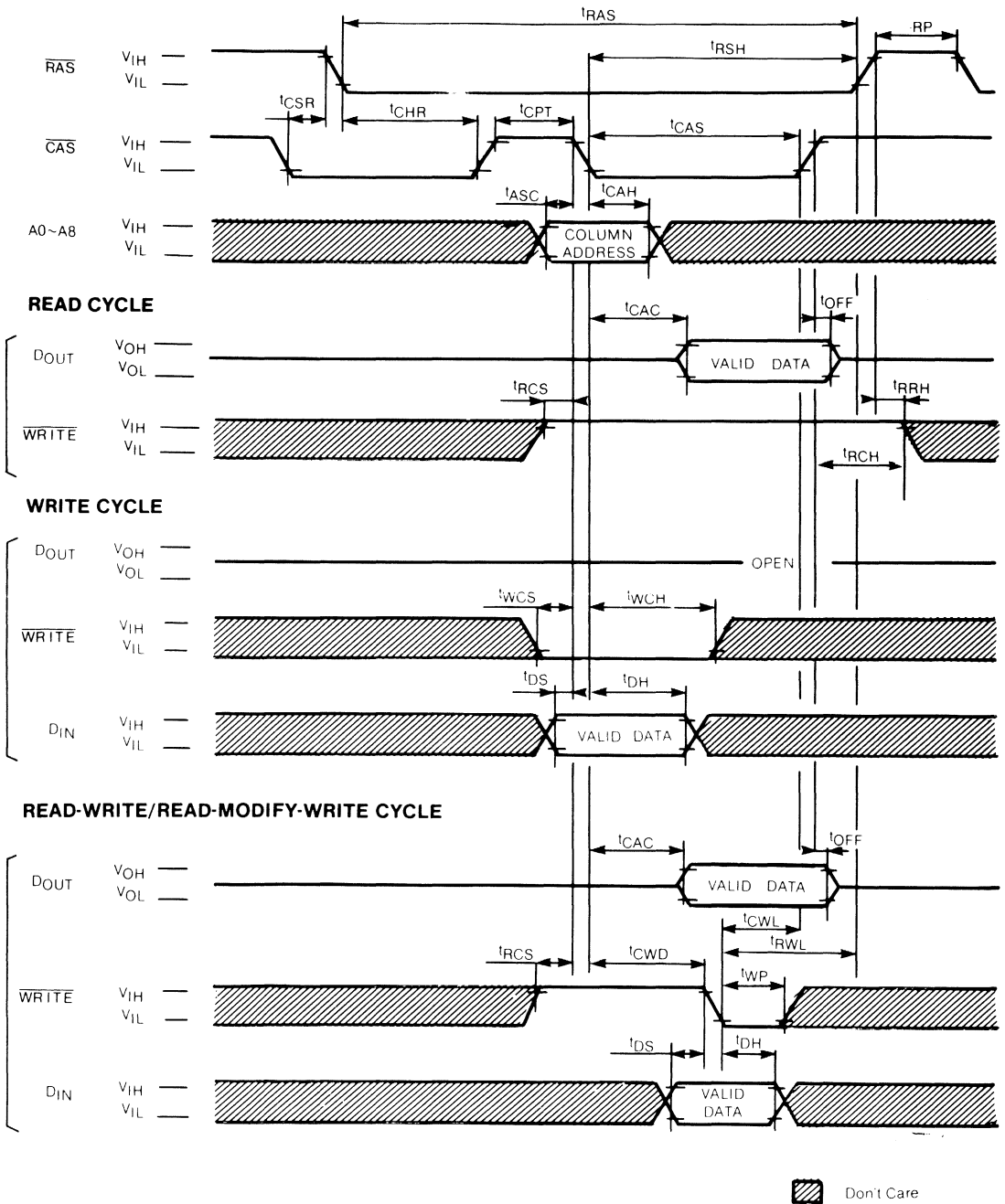


## ● HIDDEN REFRESH CYCLE (WRITE)



# TMM41257P/T-12 TMM41257P/T-15

## • CAS BEFORE RAS REFRESH CYCLE TEST CYCLE



# TMM41257P/T-12

# TMM41257P/T-15

## APPLICATION INFORMATION

### ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TMM41257P/T are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ( $\overline{RAS}$ ), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe ( $\overline{CAS}$ ), subsequently latches the 9 column address bits into the chip. Each of these signals,  $\overline{RAS}$ , and  $\overline{CAS}$ , triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the  $\overline{CAS}$  clock sequence are inhibited until the occurrence of a delayed signal derived from the  $\overline{RAS}$  clock chain. This "gated  $\overline{CAS}$ " feature allows the  $\overline{CAS}$  clock to be externally activated as soon as the Row address Hold Time specification ( $t_{RAH}$ ) has been satisfied and the address inputs have been changed from Row address to Column address information.

### DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of  $\overline{WRITE}$  and  $\overline{CAS}$  while  $\overline{RAS}$  is active. The later of the signals ( $\overline{WRITE}$  or  $\overline{CAS}$ ) to make its negative transition is the strobe for the Data In ( $D_{IN}$ ) register. This permits several options in the write cycle timing. In a write cycle, if the  $\overline{WRITE}$  input is brought low (active) prior to  $\overline{CAS}$ , the  $D_{IN}$  is strobed by  $\overline{CAS}$  and the set-up and hold times are referenced to  $\overline{CAS}$ . If the input data is not available at  $\overline{CAS}$  time or if it is desired that the cycle be a read-write cycle, the  $\overline{WRITE}$  signal will be delayed until after  $\overline{CAS}$  has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of  $\overline{WRITE}$  rather than  $\overline{CAS}$ . (To illustrate this feature,  $D_{IN}$  is referenced to  $\overline{WRITE}$  in the timing diagrams depicting the read-write and nibble mode write cycles while the "early write" cycle diagram shows  $D_{IN}$  referenced to  $\overline{CAS}$ ).

Data is retrieved from the memory in a read cycle by maintaining  $\overline{WRITE}$  in the inactive or high state throughout the portion of the memory cycle in which  $\overline{CAS}$  is active (low). Data read from the selected cell will be available at the output within the specified access time.



# TMM41257P/T-12

# TMM41257P/T-15

## DATA OUTPUT CONTROL

The normal condition of the Data Output (DOUT) of the TMM41257P/T is the high impedance (open circuit) state. This is to say, anytime  $\overline{\text{CAS}}$  is at a high level, the DOUT pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. DOUT will remain valid from access time until  $\overline{\text{CAS}}$  is taken back to the inactive (high level) condition.

## NIBBLE MODE

Nibble mode operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at  $t_{\text{CAC}}$  time. By keeping  $\overline{\text{RAS}}$  low,  $\overline{\text{CAS}}$  can be cycled up and then down, to read or write the next three pages at a high data rate (faster than  $t_{\text{CAC}}$ ). Row and column addresses need only be supplied for the first access of the cycles. From then on, the falling edge of  $\overline{\text{CAS}}$  will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Pin one (A<sub>g</sub>) determines the starting point of the circular 4 bits nibble. Row A<sub>g</sub> and column A<sub>g</sub> provide the two binary bits needed to select one of four bits. From then on, successive bits come out in a binary fashion; 00 → 01 → 10 → 11 with A<sub>g</sub> row being the least significant address.

A nibble cycle can be a read, write, or late write cycle. Any combinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as  $\overline{\text{RAS}}$  is kept low.

## $\overline{\text{RAS}}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address (A<sub>0</sub>~A<sub>7</sub>) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with " $\overline{\text{RAS}}$ -only" cycles.  $\overline{\text{RAS}}$  only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the ICC3 specification.

# TMM41257P/T-12

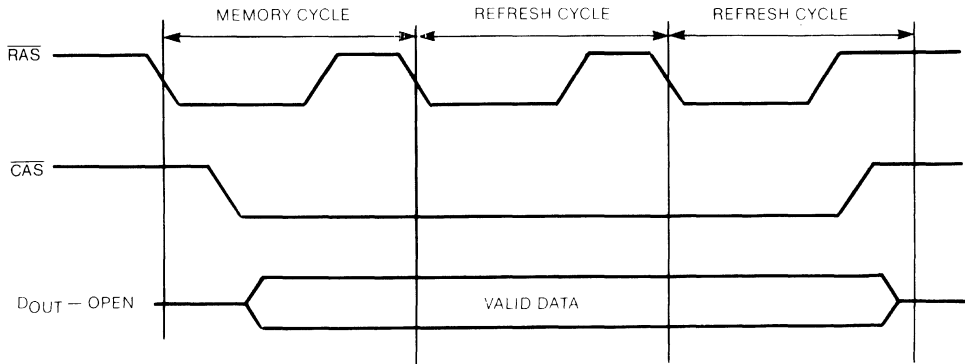
# TMM41257P/T-15

## $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH

$\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refreshing available on the TMM41257P/T offers an alternate refresh method. If  $\overline{\text{CAS}}$  is held on low for the specified period ( $t_{\text{CSR}}$ ) before  $\overline{\text{RAS}}$  goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh operation.

## HIDDEN REFRESH

An optional feature of the TMM41257P/T is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding  $\overline{\text{CAS}}$  at  $V_{\text{IL}}$  and taking  $\overline{\text{RAS}}$  high and after a specified precharge period ( $t_{\text{RP}}$ ), executing a  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

### **$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST**

The internal refresh operation of TMM41257P/T can be tested by  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  cycles as initialization cycles. The test procedure is as follows.

- (1) Write "0" into all the memory cells at normal write mode.
- (2) Select one certain column address and read "0" out and write "1" in each cell by performing  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 256 times.
- (3) Check "1" out of 256 bits at normal read mode, which was written at (2).
- (4) Using the same column as (2), read "1" out and write "0" in each cell performing  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH COUNTER TEST. Repeat this operation 256 times.
- (5) Check "0" out of 256 bits at normal read mode, which was written at (4).
- (6) Perform the above (1) to (5) with the complement data.

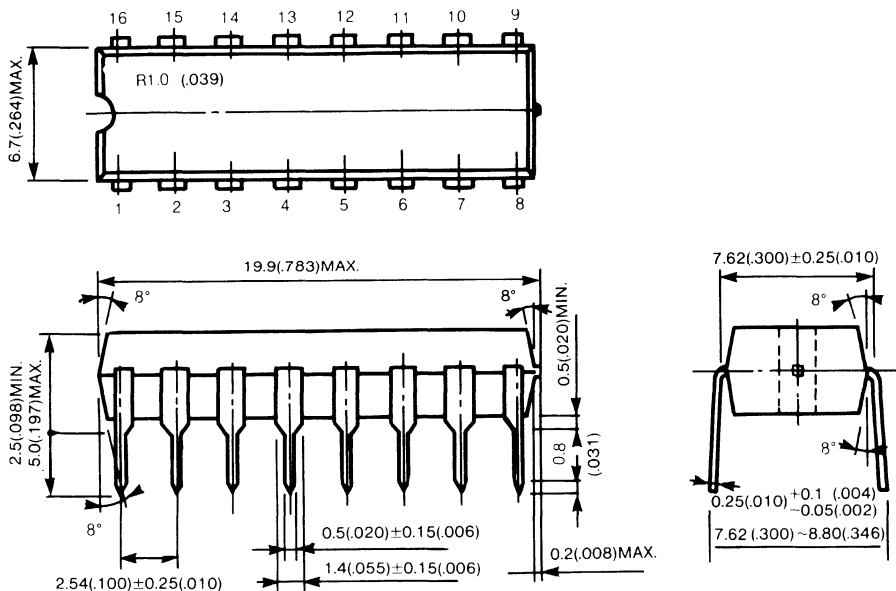
# TMM41257P/T-12

# TMM41257P/T-15

## OUTLINE DRAWINGS

- Plastic Dip

Unit in mm (inches)



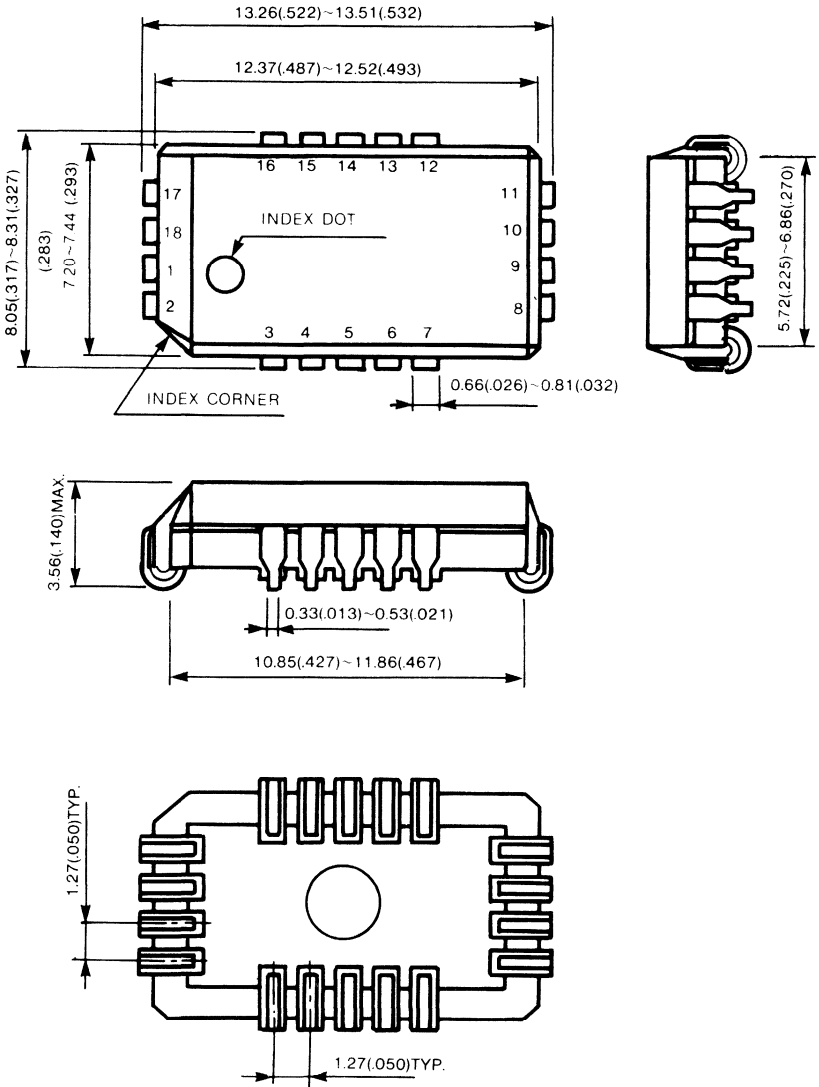
Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.16 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

**TMM41257P/T-12**  
**TMM41257P/T-15**

● Plastic LCC

Unit in mm (inches)





# TOSHIBA MOS MEMORY PRODUCT

**262,144 WORD × 1 BIT DYNAMIC RAM TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12**  
 SILICON MONOLITHIC  
 N-CHANNEL SILICON GATE CMOS **TMM41257AP/AT/AZ-15**

\*This is advanced information and specifications are subject to change without notice.

## DESCRIPTION

The TMM41257AP/AT/AZ is an N-channel dynamic RAM organized 262,144 words by 1 bit. Multiplexed address inputs permit the TMM41257AP/AT/AZ to be packaged in a standard 16 pin plastic DIP, 18 pin PLCC and 16 pin ZIP. The package size allows for high system bit densities and is compatible with widely available automated testing and insertion equipment. The double layered MOS technology with polycide and poly Si permits the TMM41257AP/AT/AZ high speed operation. Also, the advanced circuit techniques have achieved low power dissipation. System oriented features include single power supply of  $5V \pm 10\%$  tolerance, direct interfacing capability with high performance logic families such as schottky TTL. In addition to the  $\overline{\text{RAS}}$  only refresh mode, a  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  automatic refresh is available. Another special feature of the TMM41257AP/AT/AZ is nibble mode which allows the user to serially access 4 bits of data at a high data rate.

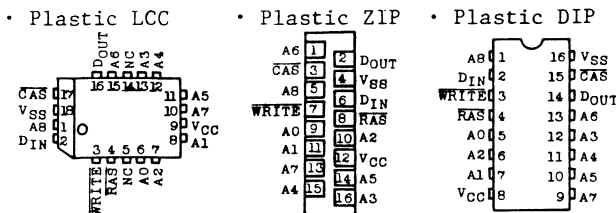
## FEATURES

- 262,144 words by 1 bit organization
- Fast access time and cycle time
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write,  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh,  $\overline{\text{RAS}}$ -only refresh, Hidden refresh, and Nibble Mode capability
- All inputs and output TTL compatible
- 256 refresh cycles/4ms
- Package
  - Plastic DIP : TMM41257AP
  - Plastic Leaded
  - Chip Carrier : TMM41257AT
  - Plastic ZIP : TMM41257AZ

	TMM41257AP/AT/AZ-10/-12/-15
RAS Access Time	100ns/120ns/150ns
CAS Access Time	50ns/ 60ns/ 75ns
Cycle Time	190ns/220ns/260ns
Nibble Mode Access Time	25ns/ 30ns/ 40ns
Nibble Mode Cycle Time	50ns/ 60ns/ 70ns

- Single power supply of  $5V \pm 10\%$  with a built-in  $V_{\text{BB}}$  generator
- Low Power:
  - 440mW MAX. Operating (TMM41257AP/AT/AZ-10)
  - 396mW MAX. Operating (TMM41257AP/AT/AZ-12)
  - 358mW MAX. Operating (TMM41257AP/AT/AZ-15)
  - 28mW MAX. Standby

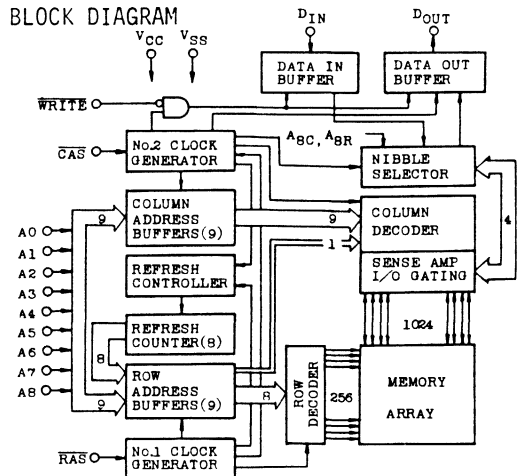
## PIN CONNECTION (TOP VIEW)



## PIN NAMES

A0 ~ A8	Address Inputs
$\overline{\text{CAS}}$	Column Address Strobe
DIN	Data In
DOUT	Data Out
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{WRITE}}$	Read/Write Input
VCC	Power (+5V)
VSS	Ground

## BLOCK DIAGRAM



# TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12 TMM41257AP/AT/AZ-15

## ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	$V_{IN}, V_{OUT}$	-1 ~ 7	V	1
Power Supply Voltage	$V_{CC}$	-1 ~ 7	V	1
Operating Temperature	$T_{OPR}$	0 ~ 70	°C	1
Storage Temperature	$T_{STG}$	-55 ~ 150	°C	1
Soldering Temperature • Time	$T_{SOLDER}$	260 • 10	°C • sec	1
Power Dissipation	$P_D$	600	mW	1
Short Circuit Output Current	$I_{OUT}$	50	mA	1

## RECOMMENDED DC OPERATING CONDITIONS ( $T_a=0 \sim 70^\circ\text{C}$ )

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
$V_{CC}$	Supply Voltage	4.5	5.0	5.5	V	2
$V_{IH}$	Input High Voltage	2.4	-	6.5	V	2
$V_{IL}$	Input Low Voltage	-1.0	-	0.8	V	2

## DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ , $T_a=0 \sim 70^\circ\text{C}$ )

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES	
$I_{CC1}$	OPERATING CURRENT Average Power Supply Operating Current ( $\overline{RAS}$ , $\overline{CAS}$ Cycling: $t_{RC}=t_{RC \text{ MIN.}}$ )	TMM41257AP/AT/AZ-10	-	80	mA	3, 4
		TMM41257AP/AT/AZ-12	-	72		
		TMM41257AP/AT/AZ-15	-	65		
$I_{CC2}$	STANDBY CURRENT Power Supply Standby Current ( $\overline{RAS}=\overline{CAS}=V_{IH}$ )	-	5	mA		
$I_{CC3}$	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Refresh Mode ( $\overline{RAS}$ Cycling, $\overline{CAS}=V_{IH}$ : $t_{RC}=t_{RC \text{ MIN.}}$ )	TMM41257AP/AT/AZ-10	-	70	mA	3
		TMM41257AP/AT/AZ-12	-	62		
		TMM41257AP/AT/AZ-15	-	55		
$I_{CC4}$	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ( $\overline{RAS}=V_{IL}$ , $\overline{CAS}$ Cycling: $t_{NC}=t_{NC \text{ MIN.}}$ )	TMM41257AP/AT/AZ-10	-	50	mA	3, 4
		TMM41257AP/AT/AZ-12	-	45		
		TMM41257AP/AT/AZ-15	-	40		
$I_{CC5}$	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Mode ( $\overline{RAS}$ , $\overline{CAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$ : $t_{RC}=t_{RC \text{ MIN.}}$ )	TMM41257AP/AT/AZ-10	-	70	mA	3
		TMM41257AP/AT/AZ-12	-	62		
		TMM41257AP/AT/AZ-15	-	55		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ( $0V \leq V_{IN} \leq 6.5V$ , All Other Pins Not Under Test = 0V)	-10	10	$\mu\text{A}$		
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT ( $D_{OUT}$ is disabled, $0V \leq V_{OUT} \leq +5.5V$ )	-10	10	$\mu\text{A}$		
$V_{OH}$	OUTPUT LEVEL Output "H" Level Voltage ( $I_{OUT} = -5\text{mA}$ )	2.4	-	V		
$V_{OL}$	OUTPUT LEVEL Output "L" Level Voltage ( $I_{OUT} = 4.2\text{mA}$ )	-	0.4	V		



# TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12 TMM41257AP/AT/AZ-15

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V<sub>CC</sub>=5V±10%, Ta=0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TMM41257AP/ AT/AZ-10		TMM41257AP/ AT/AZ-12		TMM41257AP/ AT/AZ-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t <sub>RC</sub>	Random Read or Write Cycle Time	190	-	220	-	260	-	ns	
t <sub>RWC</sub>	Read-Write Cycle Time	200	-	240	-	285	-	ns	
t <sub>RNW</sub>	Read-Modify-Write Cycle Time	220	-	260	-	310	-	ns	
t <sub>NC</sub>	Nibble Mode Cycle Time	50	-	60	-	70	-	ns	
t <sub>NRWC</sub>	Nibble Mode Read-Write / Read-Modify-Write Cycle Time	75	-	90	-	105	-	ns	
t <sub>RAC</sub>	Access Time from $\overline{\text{RAS}}$	-	100	-	120	-	150	ns	8,10
t <sub>CAC</sub>	Access Time from $\overline{\text{CAS}}$	-	50	-	60	-	75	ns	9,10
t <sub>NCAC</sub>	Nibble Mode Access Time	-	25	-	30	-	40	ns	10
t <sub>OFF</sub>	Output Buffer Turn-Off Delay	5	25	5	30	5	35	ns	11
t <sub>T</sub>	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t <sub>RP</sub>	$\overline{\text{RAS}}$ Precharge Time	80	-	90	-	100	-	ns	
t <sub>RAS</sub>	$\overline{\text{RAS}}$ Pulse Width	100	10,000	120	10,000	150	10,000	ns	
t <sub>RSH</sub>	$\overline{\text{RAS}}$ Hold Time	50	-	60	-	75	-	ns	
t <sub>CSH</sub>	$\overline{\text{CAS}}$ Hold Time	100	-	120	-	150	-	ns	
t <sub>CAS</sub>	$\overline{\text{CAS}}$ Pulse Width	50	10,000	60	10,000	75	10,000	ns	
t <sub>RCD</sub>	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	25	50	25	60	25	75	ns	13
t <sub>CRP</sub>	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	10	-	10	-	10	-	ns	
t <sub>CPN</sub>	$\overline{\text{CAS}}$ Precharge Time	15	-	20	-	25	-	ns	
t <sub>ASR</sub>	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t <sub>RAH</sub>	Row Address Hold Time	15	-	15	-	15	-	ns	
t <sub>ASC</sub>	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t <sub>CAH</sub>	Column Address Hold Time	20	-	25	-	30	-	ns	
t <sub>AR</sub>	Column Address Hold Time Reference to $\overline{\text{RAS}}$	70	-	85	-	105	-	ns	
t <sub>RCS</sub>	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t <sub>RCH</sub>	Read Command Hold Time Reference to $\overline{\text{CAS}}$	0	-	0	-	0	-	ns	12
t <sub>RRH</sub>	Read Command Hold Time Reference to $\overline{\text{RAS}}$	10	-	15	-	20	-	ns	12
t <sub>WCH</sub>	Write Command Hold Time	20	-	25	-	30	-	ns	
t <sub>WCR</sub>	Write Command Hold Time Reference to $\overline{\text{RAS}}$	70	-	85	-	105	-	ns	
t <sub>WP</sub>	Write Command Pulse Width	20	-	25	-	30	-	ns	
t <sub>RWL</sub>	Write Command to $\overline{\text{RAS}}$ Lead Time	25	-	35	-	45	-	ns	
t <sub>CWL</sub>	Write Command to $\overline{\text{CAS}}$ Lead Time	25	-	35	-	45	-	ns	

# TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12 TMM41257AP/AT/AZ-15

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TMM41527AP/ AT/AZ-10		TMM41527AP/ AT/AZ-12		TMM41527AP/ AT/AZ-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t <sub>DS</sub>	Data-In Set-Up Time	0	-	0	-	0	-	ns	14
t <sub>DH</sub>	Data-In Hold Time	20	-	25	-	30	-	ns	14
t <sub>DHR</sub>	Data-In Hold Time Reference to $\overline{\text{RAS}}$	70	-	85	-	105	-	ns	
t <sub>REF</sub>	Refresh Period	-	4	-	4	-	4	ms	
t <sub>WCS</sub>	Write Command Set-Up Time	0	-	0	-	0	-	ns	15
t <sub>CWD</sub>	$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ Delay Time	30	-	40	-	50	-	ns	15
t <sub>RWd</sub>	$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ Delay Time	80	-	100	-	125	-	ns	15
t <sub>NCAS</sub>	Nibble Mode $\overline{\text{CAS}}$ Pulse Width	25	-	30	-	40	-	ns	
t <sub>NCP</sub>	Nibble Mode $\overline{\text{CAS}}$ Precharge Time	15	-	20	-	20	-	ns	
t <sub>NRRSH</sub>	Nibble Mode $\overline{\text{RAS}}$ Hold Time (Read)	20	-	25	-	30	-	ns	
t <sub>NWRSH</sub>	Nibble Mode $\overline{\text{RAS}}$ Hold Time (Write)	40	-	45	-	50	-	ns	
t <sub>NCWD</sub>	Nibble Mode $\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ Delay Time	25	-	30	-	40	-	ns	
t <sub>NCWL</sub>	Nibble Mode $\overline{\text{WRITE}}$ Command to $\overline{\text{CAS}}$ Lead Time	20	-	25	-	30	-	ns	
t <sub>CSR</sub>	$\overline{\text{CAS}}$ Set-Up Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	10	-	10	-	10	-	ns	
t <sub>CHR</sub>	$\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	30	-	30	-	30	-	ns	
t <sub>RPC</sub>	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	0	-	0	-	0	-	ns	
t <sub>CPT</sub>	$\overline{\text{CAS}}$ Precharge Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Counter Test)	40	-	50	-	60	-	ns	

## CAPACITANCE ( $V_{CC}=5V\pm 10\%$ , $f=1\text{MHz}$ , $T_a=0\sim 70^\circ\text{C}$ )

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
C <sub>I1</sub>	Input Capacitance ( $A_0\sim A_8$ , D <sub>IN</sub> )	-	5	pF
C <sub>I2</sub>	Input Capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WRITE}}$ )	-	7	pF
C <sub>O</sub>	Output Capacitance (D <sub>OUT</sub> )	-	7	pF

# TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12 TMM41257AP/AT/AZ-15

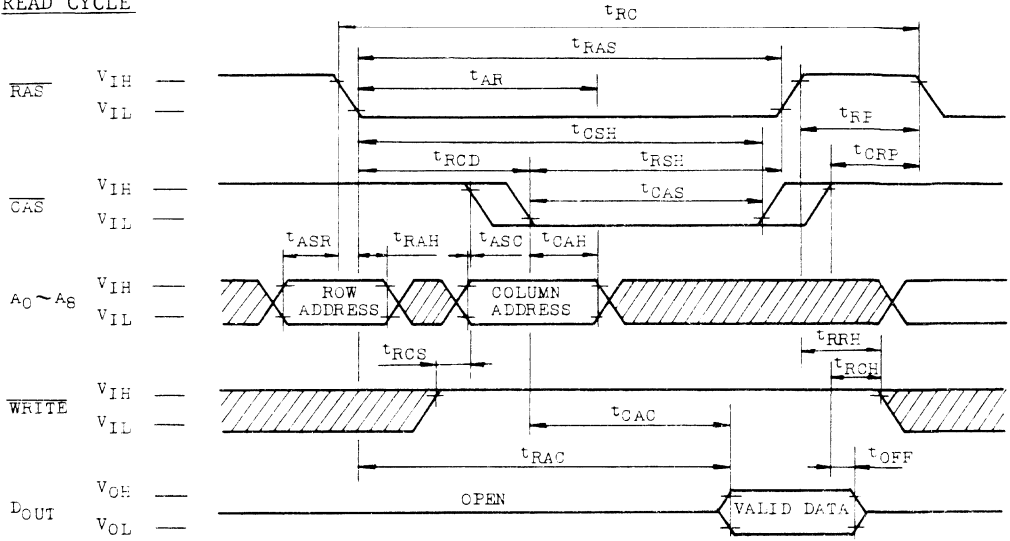
## NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to  $V_{SS}$ .
3.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ ,  $I_{CC5}$  depend on cycle rate.
4.  $I_{CC1}$ ,  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200 $\mu$ s is required after power-up followed by any 8  $\overline{RAS}$  cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS Before RAS initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
6. AC measurements assume  $t_T=5$ ns.
7.  $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
8. Assumes that  $t_{RCD} \leq t_{RCD}(\text{max.})$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds the value shown.
9. Assumes that  $t_{RCD} \geq t_{RCD}(\text{max.})$
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11.  $t_{OFF}(\text{max.})$  defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
13. Operation within the  $t_{RCD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
14. These parameters are referenced to  $\overline{CAS}$  leading edge in early write cycles and to  $\overline{WRITE}$  leading edge in read-write or read-modify-write cycles.
15.  $t_{WCS}$ ,  $t_{CWD}$  and  $t_{RWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If  $t_{CWD} \geq t_{CWD}(\text{min.})$  and  $t_{RWD} \geq t_{RWD}(\text{min.})$ , the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

# TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12 TMM41257AP/AT/AZ-15

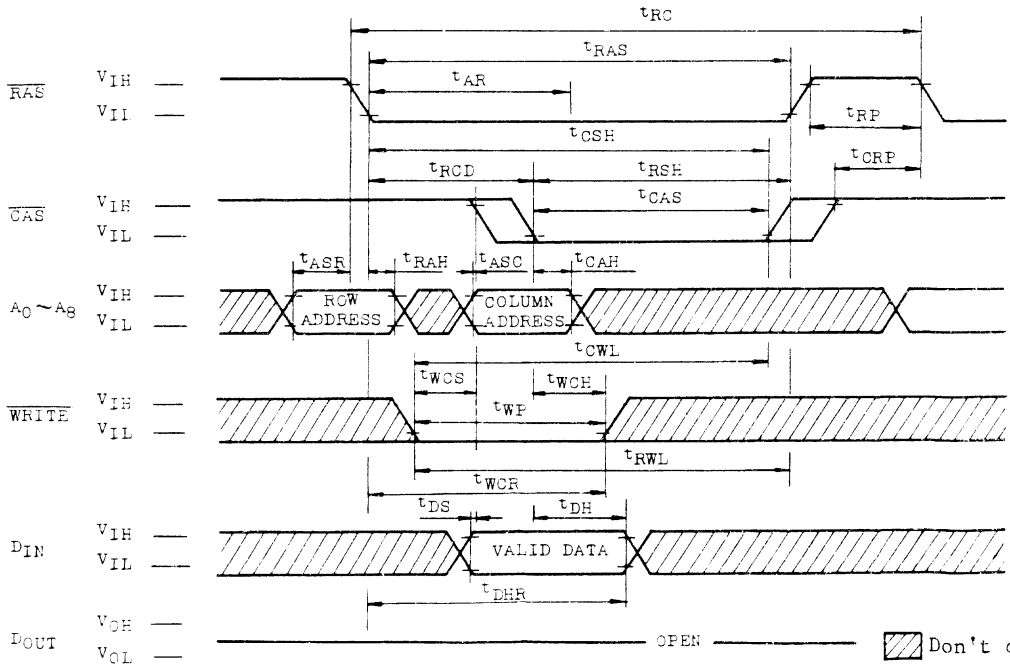
## TIMING WAVEFORMS

### READ CYCLE



Don't care

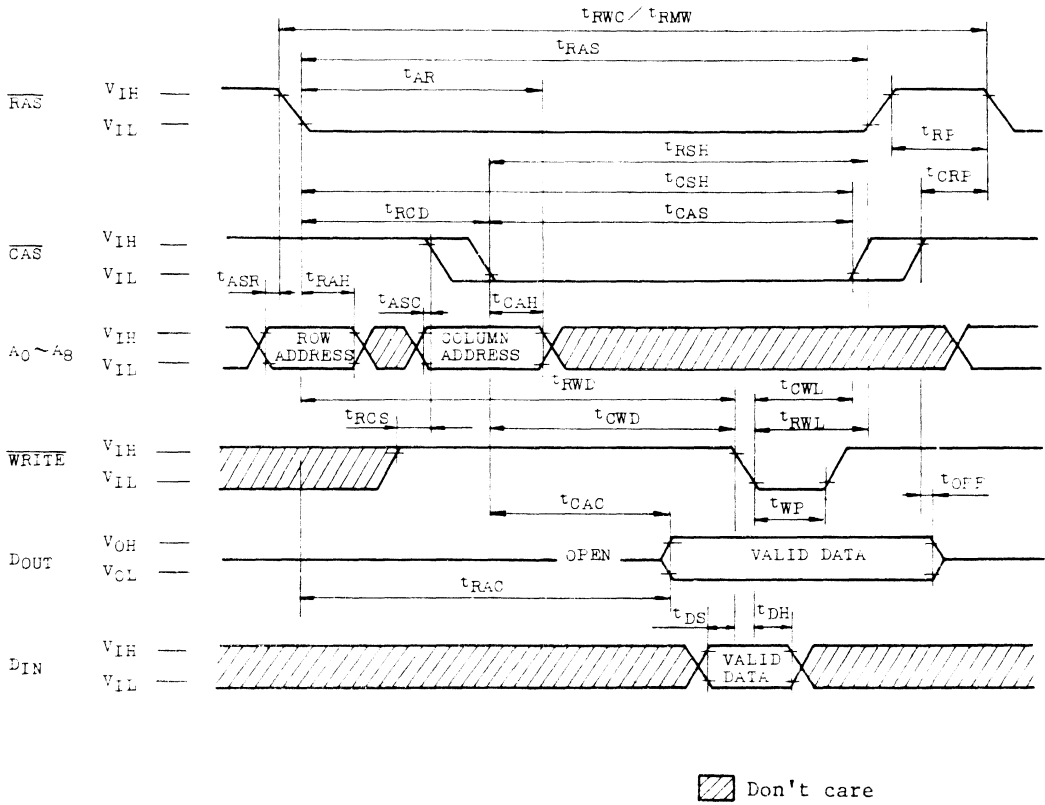
### WRITE CYCLE (EARLY WRITE)



Don't care

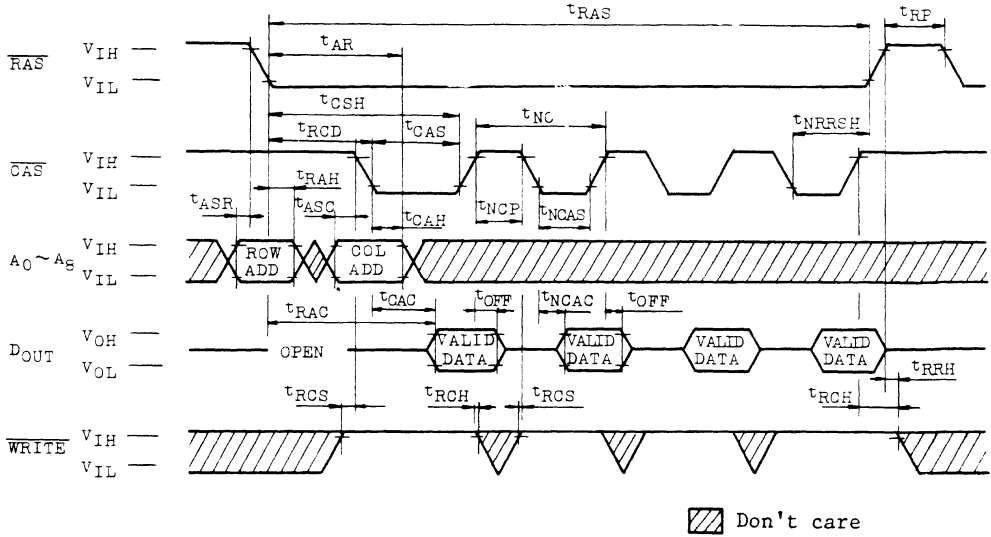
# TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12 TMM41257AP/AT/AZ-15

## READ-WRITE/READ-MODIFY-WRITE CYCLE

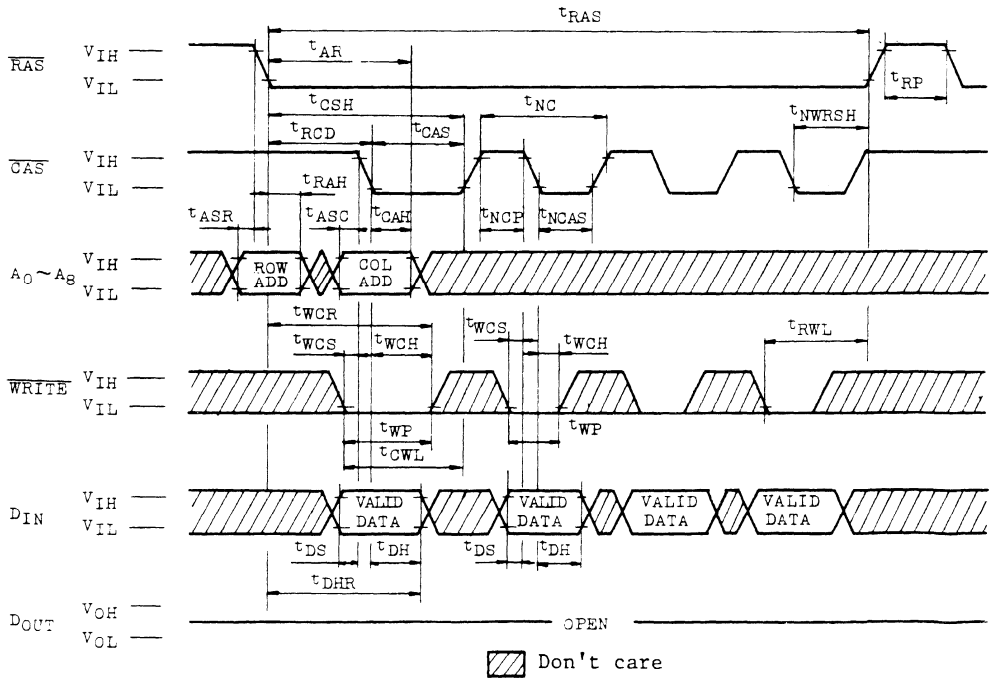


# TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12 TMM41257AP/AT/AZ-15

## NIBBLE MODE READ CYCLE

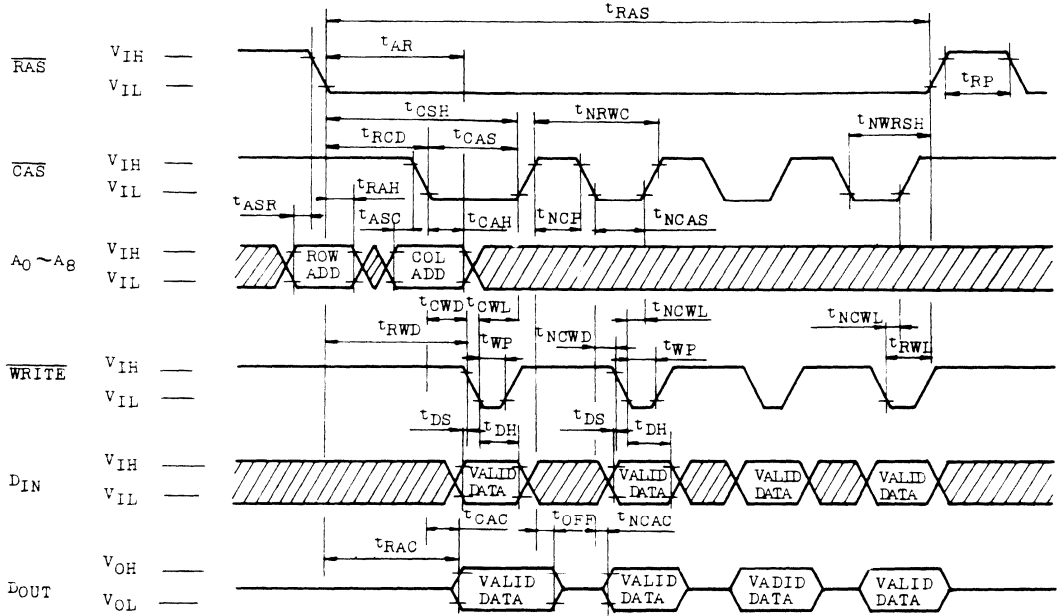



## NIBBLE MODE WRITE CYCLE (EARLY WRITE)



# TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12 TMM41257AP/AT/AZ-15

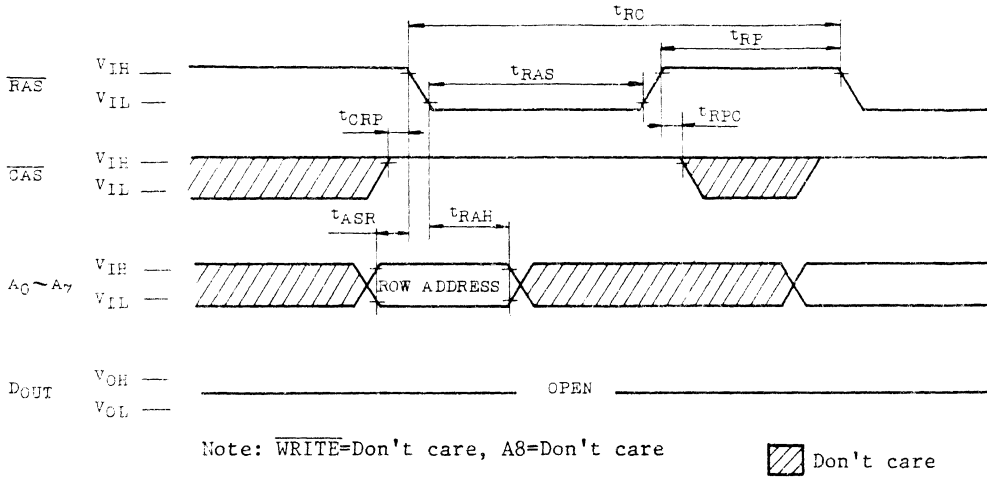
## NIBBLE MODE READ-WRITE/READ-MODIFY-WRITE CYCLE



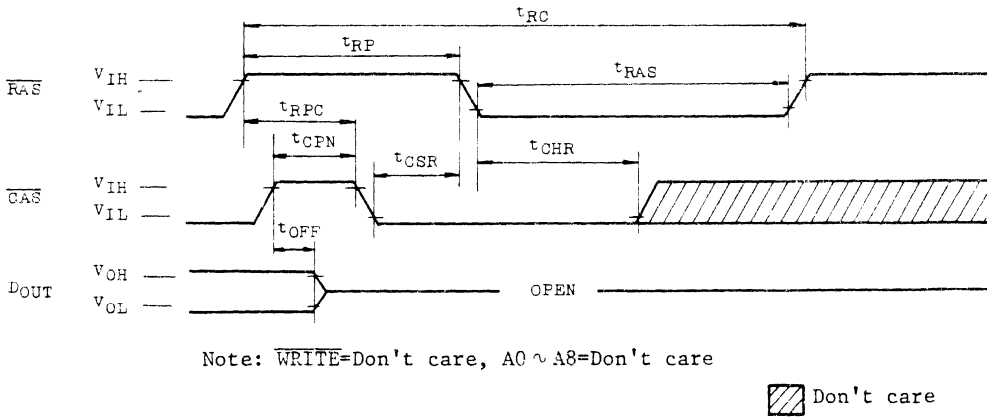
 Don't care

# TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12 TMM41257AP/AT/AZ-15

## RAS ONLY REFRESH CYCLE



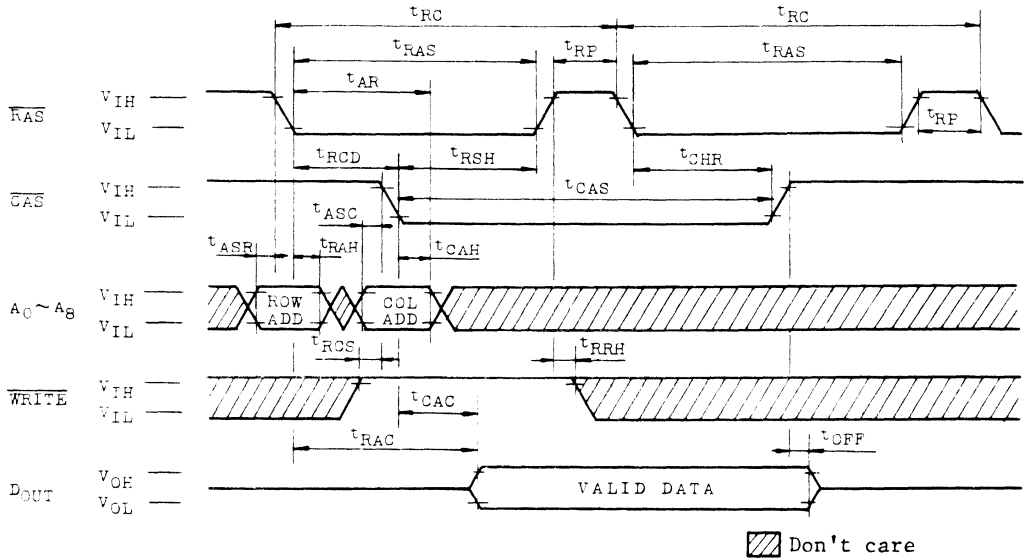
## CAS BEFORE RAS REFRESH CYCLE



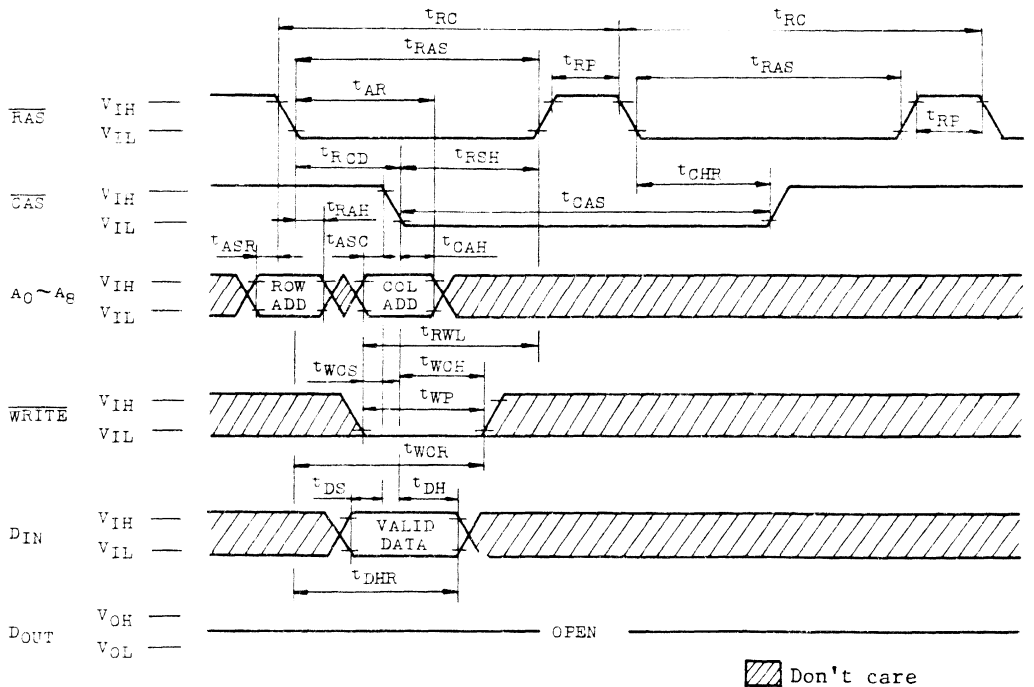


# TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12 TMM41257AP/AT/AZ-15

## HIDDEN REFRESH CYCLE (READ)

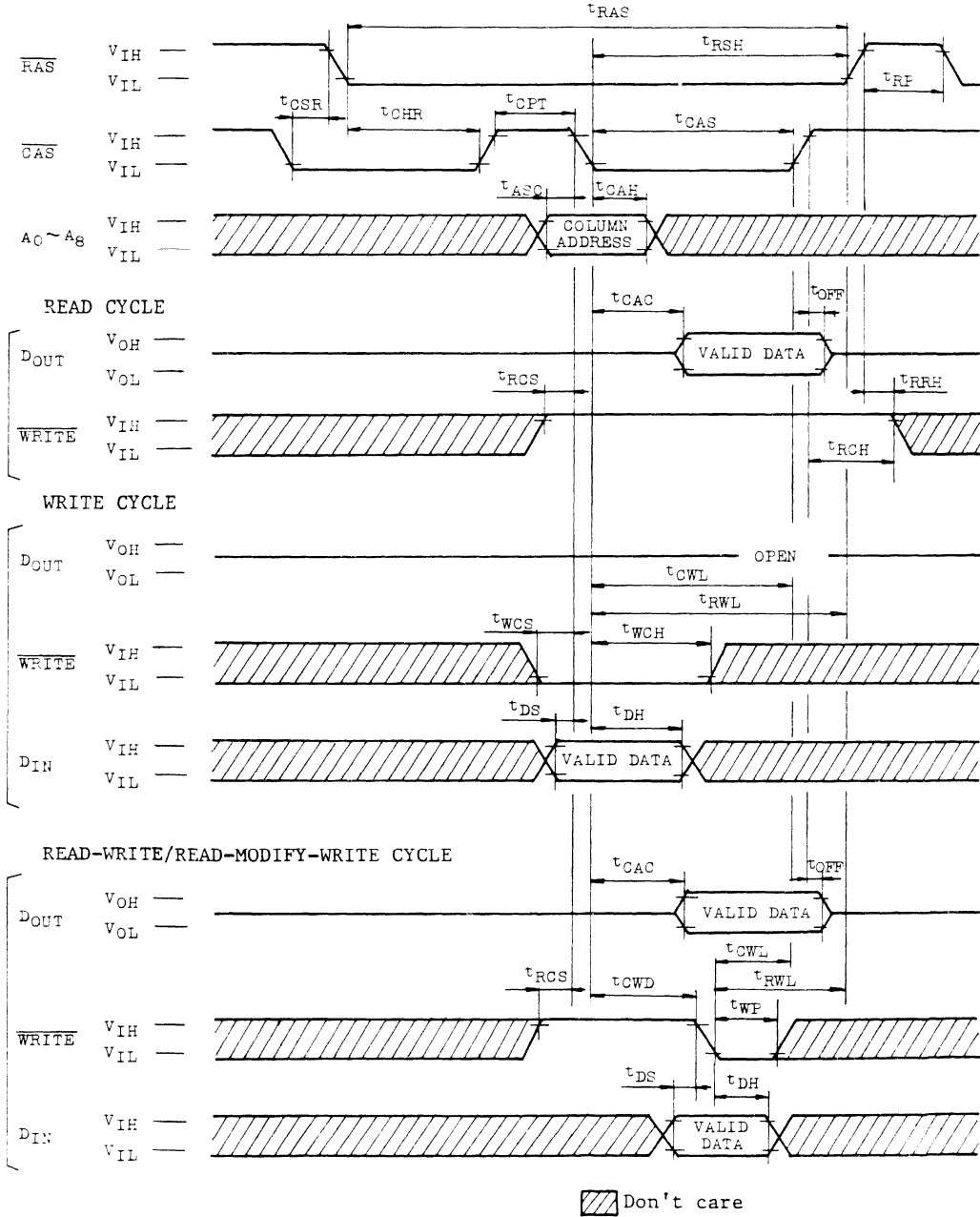


## HIDDEN REFRESH CYCLE (WRITE)



# TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12 TMM41257AP/AT/AZ-15

## CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



# TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12 TMM41257AP/AT/AZ-15

## APPLICATION INFORMATION

### ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TMM41257AP/AT/AZ are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ( $\overline{RAS}$ ), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe ( $\overline{CAS}$ ), subsequently latches the 9 column address bits into the chip. Each of these signals,  $\overline{RAS}$ , and  $\overline{CAS}$ , triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the  $\overline{CAS}$  clock sequence are inhibited until the occurrence of a delayed signal derived from the  $\overline{RAS}$  clock chain. This "gated  $\overline{CAS}$ " feature allows the  $\overline{CAS}$  clock to be externally activated as soon as the Row address Hold Time specification ( $t_{RAH}$ ) has been satisfied and the address inputs have been changed from Row address to Column address information.

### DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of  $\overline{WRITE}$  and  $\overline{CAS}$  while  $\overline{RAS}$  is active. The later of the signals ( $\overline{WRITE}$  or  $\overline{CAS}$ ) to make its negative transition is the strobe for the Data In ( $D_{IN}$ ) register. This permits several options in the write cycle timing. In a write cycle, if the  $\overline{WRITE}$  input is brought low (active) prior to  $\overline{CAS}$ , the  $D_{IN}$  is strobed by  $\overline{CAS}$  and the set-up and hold times are referenced to  $\overline{CAS}$ . If the input data is not available at  $\overline{CAS}$  time or if it is desired that the cycle be a read-write cycle, the  $\overline{WRITE}$  signal will be delayed until after  $\overline{CAS}$  has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of  $\overline{WRITE}$  rather than  $\overline{CAS}$ . (To illustrate this feature,  $D_{IN}$  is referenced to  $\overline{WRITE}$  in the timing diagrams depicting the read-write and nibble mode write cycles while the "early write" cycle diagram shows  $D_{IN}$  referenced to  $\overline{CAS}$ ).

Data is retrieved from the memory in a read cycle by maintaining  $\overline{WRITE}$  in the inactive or high state throughout the portion of the memory cycle in which  $\overline{CAS}$  is active (low). Data read from the selected cell will be available at the output within the specified access time.

# TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12 TMM41257AP/AT/AZ-15

## DATA OUTPUT CONTROL

The normal condition of the Data Output ( $D_{OUT}$ ) of the TMM41257AP/AT/AZ is the high impedance (open circuit) state. This is to say, anytime  $\overline{CAS}$  is at a high level, the  $D_{OUT}$  pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle.  $D_{OUT}$  will remain valid from access time until  $\overline{CAS}$  is taken back to the inactive (high level) condition.

## NIBBLE MODE

Nibble mode operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at  $t_{CAC}$  time. By keeping  $\overline{RAS}$  low,  $\overline{CAS}$  can be cycled up and then down, to read or write the next three pages at high data rate (faster than  $t_{CAC}$ ). Row and column addresses need only be supplied for the first access of the cycles. From then on, the falling edge of  $\overline{CAS}$  will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Pin one ( $A_8$ ) determines the starting point of the circular 4 bits nibble. Row  $A_8$  and column  $A_8$  provide the two binary bits needed to select one of four bits. From then on, successive bits come out in a binary fashion: 00 → 01 → 10 → 11 with  $A_8$  row being the least significant address.

A nibble cycle can be a read, write, or late write cycle. Any combinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as  $\overline{RAS}$  is kept low.

## $\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address ( $A_0 \sim A_7$ ) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with " $\overline{RAS}$ -only" cycles,  $\overline{RAS}$  only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the  $I_{CC3}$  specification.

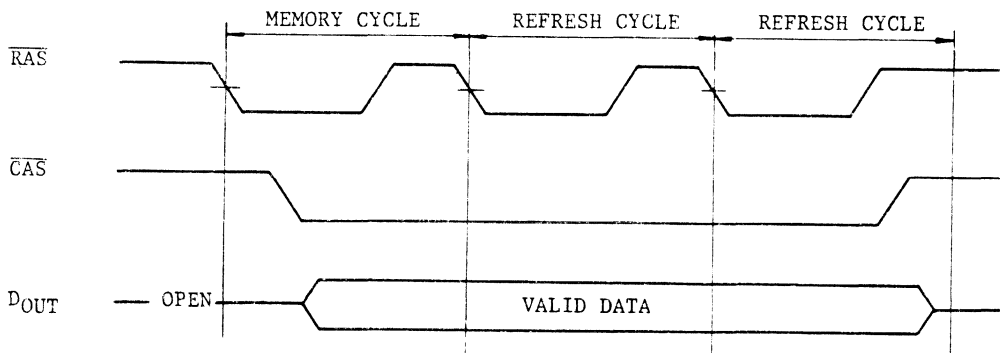
# TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12 TMM41257AP/AT/AZ-15

## $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH

$\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refreshing available on the TMM41257AP/AT/AZ offers an alternate refresh method. If  $\overline{\text{CAS}}$  is held on low for the specified period ( $t_{\text{CSR}}$ ) before  $\overline{\text{RAS}}$  goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh operation.

## HIDDEN REFRESH

An optional feature of the TMM41257AP/AT/AZ is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding  $\overline{\text{CAS}}$  at  $V_{\text{IL}}$  and taking  $\overline{\text{RAS}}$  high and after a specified precharge period ( $t_{\text{RP}}$ ), executing a  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

# TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12 TMM41257AP/AT/AZ-15

## $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TMM41257AP/AT/AZ can be tested by  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  cycles as initialization cycles. The test procedure is as follows.

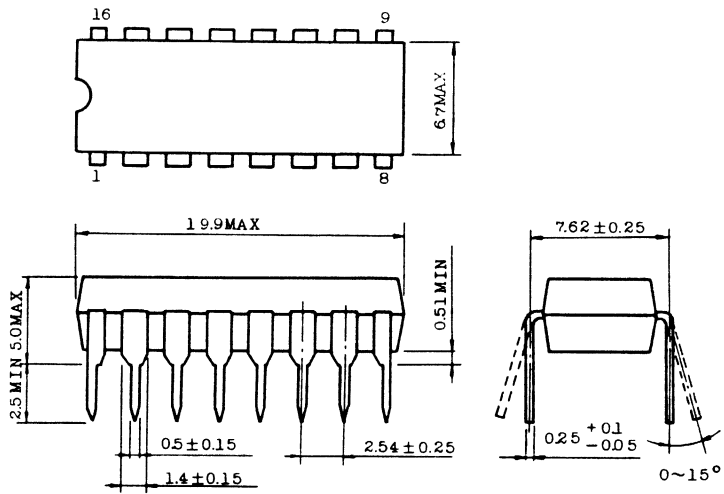
- ① Write "0" into all the memory cells at normal write mode.
- ② Select one certain column address and read "0" out and write "1" in each cell by performing  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 256 times.
- ③ Check "1" out of 256 bits at normal read mode, which was written at ②.
- ④ Using the same column as ②, read "1" out and write "0" in each cell performing  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH COUNTER TEST. Repeat this operation 256 times.
- ⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.
- ⑥ Perform the above ① to ⑤ the complement data.

# TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12 TMM41257AP/AT/AZ-15

## OUTLINE DRAWINGS

• Plastic DIP

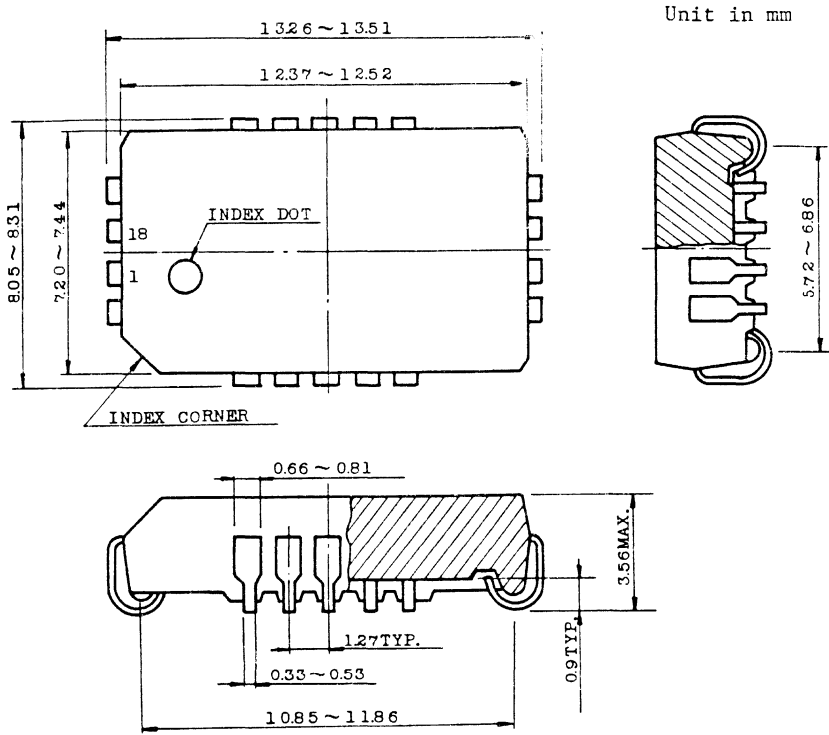
Unit in mm



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.16 leads. All dimensions are in millimeters.

**TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12  
TMM41257AP/AT/AZ-15**

• Plastic LCC



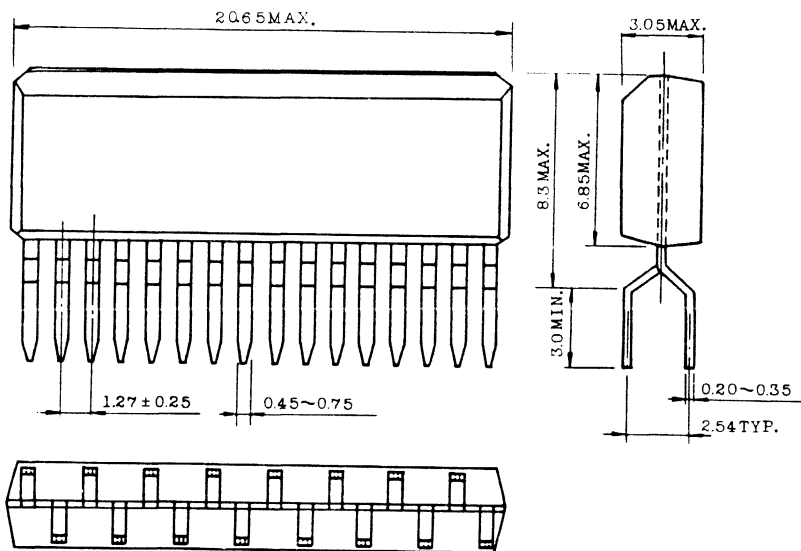
Note: Each lead pitch is 1.27mm. All dimensions are in millimeters.



# TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12 TMM41257AP/AT/AZ-15

- Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm. All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.



# TOSHIBA MOS MEMORY PRODUCT

**65,536 WORD × 4 BIT DYNAMIC RAM**  
**SILICON MONOLITHIC**  
**N-CHANNEL SILICON GATE MOS**

**TMM41464P-12**  
**TMM41464P-15**

## DESCRIPTION

The TMM41464P is the new generation dynamic RAM organized 65,536 word by 4 bit, it is successor to the industry standard TMM4164AP.

The TMM41464P utilizes TOSHIBA's N-channel/Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TMM

41464P to be packaged in a standard 18 pin plastic DIP. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include single power supply of  $5V \pm 10\%$  tolerance, direct interfacing capability with high performance logic families such as schottky TTL.

## FEATURES

- 65,536 words by 4 bit organization
- Fast access Time and cycle time

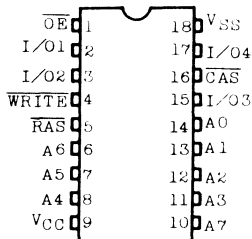
DEVICE	$t_{RAC}$	$t_{CAC}$	$t_{RC}$
TMM41464P-12	120ns	60ns	220ns
TMM41464P-15	150ns	75ns	260ns

- Single power supply of  $5V \pm 10\%$  with a built-in  $V_{BB}$  generator
- Low power:  
385mW Operating (MAX.) (TMM41464-12)

330mW Operating (MAX.) (TMM41464-15)  
 28mW Standby (MAX.)

- Industry standard 18 pin plastic DIP
- Output unlatented at cycle end allows two-dimensional chip selection
- Read-Modify-Write, RAS only refresh, Hidden refresh, CAS before RAS refresh, and Page Mode capability.
- All inputs and outputs TTL compatible
- 256 refresh cycles/4ms

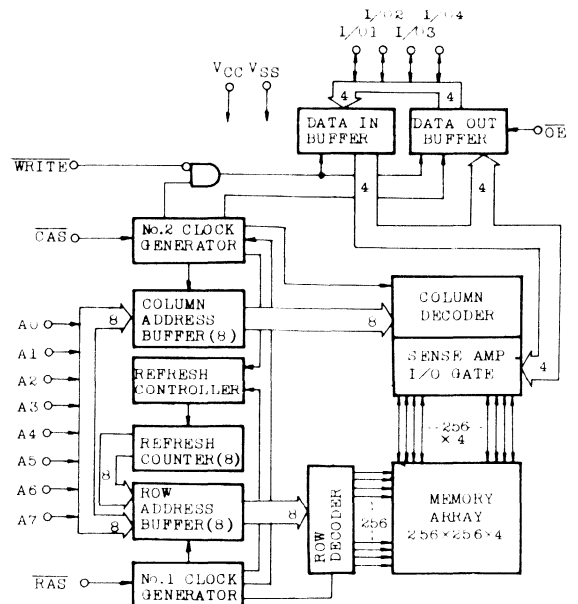
## PIN CONNECTION



## PIN NAMES

$A_0 \sim A_7$	Address Inputs
CAS	Column Address Strobe
$I/O_1 \sim I/O_4$	Data Input Output
RAS	Row Address Strobe
WRITE	Read Write Input
OE	Output Enable
$V_{CC}$	Power (+5V)
$V_{SS}$	Ground

## BLOCK DIAGRAM



# TMM41464P-12

# TMM41464P-15

## ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	$V_{in}, V_{out}$	-1~7	V	1
Power Supply Voltage	$V_{cc}$	-1~7	V	1
Operating Temperature	$T_{op}$	0~70	C	1
Storage Temperature	$T_{stg}$	55~150	C	1
Soldering Temperature-Time	$T_{solder}$	260-10	C-sec	1
Power Dissipation	$P_d$	600	mW	1
Short Circuit Output Current	$I_{sc}$	50	mA	1

## RECOMMENDED DC OPERATING CONDITIONS (Ta: 0~70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
$V_{cc}$	Supply Voltage	4.5	5.0	5.5	V	2
$V_{IH}$	Input High Voltage	2.4		6.5	V	2
$V_{IL}$	Input Low Voltage	1.0		0.8	V	2

## DC ELECTRICAL CHARACTERISTICS (V<sub>cc</sub>: 5V±10%, Ta: 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
$I_{cc1}$	OPERATING CURRENT Average Power Supply Operating Current (RAS, CAS Cycling: $t_{R1}$ to $t_{R2}$ MIN.)	TMM41464P-12	70	mA	3,4
		TMM41464P-15	60		
$I_{cc2}$	STANDBY CURRENT Power Supply Standby Current (RAS, CAS: $V_{cc}$ )		5	mA	
$I_{cc3}$	RAS ONLY REFRESH CURRENT Average Power Supply Current, RAS Only Mode (RAS Cycling, CAS: $V_{cc}$ ; $t_{R1}$ to $t_{R2}$ MIN.)	TMM41464P-12	60	mA	3
		TMM41464P-15	50		
$I_{cc4}$	PAGE MODE CURRENT Average Power Supply Current, Page Mode (RAS: $V_{cc}$ , CAS Cycling: $t_{R1}$ to $t_{R2}$ MIN.)	TMM41464P-12	60	mA	3,4
		TMM41464P-15	50		
$I_{cc5}$	CAS BEFORE RAS REFRESH CURRENT Average Power Supply Current, CAS Before RAS Mode (RAS Cycling, CAS Before RAS: $t_{R1}$ to $t_{R2}$ MIN.)	TMM41464P-12	60	mA	3
		TMM41464P-15	50		
$I_{IL}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V: $V_{cc}$ ; 6~5V, All Other Pins Not Under Test: 0V)	-10	10	$\mu$ A	
$I_{OL}$	OUTPUT LEAKAGE CURRENT (Data is disabled, 0V: $V_{cc}$ ; 6~5V)	-10	10	$\mu$ A	
$V_{OH}$	OUTPUT LEVEL Output "H" Level Voltage (I <sub>OL</sub> : -5mA)	2.4		V	
$V_{OL}$	OUTPUT LEVEL Output "L" Level Voltage (I <sub>OH</sub> : 4.2mA)		0.4	V	

# TMM41464P-12

# TMM41464P-15

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V<sub>CC</sub> = 5V ± 10%, T<sub>a</sub> = 0 ~ 70 °C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TMM41464P-12		TMM41464P-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t <sub>RC</sub>	Random Read or Write Cycle Time	220	—	260	—	ns	
t <sub>RMW</sub>	Read Modify Write Cycle Time	295	—	355	—	ns	
t <sub>PC</sub>	Page Mode Cycle Time	120	—	145	—	ns	
t <sub>RAC</sub>	Access Time from RAS	—	120	—	150	ns	8, 10
t <sub>CAC</sub>	Access Time from CAS	—	60	—	75	ns	9, 10
t <sub>OFF</sub>	Output Buffer Turn-Off Delay	0	35	0	40	ns	11
t <sub>t</sub>	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t <sub>RP</sub>	RAS Precharge Time	90	—	100	—	ns	
t <sub>RAS</sub>	RAS Pulse Width	120	10,000	150	10,000	ns	
t <sub>RSH</sub>	RAS Hold Time	60	—	75	—	ns	
t <sub>CSH</sub>	CAS Hold Time	120	—	150	—	ns	
t <sub>CAS</sub>	CAS Pulse Width	60	10,000	75	10,000	ns	
t <sub>RCO</sub>	RAS to CAS Delay Time	25	60	25	75	ns	13
t <sub>CRP</sub>	CAS to RAS Precharge Time	10	—	10	—	ns	
t <sub>CPN</sub>	CAS Precharge Time	20	—	25	—	ns	
t <sub>CP</sub>	CAS Precharge Time (for Page Mode Cycle Only)	50	—	60	—	ns	
t <sub>ASR</sub>	Row Address Set Up Time	0	—	0	—	ns	
t <sub>AH</sub>	Row Address Hold Time	15	—	15	—	ns	
t <sub>ASC</sub>	Column Address Set-Up Time	0	—	0	—	ns	
t <sub>AH</sub>	Column Address Hold Time	25	—	35	—	ns	
t <sub>AR</sub>	Column Address Hold Time Reference to RAS	85	—	110	—	ns	
t <sub>RCS</sub>	Read Command Set-Up Time	0	—	0	—	ns	
t <sub>RCH</sub>	Read Command Hold Time Reference to CAS	0	—	0	—	ns	12
t <sub>RRH</sub>	Read Command Hold Time Reference to RAS	15	—	20	—	ns	12
t <sub>WCH</sub>	Write Command Hold Time	35	—	45	—	ns	
t <sub>WCR</sub>	Write Command Hold Time Reference to RAS	95	—	120	—	ns	
t <sub>WP</sub>	Write Command Pulse Width	35	—	45	—	ns	
t <sub>RWL</sub>	Write Command to RAS Lead Time	35	—	45	—	ns	
t <sub>CWL</sub>	Write Command to CAS Lead Time	35	—	45	—	ns	
t <sub>DS</sub>	Data-In Set-Up Time	0	—	0	—	ns	14
t <sub>DH</sub>	Data-In Hold Time	35	—	45	—	ns	14
t <sub>DHR</sub>	Data-In Hold Time Reference to RAS	95	—	120	—	ns	
t <sub>REF</sub>	Refresh Period	—	4	—	4	ms	
t <sub>WCS</sub>	Write Command Set-Up Time	0	—	0	—	ns	15
t <sub>CWD</sub>	CAS to WRITE Delay	100	—	120	—	ns	15
t <sub>RWD</sub>	RAS to WRITE Delay	160	—	195	—	ns	15
t <sub>OEA</sub>	OE Access time	—	30	—	40	ns	
t <sub>OED</sub>	OE to Data Delay	30	—	40	—	ns	
t <sub>OEZ</sub>	Output Buffer Turn-Off Delay Time from OE	0	30	0	40	ns	
t <sub>OFH</sub>	OE Command Hold Time	30	—	40	—	ns	
t <sub>ROH</sub>	RAS Hold Time Reference to OE	0	—	0	—	ns	

# TMM41464P-12

# TMM41464P-15

SYMBOL	PARAMETER	TMM41464P-12		TMM41464P-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
$t_{H0}$	CAS Hold Time for CAS Before RAS Refresh	30	—	30	—	ns	
$t_{S0}$	CAS Set-Up Time for CAS Before RAS Refresh	10	—	10	—	ns	
$t_{P0}$	CAS Precharge to CAS Active Time	0	—	0	—	ns	
$t_{PC}$	CAS Precharge Time for CAS Before RAS Counter	50	—	60	—	ns	
$t_{TEST}$	Test						

## CAPACITANCE (V<sub>CC</sub> = 5V ± 10%, f = 1MHz, Ta = 0 ~ 70°C)

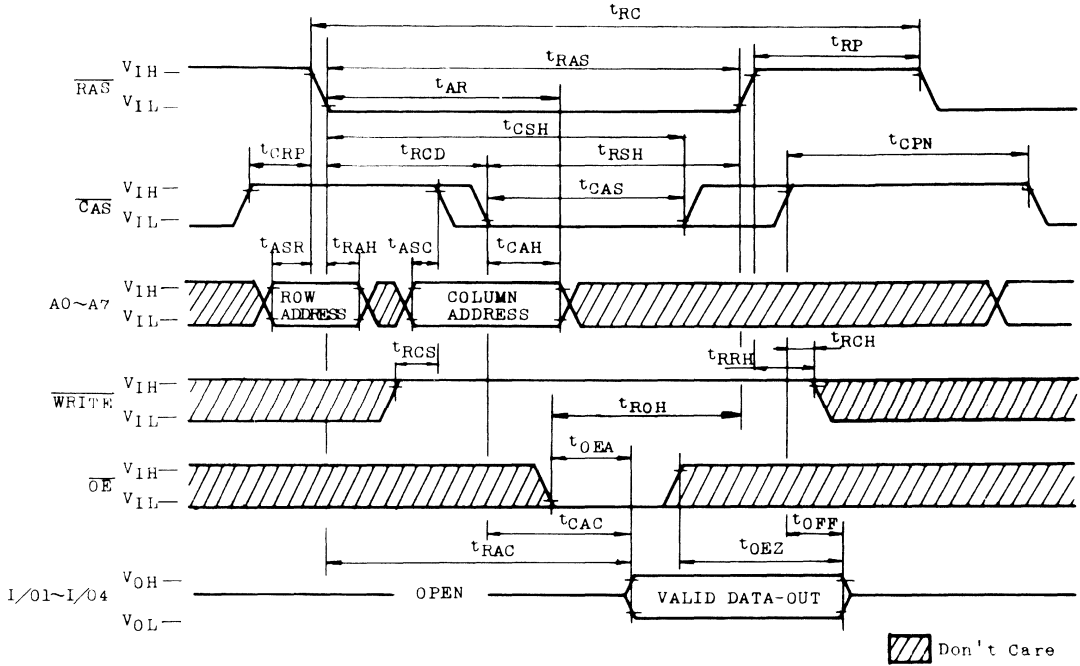
SYMBOL	PARAMETER	MIN.	MAX.	UNITS
$C_{II}$	Input Capacitance (A <sub>1</sub> ~ A <sub>4</sub> )		5	pf
$C_{IO}$	Input Capacitance (RAS, CAS, WRITE, OE)		7	pf
$C_{O}$	Input-Output Capacitance (I <sub>01</sub> ~ I <sub>04</sub> )		7	pf

### NOTES:

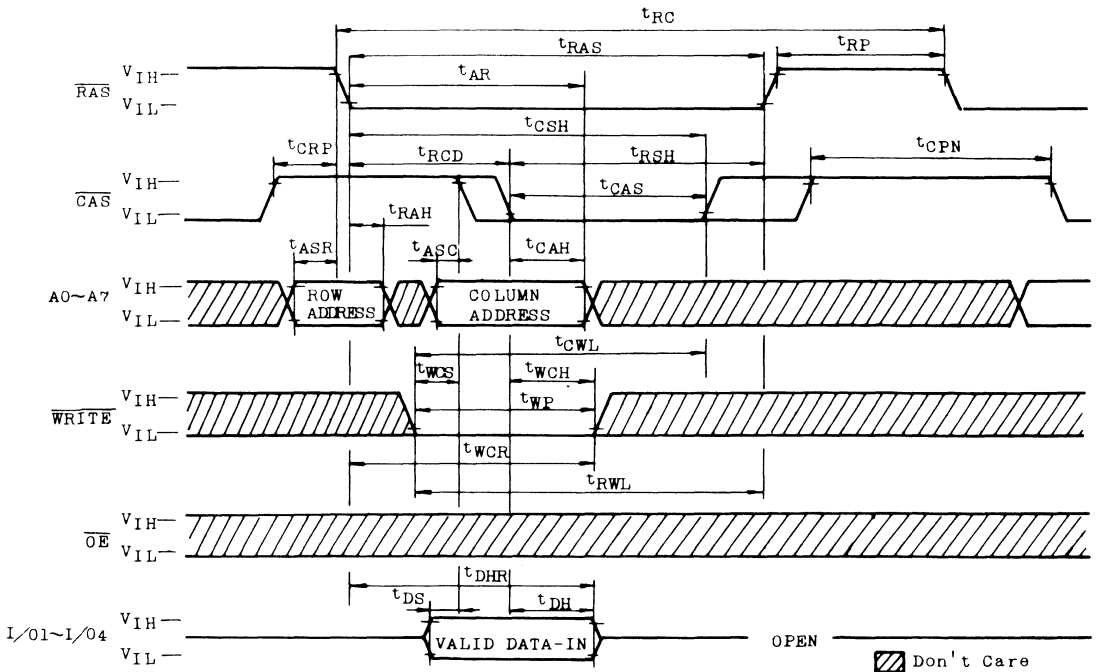
- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
- All voltages are referenced to V<sub>SS</sub>.
- I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub>, I<sub>CC5</sub> depend on cycle rate.
- I<sub>CC1</sub>, I<sub>CC4</sub> depend on output loading. Specified values are obtained with the output open.
- An initial pause of 200μs is required after power-up followed by any 8 CAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS Before RAS initialization cycles instead of 8 RAS cycle are required.
- AC measurements assume t<sub>r</sub> = 5ns.
- V<sub>IH(min.)</sub> and V<sub>IL(max.)</sub> are reference levels for measuring timing of input signals. Also, transition times are measured between V<sub>IH</sub> and V<sub>IL</sub>.
- Assumes that t<sub>RCD</sub> ≤ t<sub>RCD</sub> (max.). If t<sub>RCD</sub> is greater than the maximum recommended value shown in this table, t<sub>RAC</sub> will increase by the amount that t<sub>RCD</sub> exceeds the value shown.
- Assumes that t<sub>RCD</sub> ≥ t<sub>RCD</sub> (max.).
- Measured with a load equivalent to 2 TLL loads and 100pF.
- t<sub>OFF</sub> (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- Either t<sub>RCH</sub> or t<sub>RPH</sub> must be satisfied for a read cycle.
- Operation within the t<sub>RCD</sub> (max.) limit insures that t<sub>RAC</sub> (max.) can be met.  
t<sub>RCD</sub> (max.) is specified as a reference point only: If t<sub>RCD</sub> is greater than the specified t<sub>RCD</sub> (max.) limit, then access time is controlled exclusively by t<sub>RAC</sub>.
- These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in read/write or read-modify-write cycles.
- t<sub>WCS</sub>, t<sub>OWD</sub> and t<sub>RWD</sub> are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t<sub>WCS</sub> ≥ t<sub>WCS</sub> (min.), the cycle is an early write cycle and the input/output pin will remain open circuits (high impedance) throughout the entire cycle; If t<sub>RWD</sub> ≥ t<sub>RWD</sub> (min.) and t<sub>RWD</sub> ≥ t<sub>RWD</sub> (min.), the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell.

**TMM41464P-12**  
**TMM41464P-15**

● READ CYCLE

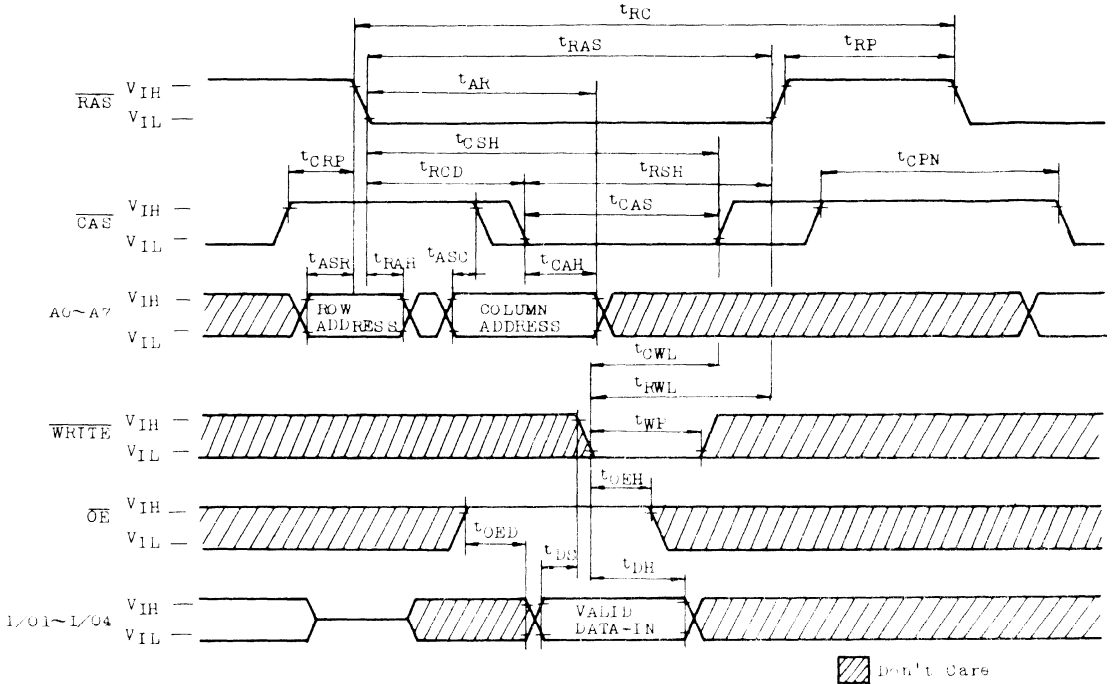


● WRITE CYCLE (EARLY WRITE)

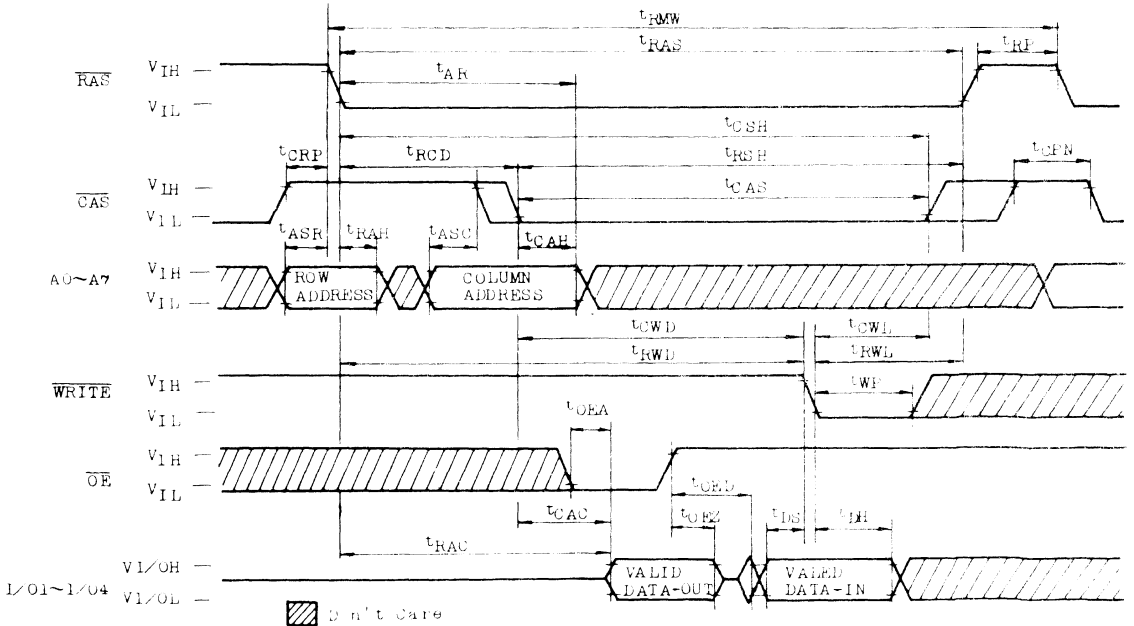


# TMM41464P-12 TMM41464P-15

## ● WRITE CYCLE (OE CONTROLLED WRITE)



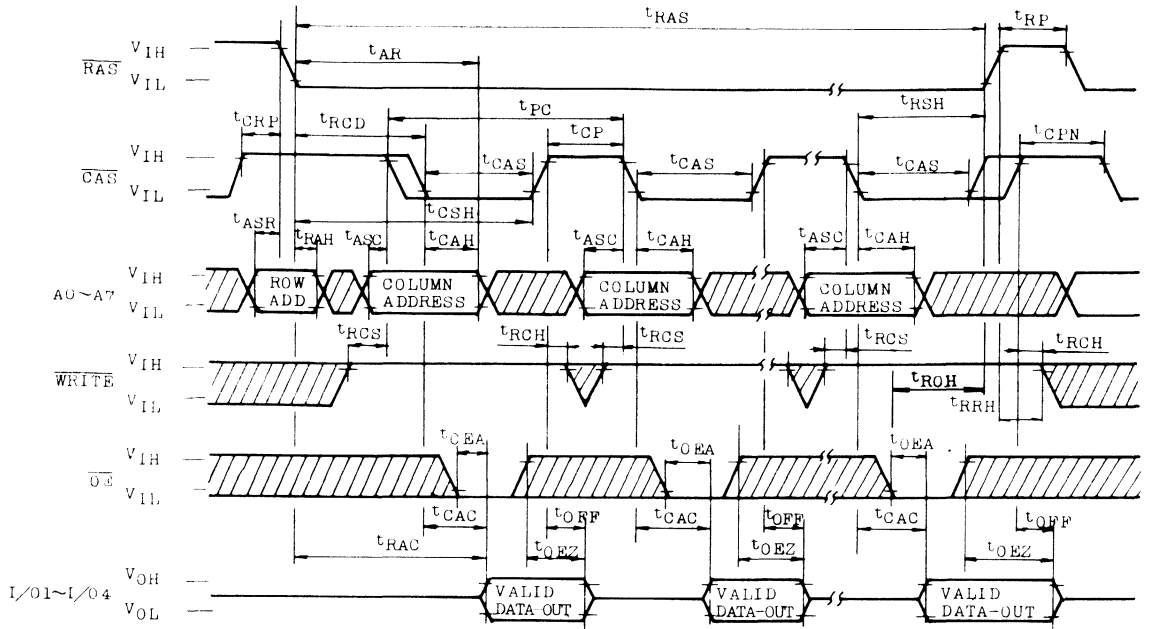
## ● READ-WRITE READ-MODIFY-WRITE CYCLE



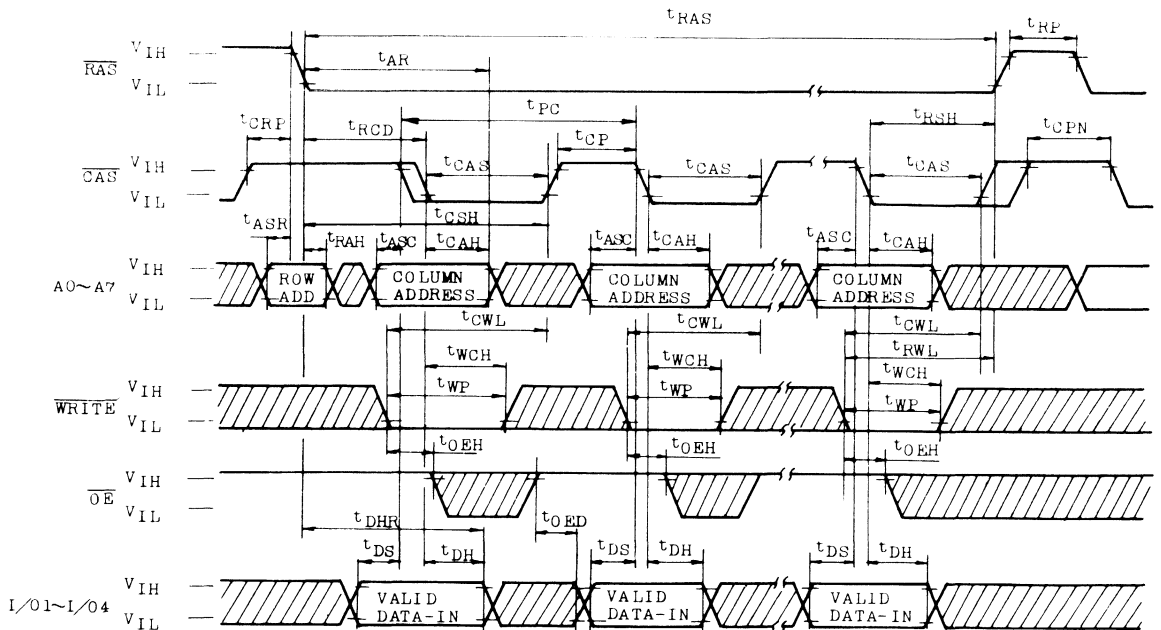


# TMM41464P-12 TMM41464P-15

## ● PAGE MODE READ CYCLE

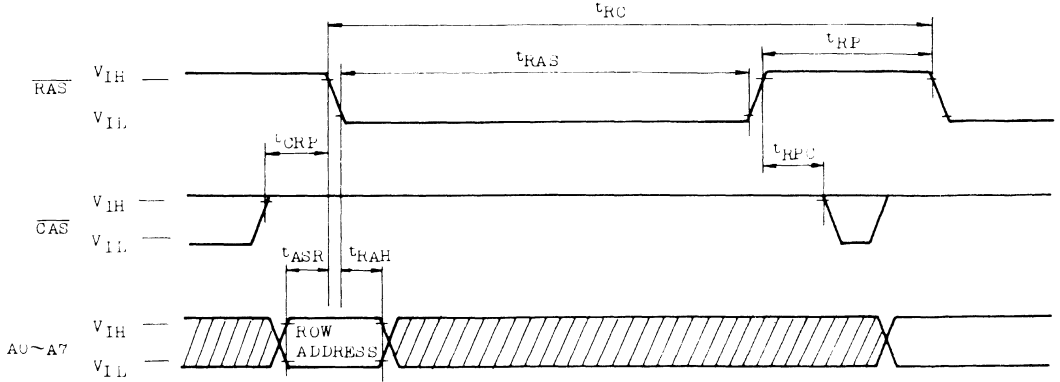


## ● PAGE MODE WRITE CYCLE



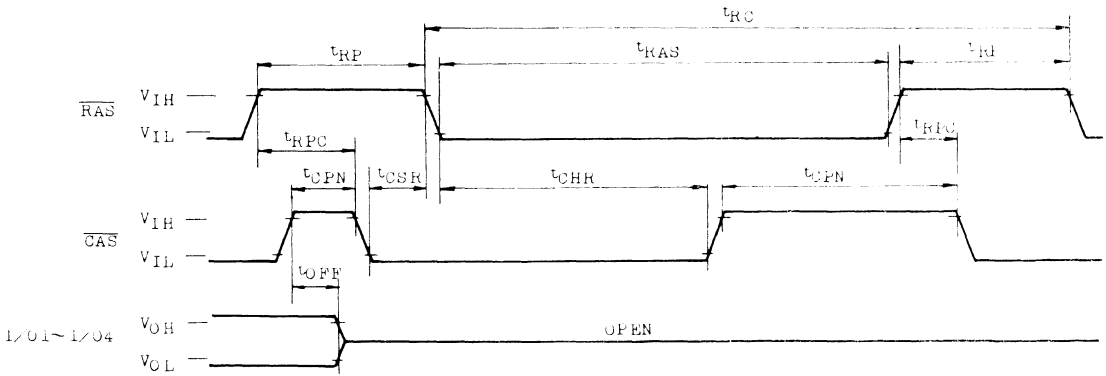
# TMM41464P-12 TMM41464P-15

●  $\overline{\text{RAS}}$  ONLY REFRESH CYCLE



Notes:  $\overline{\text{WRITE}}$ ,  $\overline{\text{OE}}$ =Don't Care      Don't Care

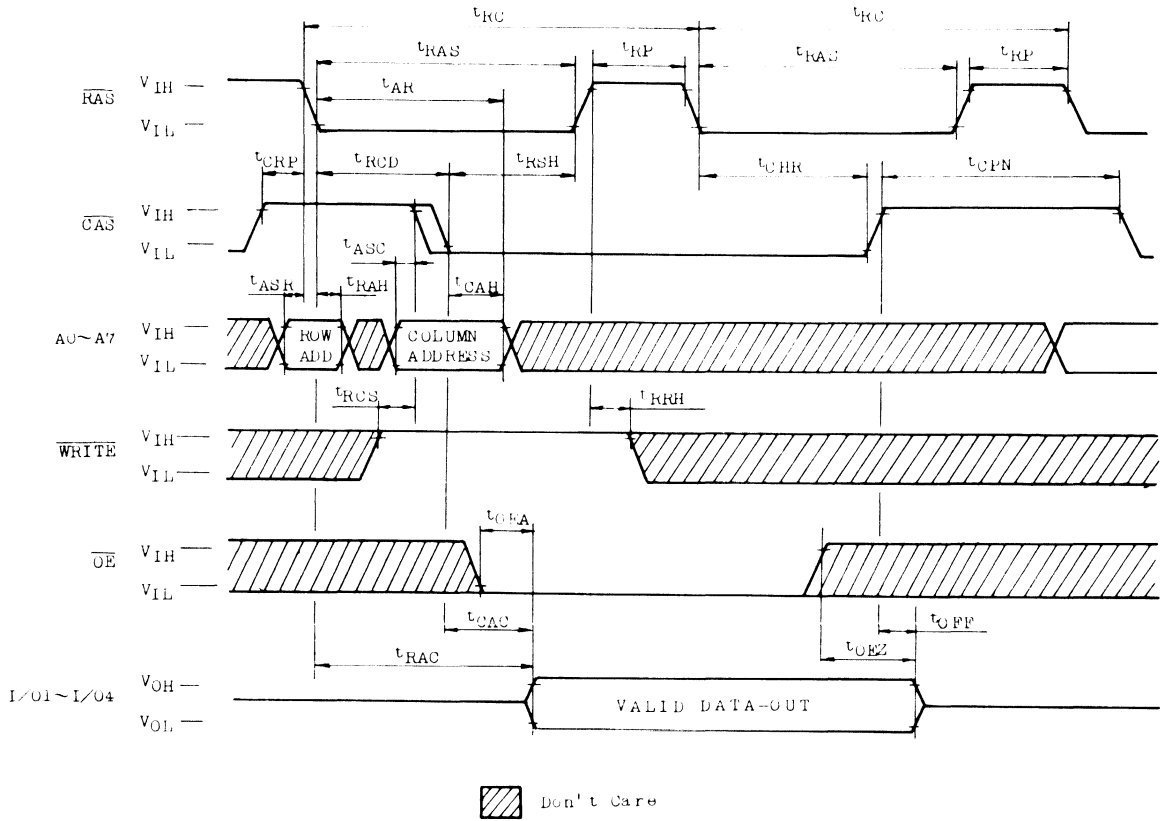
● CAS BEFORE RAS REFRESH CYCLE



Note:  $\overline{\text{WRITE}}$ ,  $\overline{\text{OE}}$ , A0 ~ A7=Don't Care

**TMM4164P-12**  
**TMM4164P-15**

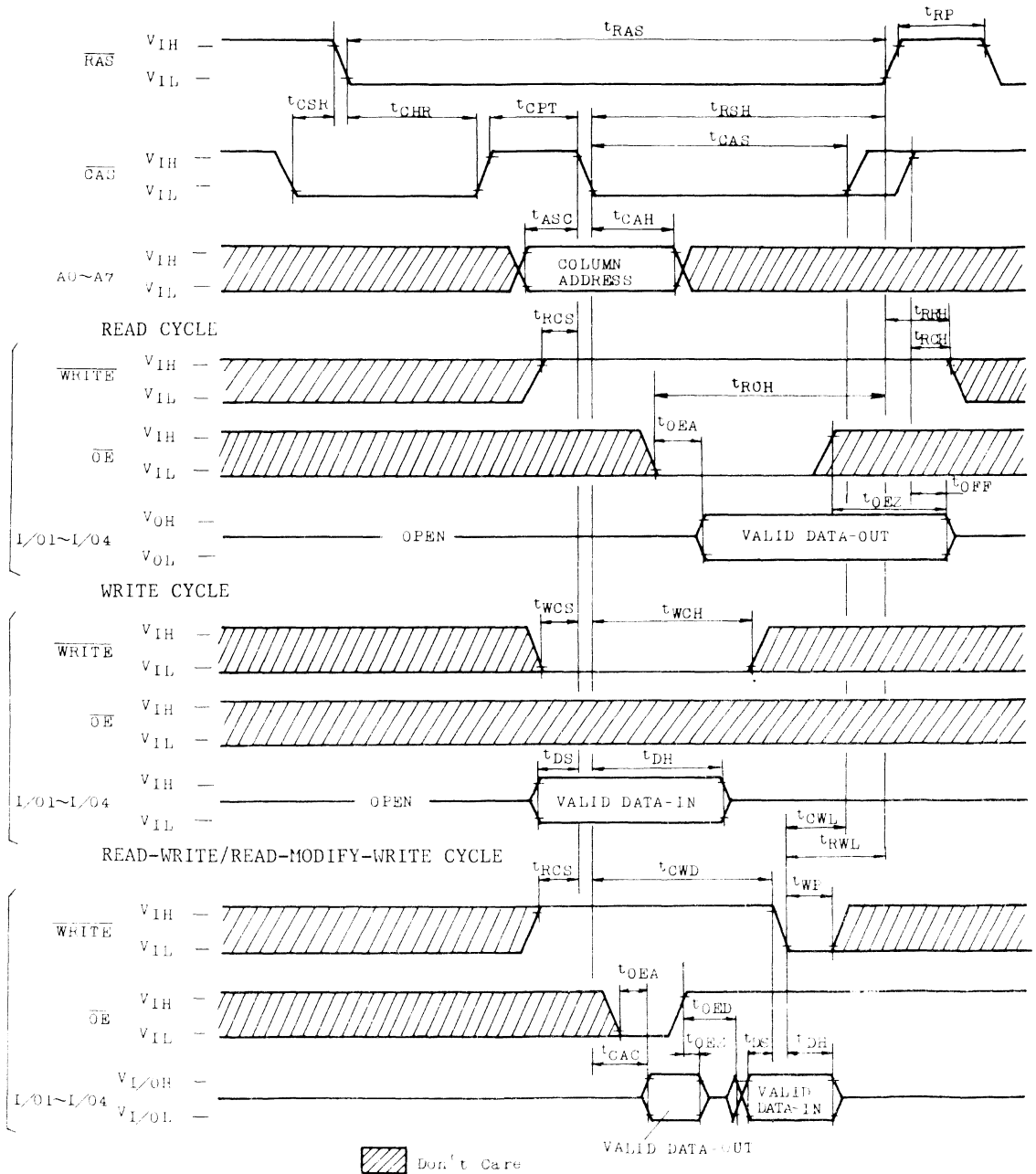
● HIDDEN REFRESH CYCLE



# TMM41464P-12

# TMM41464P-15

● CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



## APPLICATION INFORMATION

### ADDRESSING

The 16 address bits required to decode 1 of the 65,536 cell locations within the TMM41464P are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ( $\overline{\text{RAS}}$ ), latches the 8 row address bits into the chip. The second clock, the Column Address Strobe ( $\overline{\text{CAS}}$ ), subsequently latches the 8 column address bits into the chip. Each of these signals,  $\overline{\text{RAS}}$ , and  $\overline{\text{CAS}}$ , triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the  $\overline{\text{CAS}}$  clock sequence are inhibited until the occurrence of a delayed signal derived from the  $\overline{\text{RAS}}$  clock chain. This "gated  $\overline{\text{CAS}}$ " feature allows the  $\overline{\text{CAS}}$  clock to be externally activated as soon as the Row Address Hold Time specification ( $t_{\text{RAH}}$ ) has been satisfied and the address inputs have been changed from Row address to Column address information.

### Data Inputs

Data is written during write or read-modify-write cycle.

The falling edge of  $\overline{\text{CAS}}$  or  $\overline{\text{WRITE}}$  strobes data into the on-chip data latches.

In an early-write cycle,  $\overline{\text{WRITE}}$  is brought low prior to  $\overline{\text{CAS}}$  and the data is strobed in by  $\overline{\text{CAS}}$  with setup and hold times referenced to this signal. In delayed write or read-modify-write cycle,  $\overline{\text{CAS}}$  will already be low, thus the data will be strobed in by  $\overline{\text{WRITE}}$  with setup and hold time referenced to this signal.

In delayed or read-modify-write,  $\overline{\text{OE}}$  must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

### Data outputs

The three-state output buffers provide direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until  $\overline{\text{CAS}}$  is brought low. In a read cycle the outputs go active after the access time interval  $t_{\text{RAC}}$  and  $t_{\text{OEA}}$  are satisfied.

The outputs become valid after the access time has elapsed and remain valid while  $\overline{\text{CAS}}$  and  $\overline{\text{OE}}$  are

low.  $\overline{\text{CAS}}$  or  $\overline{\text{OE}}$  going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The  $\overline{\text{OE}}$  controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the  $\overline{\text{OE}}$  input is brought to a logic low level, the output buffers are enabled. Both  $\overline{\text{CAS}}$  and  $\overline{\text{OE}}$  can control the outputs. Thus in a read operation, either  $\overline{\text{OE}}$  or  $\overline{\text{CAS}}$  returning high forces the outputs into the high impedance state.

### $\overline{\text{RAS}}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address ( $A_0$ - $A_7$ ) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "RAS-only" cycles,  $\overline{\text{RAS}}$  only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the  $I_{\text{CC3}}$  specification.

### $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH

$\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refreshing available on the TMM41464P offers an alternate refresh method. If  $\overline{\text{CAS}}$  is held on low for the specified period ( $t_{\text{CSH}}$ ) before  $\overline{\text{RAS}}$  goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place.

After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh operation.

### PAGE MODE

The "Page-Mode" feature of the TMM41464P allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the  $\overline{\text{RAS}}$  signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page-Mode" of operation will not dissipate the power associated with the negative

# TMM41464P-12

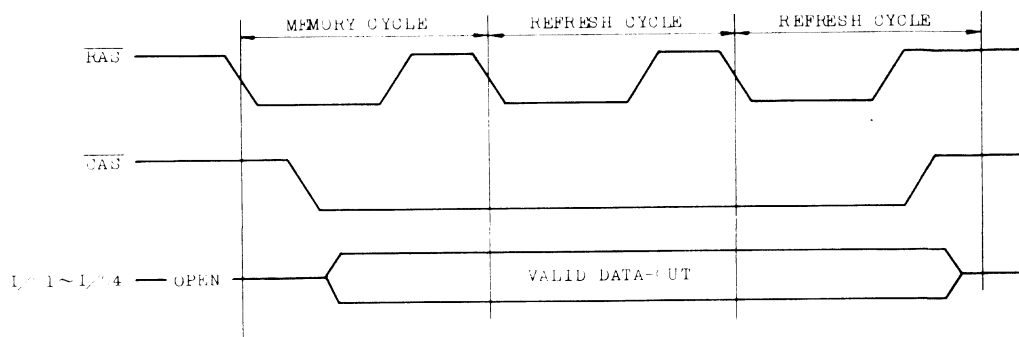
# TMM41464P-15

going edge of  $\overline{\text{RAS}}$ . Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

## HIDDEN REFRESH

An optional feature of the TMM41464P is that

refresh cycle may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding  $\overline{\text{CAS}}$  at  $V_{IL}$  and taking  $\overline{\text{RAS}}$  high and after a specified precharge period ( $t_{RP}$ ), executing a  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

## $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TMM41464P can be tested by  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  cycles as initialization cycles. The test procedure is as follows.

- ① Write "0" into all the memory cells at normal write mode.
- ② Select one certain column address and read "0" out and write "1" in each cell by performing  $\overline{\text{CAS}}$

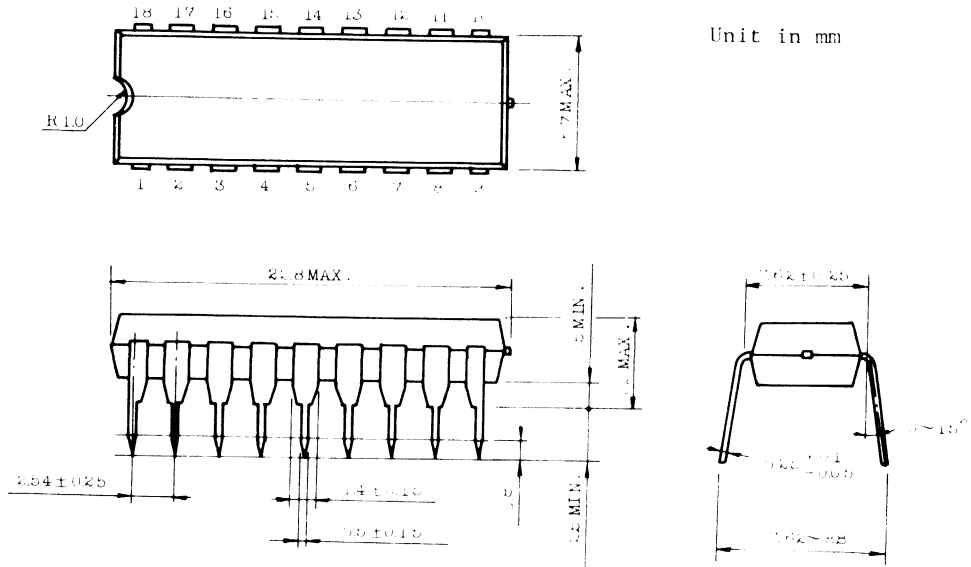
## BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-WRITE CYCLE).

Repeat this operation 256 times.

- ③ Check "1" out of 256 bits at normal read mode, which was written at ②.
- ④ Using the same column as ②, read "1" out and write "0" in each cell performing  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH COUNTER TEST. Repeat this operation 256 times.
- ⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.
- ⑥ Perform the above ① to ⑤ to the complement data.

**TMM41464P-12**  
**TMM41464P-15**

**OUTLINE DRAWINGS**



Unit in mm

NOTES : Each lead pitch is  $2.54 \text{ mm}$ . All leads are located within  $0.25 \text{ mm}$  of their true longitudinal position with respect to No. 1 and No. 18 leads. All dimensions are in millimeters.

**TMM41464P-12**  
**TMM41464P-15**

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.  
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# TOSHIBA MOS MEMORY PRODUCT

1,048,576 WORDS × 1 BIT DYNAMIC RAM  
SILICON GATE CMOS

TC511000P/J/Z-85, TC511000P/J/Z-10  
TC511000P/J/Z-12

## DESCRIPTION

The TC511000P/J/Z is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511000P/J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511000P/J/Z to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. "Test Mode" function is implemented from Revision C.

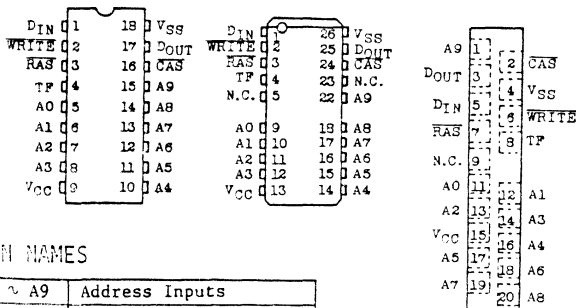
## FEATURES

- 1,048,576 words by 1 bit organization
- Fast access time and cycle time
- Low Power  
385mW MAX. Operating (TC511000P/J/Z-85)  
330mW MAX. Operating (TC511000P/J/Z-10)  
275mW MAX. Operating (TC511000P/J/Z-12)  
5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write,  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh,  $\overline{\text{RAS}}$ -only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/3ms
- Package  
Plastic DIP: TC511000P  
Plastic SOJ: TC511000J  
Plastic ZIP: TC511000Z

		TC511000P/J/Z-85-10-12		
$t_{\text{RAC}}$	$\overline{\text{RAS}}$ Access Time	85ns	100ns	120ns
$t_{\text{AA}}$	Column Address Access Time	45ns	50ns	60ns
$t_{\text{CAC}}$	$\overline{\text{CAS}}$ Access Time	25ns	25ns	30ns
$t_{\text{RC}}$	Cycle Time	165ns	190ns	220ns
$t_{\text{PC}}$	Fast Page Mode Cycle Time	50ns	55ns	70ns

## PIN CONNECTION (TOP VIEW)

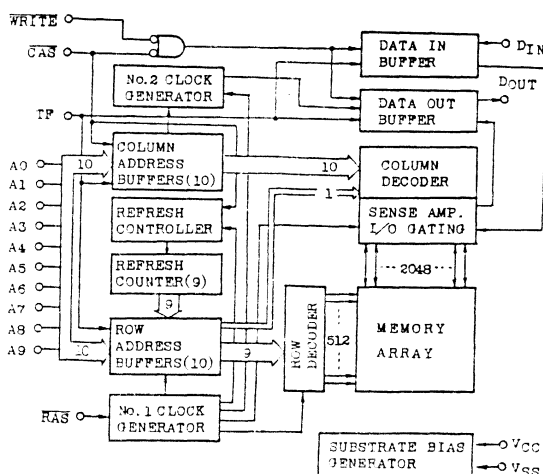
Plastic DIP      Plastic SOJ      Plastic ZIP



## PIN NAMES

A0 ~ A9	Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
DIN	Data In
DOUT	Data Out
$\overline{\text{CAS}}$	Column Address Strobe
WRITE	Read/Write Input
$V_{\text{CC}}$	Power (+5V)
$V_{\text{SS}}$	Ground
TF	Test Function
N.C.	No Connection

## BLOCK DIAGRAM



# TC511000P/J/Z-85, TC511000P/J/Z-10 TC511000P/J/Z-12

## ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V <sub>IN</sub>	-1 ~ 7	V	1
Test Function Input Voltage	V <sub>IN(TF)</sub>	-1 ~ 10.5	V	1
Output Voltage	V <sub>OUT</sub>	-1 ~ 7	V	1
Power Supply Voltage	V <sub>CC</sub>	-1 ~ 7	V	1
Operating Temperature	T <sub>OPR</sub>	0 ~ 70	°C	1
Storage Temperature	T <sub>STG</sub>	-55 ~ 150	°C	1
Soldering Temperature · Time	T <sub>SDLER</sub>	260 · 10	°C · sec	1
Power Dissipation	P <sub>d</sub>	600	mW	1
Short Circuit Output Current	I <sub>OUT</sub>	50	mA	1

## RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V	2
V <sub>IH</sub>	Input High Voltage	2.4	-	6.5	V	2
V <sub>IL</sub>	Input Low Voltage	-1.0	-	0.8	V	2
V <sub>IH(TF)</sub>	Test Enable Input High Voltage	V <sub>CC</sub> +4.5	-	10.5	V	2

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10%, Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES	
I <sub>CC1</sub>	OPERATING CURRENT	TC511000P/J/Z-85	-	70	mA	3,4
	Average Power Supply Operating Current (RAS, CAS, Address Cycling: t <sub>RC</sub> =t <sub>RC</sub> MIN.)	TC511000P/J/Z-10	-	60		
		TC511000P/J/Z-12	-	50		
I <sub>CC2</sub>	STANDBY CURRENT Power Supply Standby Current (RAS=CAS=V <sub>IH</sub> )	-	2	mA		
I <sub>CC3</sub>	RAS ONLY REFRESH CURRENT	TC511000P/J/Z-85	-	70	mA	3
	Average Power Supply Current, RAS Only Mode (RAS Cycling, CAS=V <sub>IH</sub> : t <sub>RC</sub> =t <sub>RC</sub> MIN.)	TC511000P/J/Z-10	-	60		
		TC511000P/J/Z-12	-	50		
I <sub>CC4</sub>	FAST PAGE MODE CURRENT	TC511000P/J/Z-85	-	50	mA	3,4
	Average Power Supply Current, Fast Page Mode (RAS=V <sub>IL</sub> , CAS, Address Cycling: t <sub>PC</sub> =t <sub>PC</sub> MIN.)	TC511000P/J/Z-10	-	40		
		TC511000P/J/Z-12	-	30		
I <sub>CC5</sub>	STANDBY CURRENT Power Supply Standby Current (RAS=CAS=V <sub>CC</sub> -0.2V)	-	1	mA		
I <sub>CC6</sub>	CAS BEFORE RAS REFRESH CURRENT	TC511000P/J/Z-85	-	70	mA	3
	Average Power Supply Current, CAS Before RAS Mode (RAS, CAS Cycling: t <sub>RC</sub> =t <sub>RC</sub> MIN.)	TC511000P/J/Z-10	-	60		
		TC511000P/J/Z-12	-	50		
I <sub>I(L)</sub>	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input (0V ≤ V <sub>IN</sub> ≤ 6.5V, All Other Pins Not Under Test=0V)	-10	10	μA		
I <sub>ITF(L)</sub>	INPUT LEAKAGE CURRENT (only TF) (0V ≤ V <sub>IN(TF)</sub> ≤ 0.8V, All Other Pins Not Under Test=0V)	-10	10	μA		
I <sub>O(L)</sub>	OUTPUT LEAKAGE CURRENT (DOUT is disabled, 0V ≤ V <sub>OUT</sub> ≤ 5.5V)	-10	10	μA		
I <sub>TF</sub>	TEST FUNCTION INPUT CURRENT (V <sub>CC</sub> +4.5V ≤ V <sub>IN(TF)</sub> ≤ 10.5V)	-	1	mA		
V <sub>OH</sub>	OUTPUT LEVEL Output "H" Level Voltage (I <sub>OUT</sub> =-5mA)	2.4	-	V		
V <sub>OL</sub>	OUTPUT LEVEL Output "L" Level Voltage (I <sub>OUT</sub> =4.2mA)	-	0.4	V		

# TC511000P/J/Z-85, TC511000P/J/Z-10 TC511000P/J/Z-12

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V<sub>CC</sub>=5V±10%, T<sub>a</sub>=0~70°C)(Notes 5, 6, 7)

SYMBOL	PARAMETER	TC511000P/J/Z-85		TC511000P/J/Z-10		TC511000P/J/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t <sub>RC</sub>	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t <sub>RWC</sub>	Read-Write Cycle Time	190	-	220	-	255	-	ns	
t <sub>PC</sub>	Fast Page Mode Cycle Time	50	-	55	-	70	-	ns	
t <sub>PRWC</sub>	Fast Page Mode Read-Write Cycle Time	75	-	85	-	105	-	ns	
t <sub>RAC</sub>	Access Time from $\overline{\text{RAS}}$	-	85	-	100	-	120	ns	8,13
t <sub>CAC</sub>	Access Time from $\overline{\text{CAS}}$	-	25	-	25	-	30	ns	8,13
t <sub>AA</sub>	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
t <sub>CPA</sub>	Access Time from $\overline{\text{CAS}}$ Precharge	-	45	-	50	-	65	ns	8
t <sub>CLZ</sub>	$\overline{\text{CAS}}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
t <sub>OFF</sub>	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
t <sub>T</sub>	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t <sub>RP</sub>	$\overline{\text{RAS}}$ Precharge Time	70	-	80	-	90	-	ns	
t <sub>RAS</sub>	$\overline{\text{RAS}}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t <sub>RASP</sub>	$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	85	100,000	100	100,000	120	100,000	ns	
t <sub>RSH</sub>	$\overline{\text{RAS}}$ Hold Time	25	-	25	-	30	-	ns	
t <sub>CSH</sub>	$\overline{\text{CAS}}$ Hold Time	85	-	100	-	120	-	ns	
t <sub>CAS</sub>	$\overline{\text{CAS}}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t <sub>RCD</sub>	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	25	60	25	75	25	90	ns	13
t <sub>RAD</sub>	$\overline{\text{RAS}}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t <sub>CRP</sub>	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	10	-	10	-	10	-	ns	
t <sub>CP</sub>	$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	10	-	10	-	15	-	ns	
t <sub>ASR</sub>	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t <sub>RAH</sub>	Row Address Hold Time	15	-	15	-	15	-	ns	
t <sub>ASC</sub>	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t <sub>CAH</sub>	Column Address Hold Time	20	-	20	-	25	-	ns	
t <sub>AR</sub>	Column Address Hold Time referenced to $\overline{\text{RAS}}$	65	-	75	-	90	-	ns	
t <sub>RAL</sub>	Column Address to $\overline{\text{RAS}}$ Lead Time	45	-	50	-	60	-	ns	
t <sub>RCS</sub>	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t <sub>RCH</sub>	Read Command Hold Time	0	-	0	-	0	-	ns	10
t <sub>RRH</sub>	Read Command Hold Time referenced to $\overline{\text{RAS}}$	0	-	0	-	0	-	ns	10

**TC511000P/J/Z-85, TC511000P/J/Z-10  
TC511000P/J/Z-12**

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC511000P/J/Z-85		TC511000P/J/Z-10		TC511000P/J/Z-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$t_{WCH}$	Write Command Hold Time	20	-	20	-	25	-	ns	
$t_{WCR}$	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
$t_{WP}$	Write Command Pulse Width	20	-	20	-	25	-	ns	
$t_{RWL}$	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
$t_{CWL}$	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	30	-	ns	
$t_{DS}$	Data Set-Up Time	0	-	0	-	0	-	ns	11
$t_{DH}$	Data Hold Time	20	-	20	-	25	-	ns	11
$t_{DHR}$	Data Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
$t_{REF}$	Refresh Period	-	8	-	8	-	8	ms	
$t_{WCS}$	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
$t_{CWD}$	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	25	-	25	-	30	-	ns	12
$t_{RWD}$	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	85	-	100	-	120	-	ns	12
$t_{AWD}$	Column Address to $\overline{WRITE}$ Delay Time	45	-	50	-	60	-	ns	12
$t_{CSR}$	$\overline{CAS}$ Set-Up Time ( $\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
$t_{CHR}$	$\overline{CAS}$ Hold Time ( $\overline{CAS}$ before $\overline{RAS}$ Cycle)	30	-	30	-	30	-	ns	
$t_{RPC}$	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
$t_{CPT}$	$\overline{CAS}$ Precharge Time ( $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50	-	50	-	60	-	ns	
$t_{CPN}$	$\overline{CAS}$ Precharge Time	15	-	15	-	20	-	ns	
$t_{TES}$	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	
$t_{TEH}$	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	

# TC511000P/J/Z-85, TC511000P/J/Z-10 TC511000P/J/Z-12

CAPACITANCE ( $V_{CC}=5V\pm 10\%$ ,  $f=1\text{MHz}$ ,  $T_a=0\sim 70^\circ\text{C}$ )

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$C_{I1}$	Input Capacitance ( $A0 \sim A9, D_{IN}$ )	-	5	pF
$C_{I2}$	Input Capacitance ( $\overline{\text{RAS}}, \overline{\text{CAS}}, \overline{\text{WRITE}}, \text{TF}$ )	-	7	
$C_O$	Output Capacitance ( $D_{OUT}$ )	-	7	

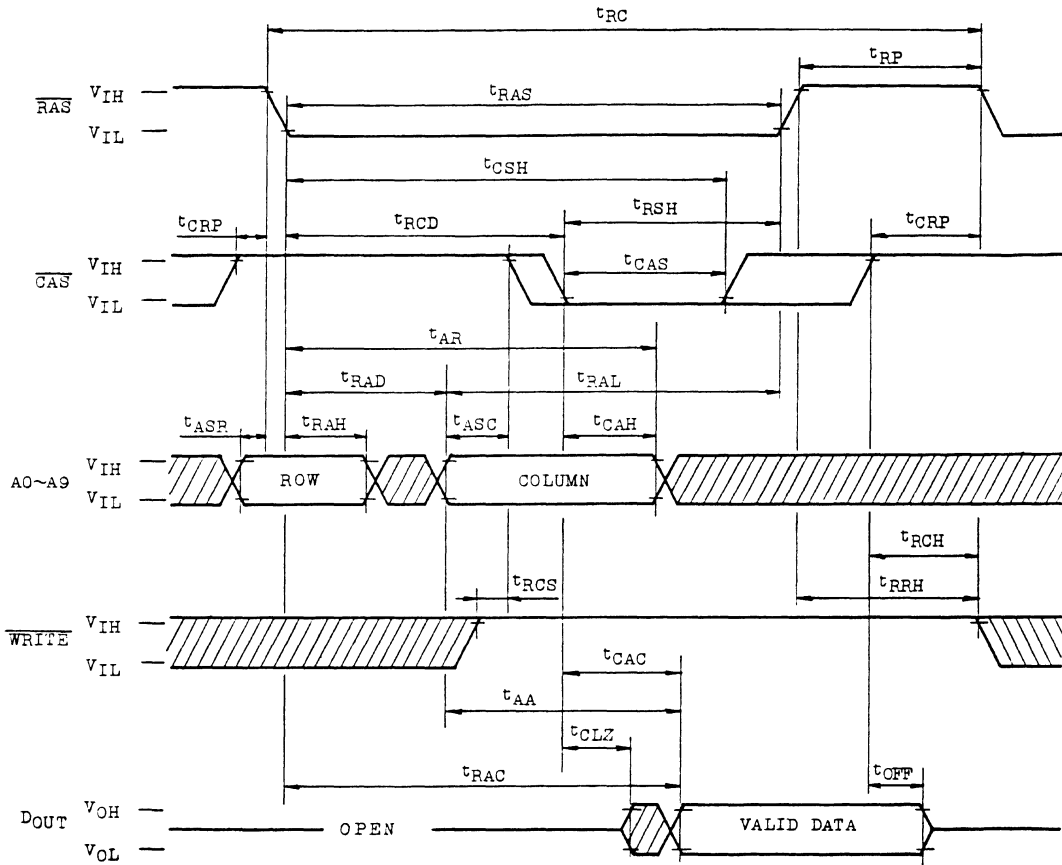
**NOTES:**


1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All Voltages are referenced to  $V_{SS}$ .
3.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ ,  $I_{CC6}$  depend on cycle rate.
4.  $I_{CC1}$ ,  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200 $\mu$ s is required after power-up followed by 8  $\overline{\text{RAS}}$  cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  initialization cycles instead of 8  $\overline{\text{RAS}}$  cycles are required.
6. AC measurements assume  $t_I=5\text{ns}$ .
7.  $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9.  $t_{OFF}(\text{max.})$  defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
11. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early write cycles and to  $\overline{\text{WRITE}}$  leading edge in read-write cycles.
12.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$  and  $t_{AWD} \geq t_{AWD}(\text{min.})$ , the cycle is a read-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the  $t_{RCD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled by  $t_{CAC}$ .
14. Operation within the  $t_{RAD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only: If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled by  $t_{AA}$ .

# TC511000P/J/Z-85, TC511000P/J/Z-10 TC511000P/J/Z-12

## TIMING WAVEFORMS

### READ CYCLE

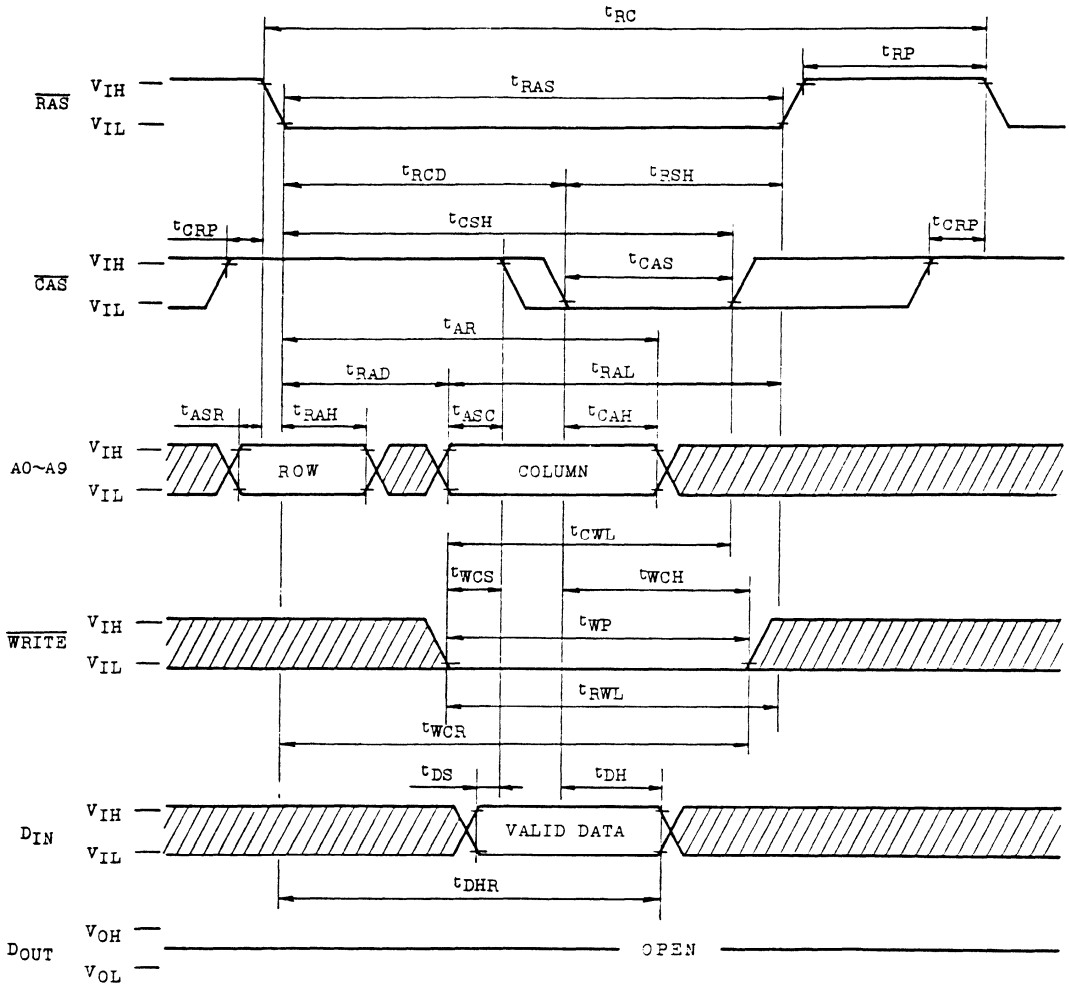



 : "H" or "L"

NOTE: "TF" pin should be connected to  $V_{IL}$  level or open, if "Test Mode" is not used.

**TC511000P/J/Z-85, TC511000P/J/Z-10  
TC511000P/J/Z-12**

WRITE CYCLE (EARLY WRITE)

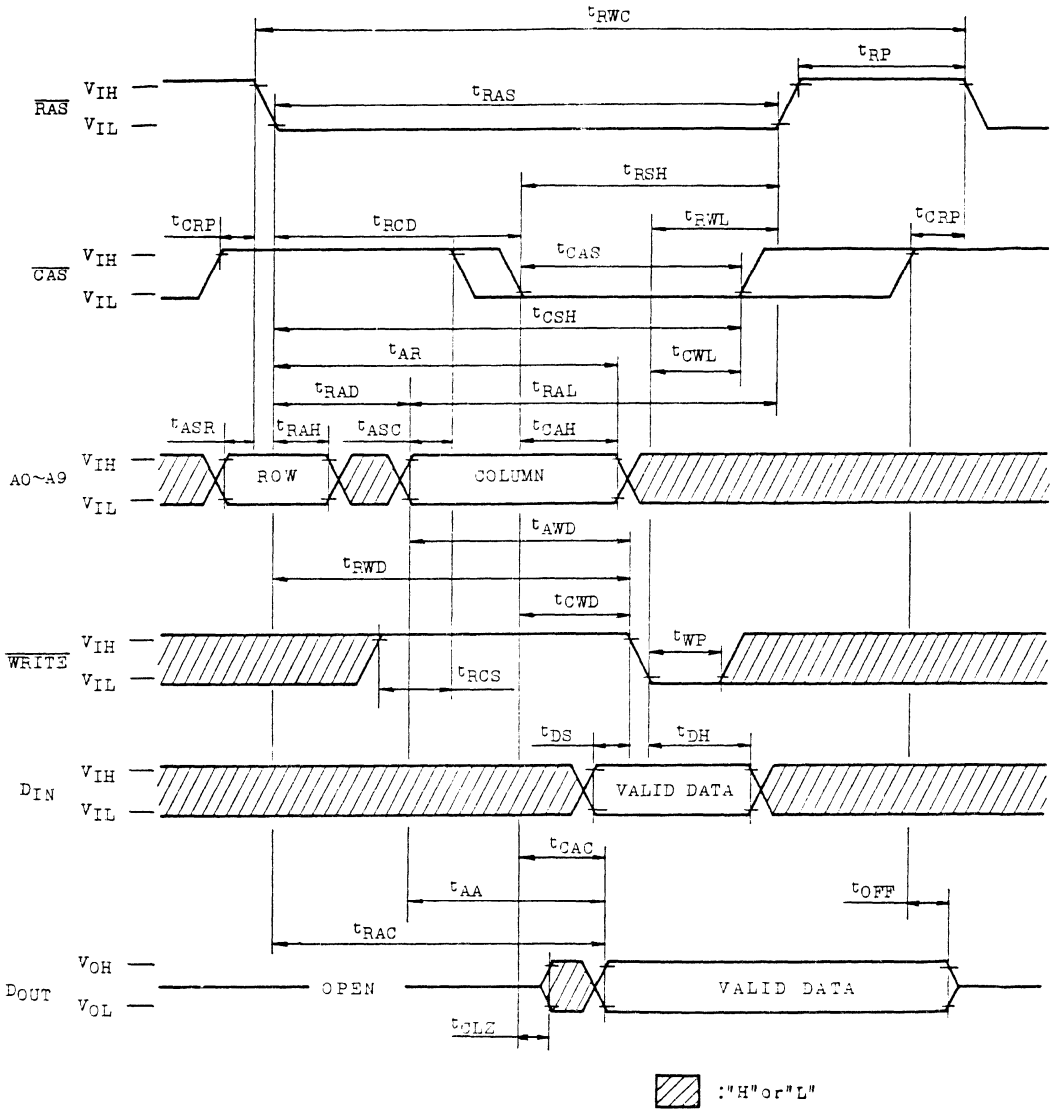


 : "H" or "L"

NOTE: "TF" pin should be connected to  $V_{IL}$  level or open, if "Test Mode" is not used.

**TC511000P/J/Z-85, TC511000P/J/Z-10  
TC511000P/J/Z-12**

READ-WRITE CYCLE

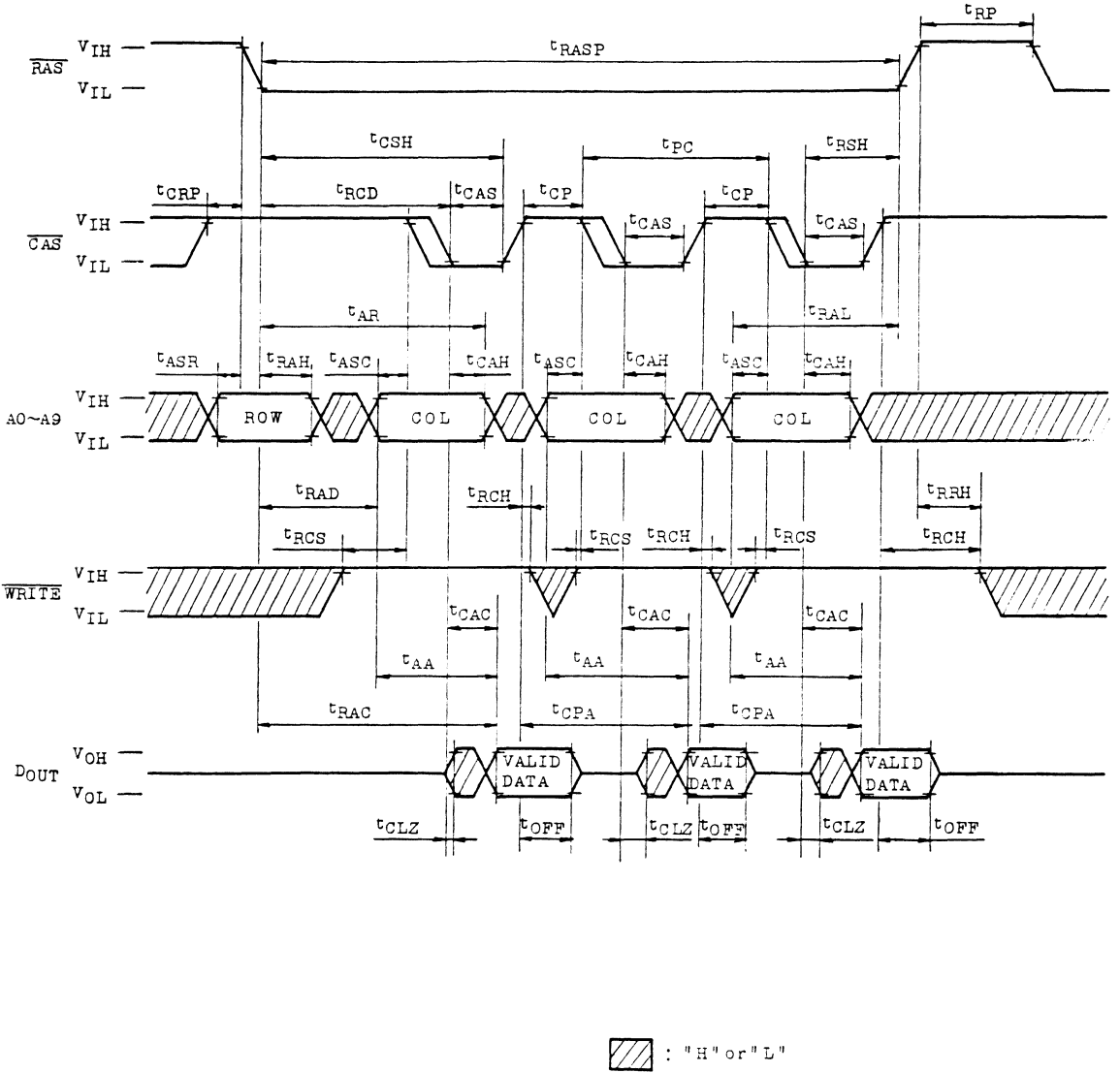


NOTE: "TF" pin should be connected to  $V_{IL}$  level or open, if "Test Mode" is not used.



# TC511000P/J/Z-85, TC511000P/J/Z-10 TC511000P/J/Z-12

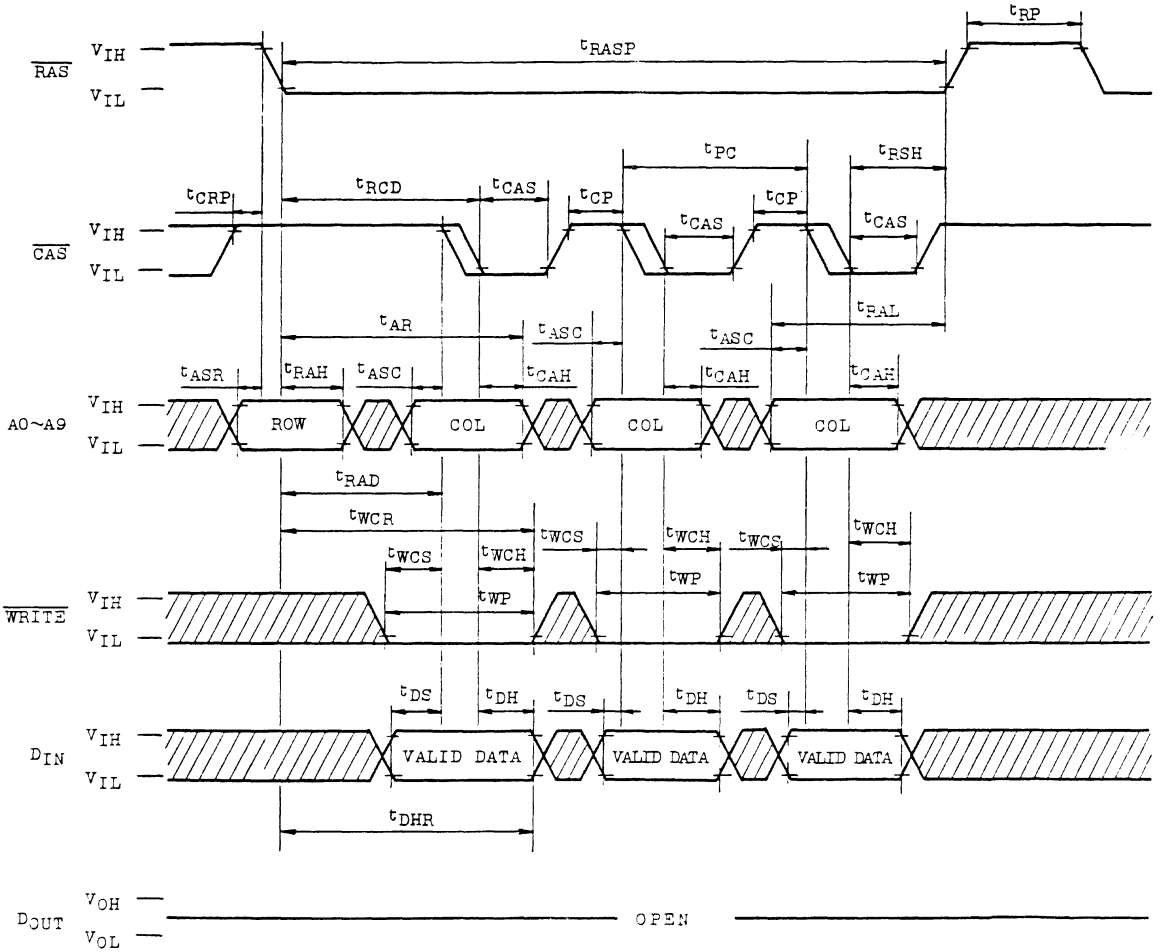
## FAST PAGE MODE READ CYCLE




NOTE: "TF" pin should be connected to  $V_{IL}$  level or open, if "Test Mode" is not used.

# TC511000P/J/Z-85, TC511000P/J/Z-10 TC511000P/J/Z-12

## FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

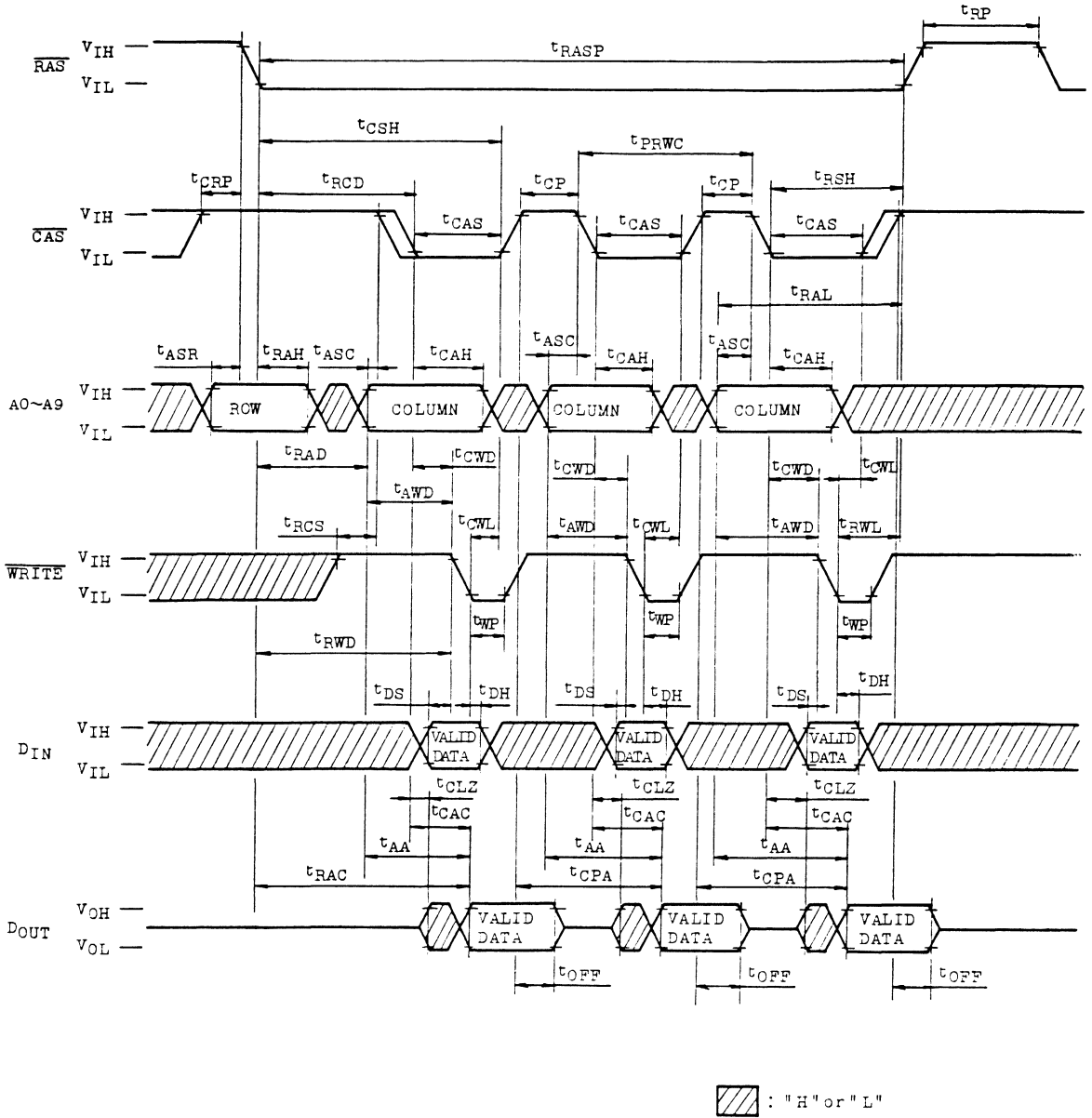


 : "H" or "L"

NOTE: "TF" pin should be connected to  $V_{IL}$  level or open, if "Test Mode" is not used.

# TC51100P/J/Z-85, TC51100P/J/Z-10 TC51100P/J/Z-12

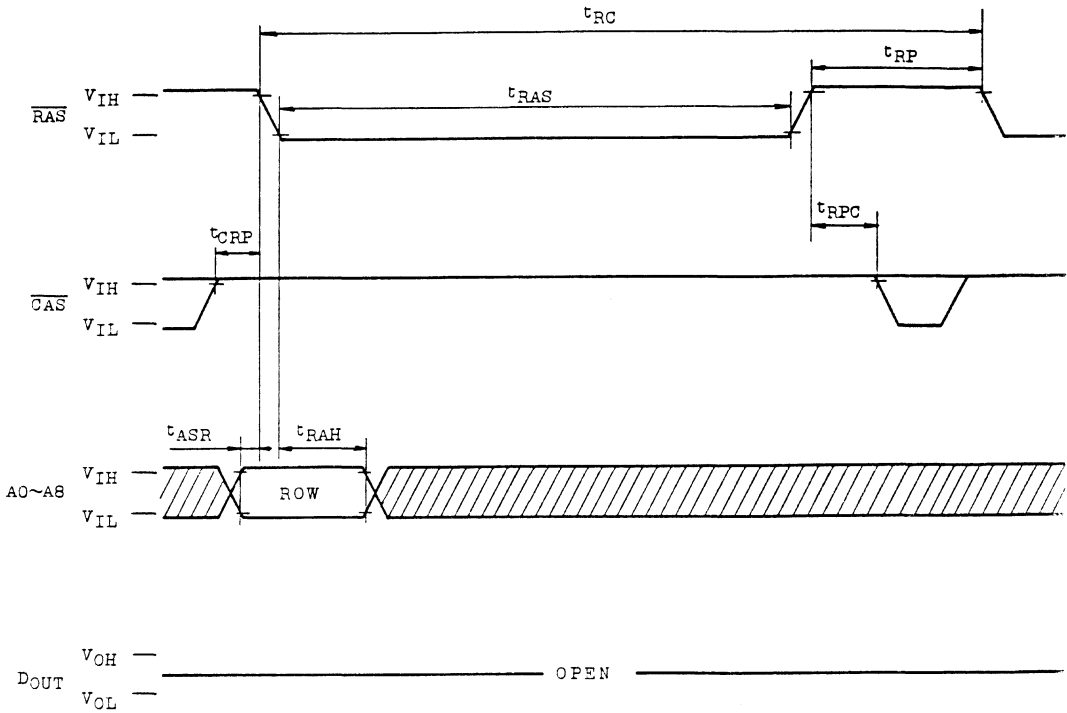
## FAST PAGE MODE READ-WRITE CYCLE




NOTE: "TF" pin should be connected to  $V_{IL}$  level or open, if "Test Mode" is not used.

**TC511000P/J/Z-85, TC511000P/J/Z-10  
TC511000P/J/Z-12**

RAS ONLY REFRESH CYCLE



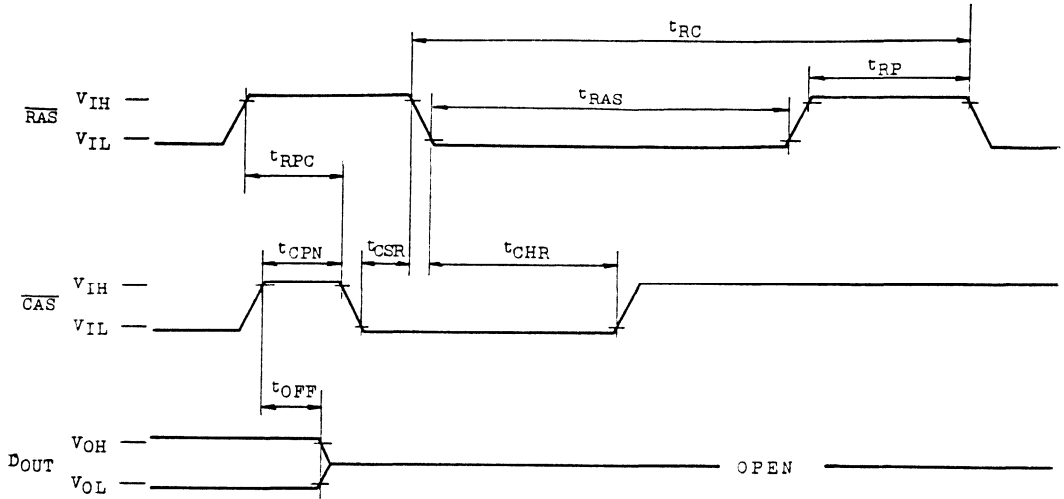
 : "H" or "L"


NOTE:  $\overline{\text{WRITE}}$ ="H" or "L",  $\text{A9}$ ="H" or "L"

"TF" pin should be connected to  $V_{IL}$  level or open, if "Test Mode" is not used.

**TC511000P/J/Z-85, TC511000P/J/Z-10  
TC511000P/J/Z-12**

CAS BEFORE RAS REFRESH CYCLE



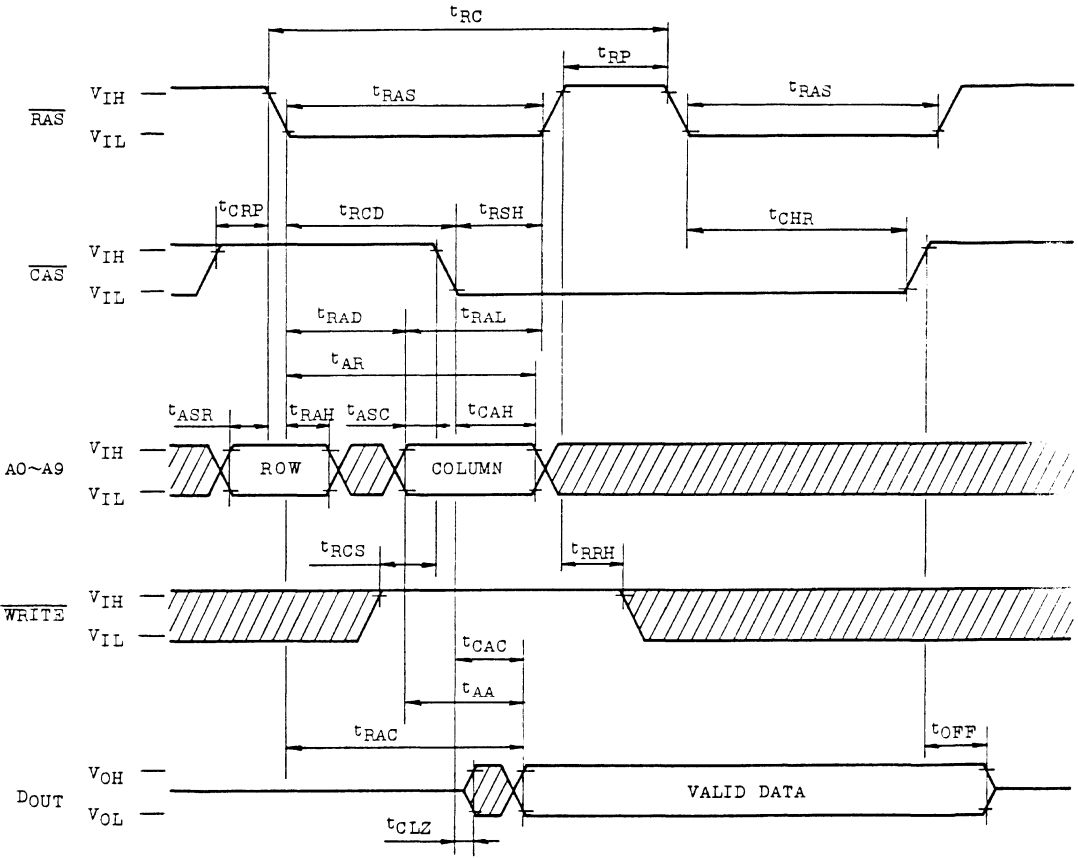
 : "H" or "L"


NOTE:  $\overline{WRITE}$ ="H" or "L", A0 ~ A9="H" or "L"

"TF" pin should be connected to  $V_{IL}$  level or open, if "Test Mode" is not used.

**TC511000P/J/Z-85, TC511000P/J/Z-10  
TC511000P/J/Z-12**

HIDDEN REFRESH CYCLE (READ)

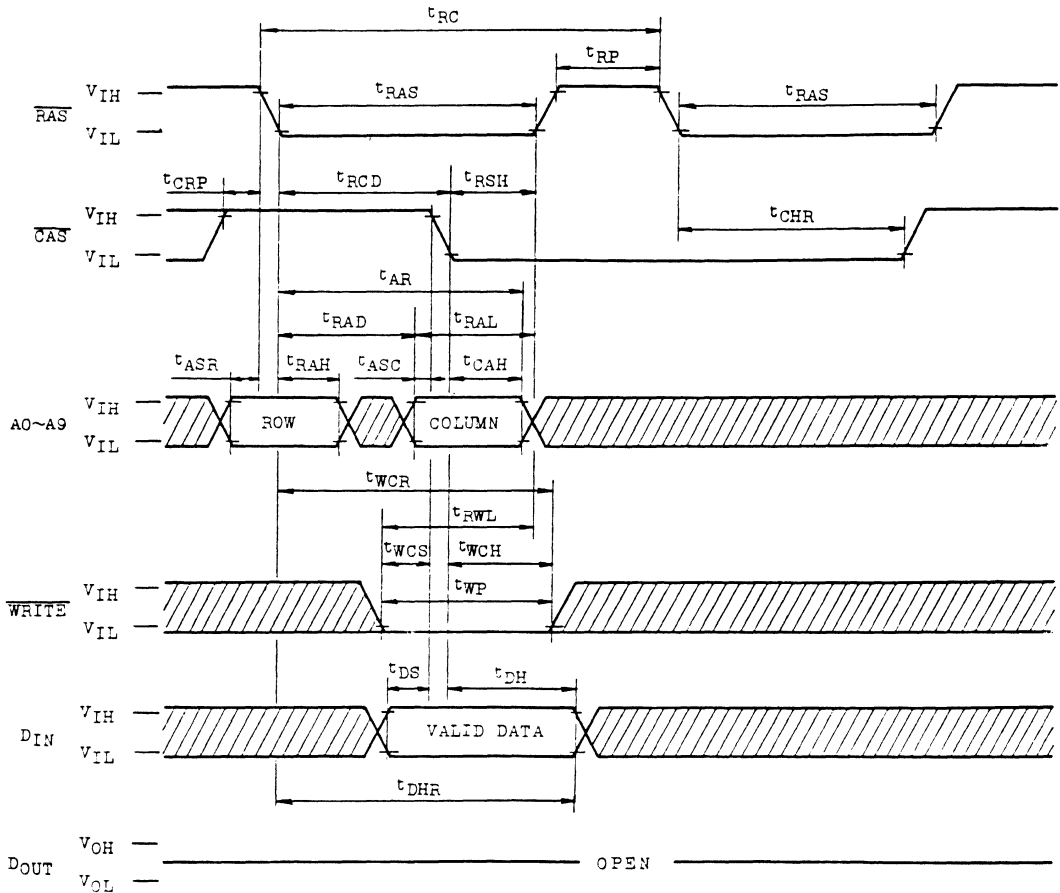


 : "H" or "L"

NOTE: "TF" pin should be connected to V<sub>IL</sub> level or open, if "Test Mode" is not used.

# TC51100P/J/Z-85, TC51100P/J/Z-10 TC51100P/J/Z-12

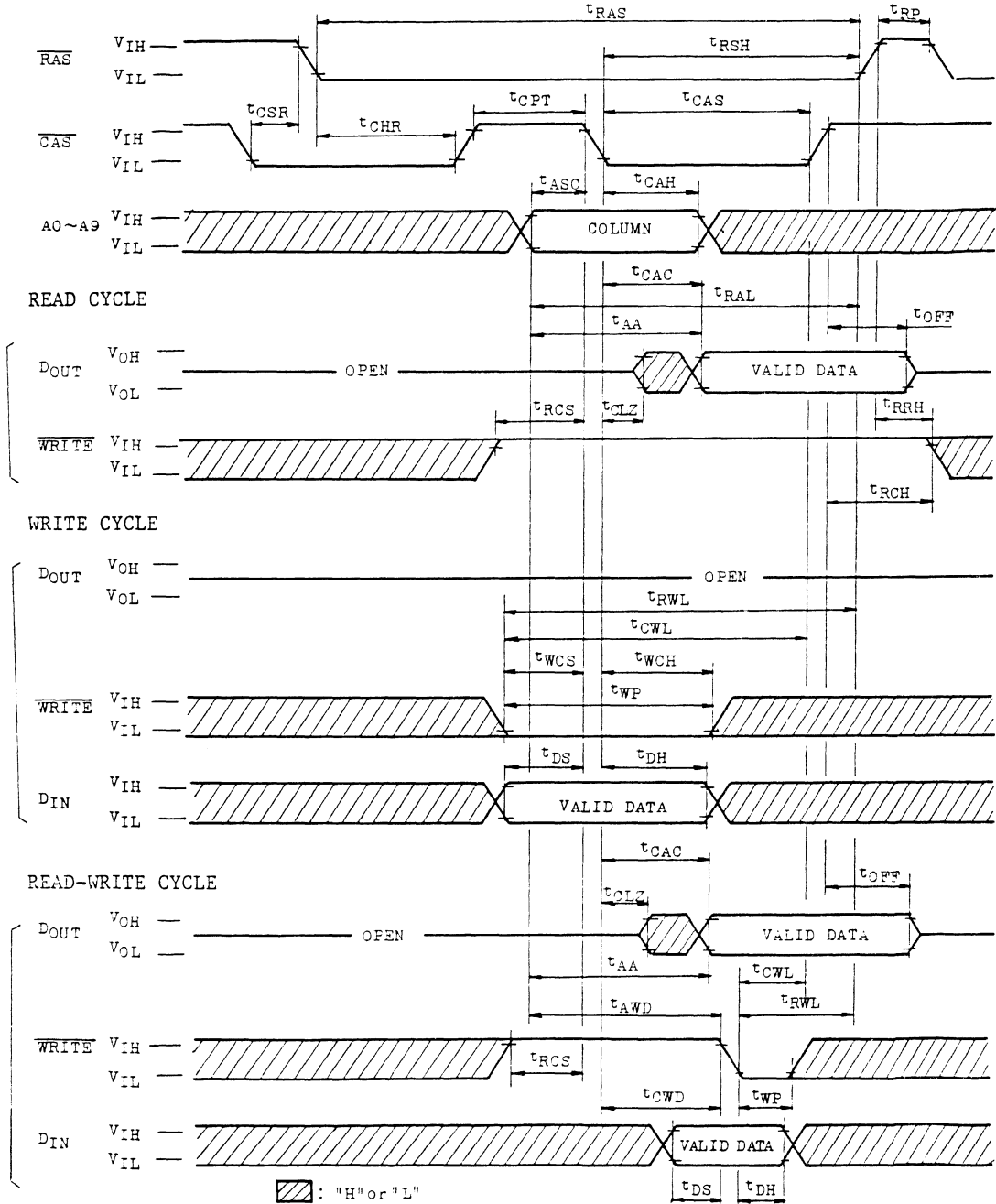
## HIDDEN REFRESH CYCLE (WRITE)



NOTE: "TF" pin should be connected to  $V_{IL}$  level or open, if "Test Mode" is not used.

# TC511000P/J/Z-85, TC511000P/J/Z-10 TC511000P/J/Z-12

CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



NOTE: "TF" pin should be connected  $V_{IL}$  level or open, if "Test Mode" is not used.



# TC511000P/J/Z-85, TC511000P/J/Z-10 TC511000P/J/Z-12

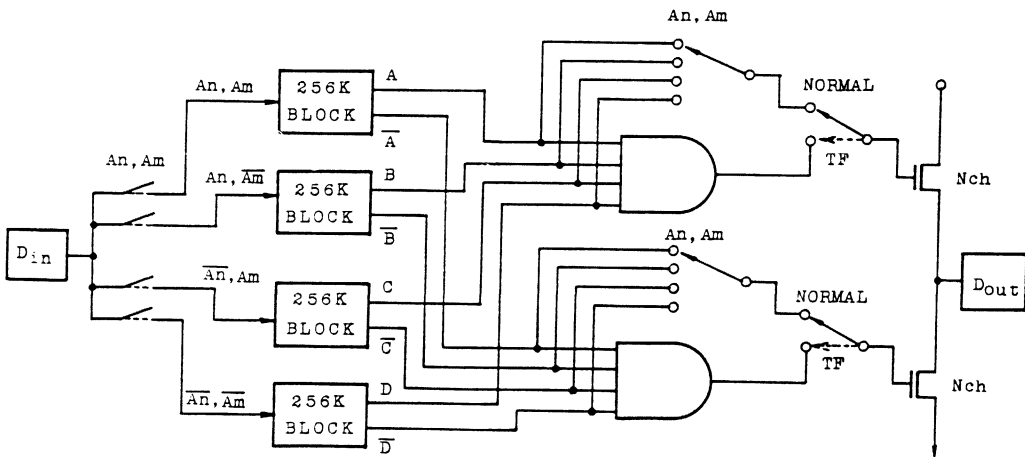
## DESCRIPTION OF THE TEST MODE FOR 1M DRAMS

The TC511000/1/2 is a CMOS DRAM organized as 1,048,576 words by 1-bit. It is internally organized as 262,144 words by 4-bits.

The "Test Mode" function allows for a 1M DRAM to be tested virtually as if it were a 256K DRAM. Figure 1 shows the block diagram of the "Test Mode" circuit. Data is written into the four 256K blocks in parallel and is retrieved the same way. A logical "and" operation is performed on the outputs of the four internal 256K blocks.

- o For a good device, the output data of the four internal blocks are identical to the input data (all "H" or all "L") and consequently the same data will appear on the output pin.
- o For a bad device, the output data of one or more of the internal blocks will differ from the input data and a high impedance state will be detected on the output pin.

### Block Diagram in Test Mode



TF Pin = Super voltage; Test Mode  
TF Pin = Low level or Hi-Z; Normal

### Truth Table in Test mode Function

A	B	C	D	DOUT
0	0	0	0	0
1	1	1	1	1
otherwise				Hi-Z

Fig. 1

# TC511000P/J/Z-85, TC511000P/J/Z-10 TC511000P/J/Z-12

## DESCRIPTION OF THE TEST MODE FOR 1M DRAMS (CONTINUED)

The "Test Mode" function is enabled by applying a "Super Voltage" ( $V_{CC}+4.5V$ , max. voltage=10.5V) on the "TF" pin for a specified period ( $t_{TES}$  and  $t_{TEH}$  as shown in figure 2). It can be used while operating in any mode, including static column mode. It achieves a 4:1 reduction in test time for N patterns and a 16:1 reduction in test time for  $N^2$  patterns. The A9 address input is ignored during the "Test Mode".

During normal operation or when the "Test Mode" function is not used, the "TF" pin must be connected to VSS or TTL Logic Low Level, or left unconnected on the printed wiring board.

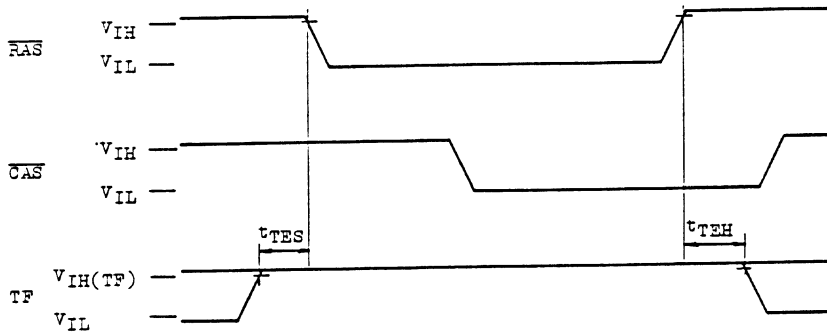
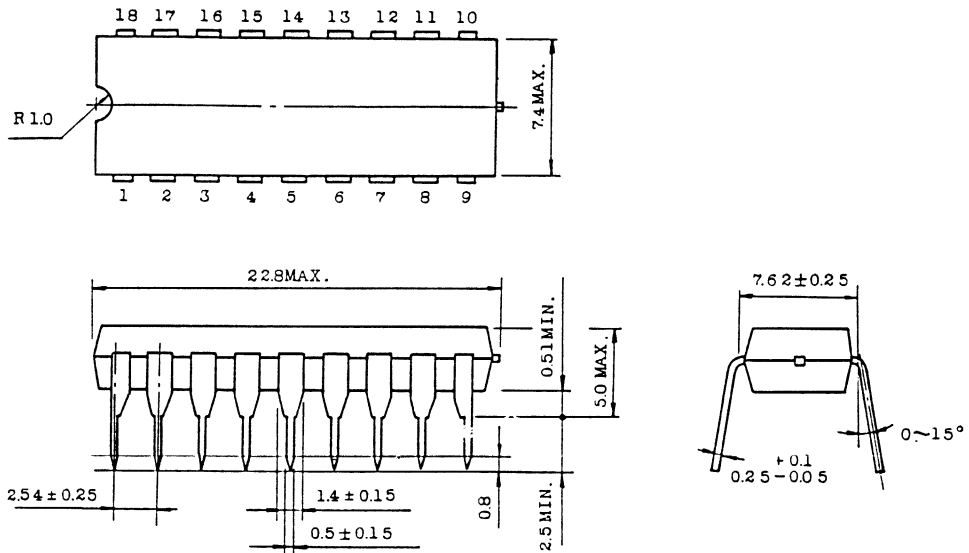


Fig.2 Test Mode Cycle

# TC511000P/J/Z-85, TC511000P/J/Z-10 TC511000P/J/Z-12

• Plastic DIP

Unit in mm



Note: Each lead pitch is 2.54mm.

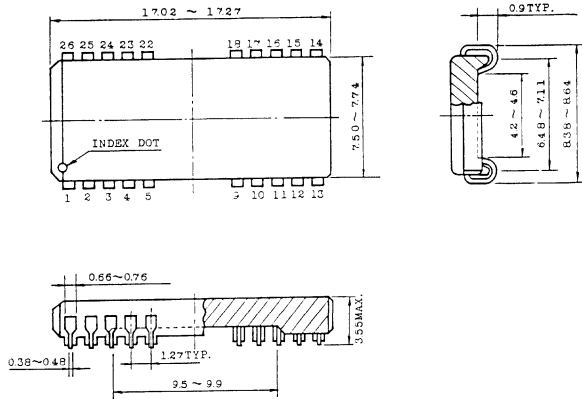
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.18 leads.

All dimensions are in millimeters.

# TC511000P/J/Z-85, TC511000P/J/Z-10 TC511000P/J/Z-12

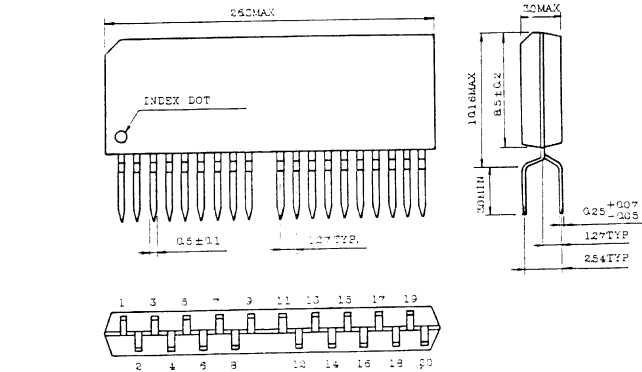
• Plastic SOJ

Unit in mm



• Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.

All dimensions are in millimeters.

Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

# TOSHIBA MOS MEMORY PRODUCT

1,048,576 WORDS × 1 BIT DYNAMIC RAM  
SILICON GATE CMOS

TC511001P/J/Z-85, TC511001P/J/Z-10  
TC511001P/J/Z-12

## DESCRIPTION

The TC511001P/J/Z is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511001P/J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511001P/J/Z to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. The special feature of TC511001P/J/Z is nibble mode, allowing the user to serially access 4 bits of data at a high data rate. "Test Mode" function is implemented from Revision C.

## FEATURES

- 1,048,576 words by 1 bit organization
- Fast access time and cycle time

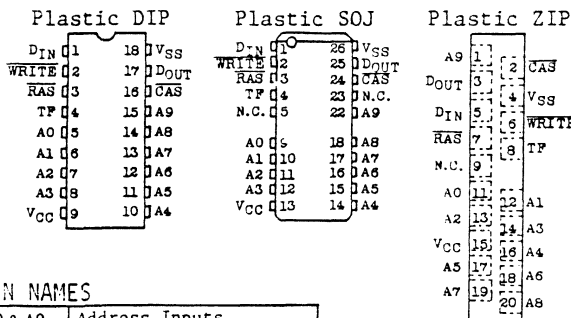
		TC511001P/J/Z-85-10-12		
t <sub>RAC</sub>	RAS Access Time	85ns	100ns	120ns
t <sub>AA</sub>	Column Address Access Time	45ns	50ns	60ns
t <sub>CAC</sub>	CAS Access Time	30ns	35ns	40ns
t <sub>RC</sub>	Cycle Time	165ns	190ns	220ns
t <sub>NCAC</sub>	Nibble Mode Access Time	20ns	20ns	25ns
t <sub>NC</sub>	Nibble Mode Cycle Time	40ns	40ns	50ns

- Single power supply of 5V±10% with a built-in V<sub>BB</sub> generator

- Low Power:
  - 385mW MAX. Operating (TC511001P/J/Z-85)
  - 330mW MAX. Operating (TC511001P/J/Z-10)
  - 275mW MAX. Operating (TC511001P/J/Z-12)
  - 5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, CAS before RAS refresh, RAS-only refresh, Hidden refresh, Nibble Mode and Test Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms

- Package Plastic DIP: TC511001P  
Plastic SOJ: TC511001J  
Plastic ZIP: TC511001Z

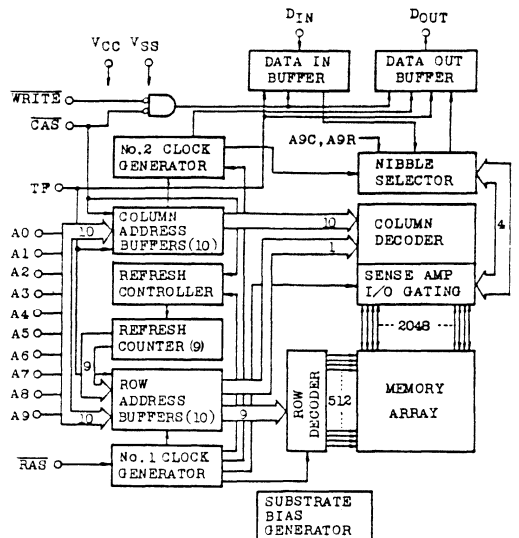
## PIN CONNECTION (TOP VIEW)



## PIN NAMES

A0 ~ A9	Address Inputs
CAS	Column Address Strobe
DIN	Data In
DOUT	Data Out
RAS	Row Address Strobe
WRITE	Read/Write Input
VCC	Power (+5V)
VSS	Ground
TF	Test Function
N.C.	No Connection

## BLOCK DIAGRAM



# TC511001P/J/Z-85, TC511001P/J/Z-10 TC511001P/J/Z-12

## ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V <sub>IN</sub>	-1 ~ 7	V	1
Test Mode Input Voltage	V <sub>IN</sub> (TF)	-1 ~ 10.5	V	1
Output Temperature	V <sub>OUT</sub>	-1 ~ 7	V	1
Power Supply Voltage	V <sub>CC</sub>	-1 ~ 7	V	1
Operating Temperature	T <sub>OPR</sub>	0 ~ 70	°C	1
Storage Temperature	T <sub>STG</sub>	-55 ~ 150	°C	1
Soldering Temperature · Time	T <sub>SOLDER</sub>	260 · 10	°C·sec	1
Power Dissipation	P <sub>D</sub>	600	mW	1
Short Circuit Output Current	I <sub>OUT</sub>	50	mA	1

## RECOMMENDED DC OPERATING CONDITIONS (T<sub>a</sub>=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V	2
V <sub>IH</sub>	Input High Voltage	2.4	-	6.5	V	2
V <sub>IL</sub>	Input Low Voltage	-1.0	-	0.8	V	2
V <sub>IH</sub> (TF)	Test Enable Input High Voltage	V <sub>CC</sub> +4.5	-	10.5	V	2

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5±10%, T<sub>a</sub>=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES	
I <sub>CC1</sub>	OPERATING CURRENT Average Power Supply Operating Current ( $\overline{RAS}$ , $\overline{CAS}$ , Address Cycling: t <sub>RC</sub> =t <sub>RC</sub> MIN.)	TC511001P/J/Z-85	-	70	mA	3,
		TC511001P/J/Z-10	-	60	mA	
		TC511001P/J/Z-12	-	50	mA	
I <sub>CC2</sub>	STANDBY CURRENT Power Supply Standby Current ( $\overline{RAS}=\overline{CAS}=V_{IH}$ )		-	2	mA	3
I <sub>CC3</sub>	RAS ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ( $\overline{RAS}$ Cycling, $\overline{CAS}=V_{IH}$ : t <sub>RC</sub> =t <sub>RC</sub> MIN.)	TC511001P/J/Z-85	-	70	mA	3
		TC511001P/J/Z-10	-	60	mA	
		TC511001P/J/Z-12	-	50	mA	
I <sub>CC4</sub>	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ( $\overline{RAS}=V_{IL}$ , $\overline{CAS}$ Cycling: t <sub>NC</sub> =t <sub>NC</sub> MIN.)	TC511001P/J/Z-85	-	50	mA	3,4
		TC511001P/J/Z-10	-	40	mA	
		TC511001P/J/Z-12	-	30	mA	
I <sub>CC5</sub>	STANDBY CURRENT Power Supply Standby Current ( $\overline{RAS}=\overline{CAS}=V_{CC}-0.2V$ )		-	1	mA	
I <sub>CC6</sub>	CAS BEFORE RAS REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ( $\overline{RAS}$ , $\overline{CAS}$ Cycling: t <sub>RC</sub> =t <sub>RC</sub> MIN.)	TC511001P/J/Z-85	-	70	mA	3
		TC511001P/J/Z-10	-	60	mA	
		TC511001P/J/Z-12	-	50	mA	
I <sub>I(L)</sub>	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input (0V ≤ V <sub>IN</sub> ≤ 6.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
I <sub>ITF(L)</sub>	INPUT LEAKAGE CURRENT (only TF) (0V ≤ V <sub>IN</sub> (TF) ≤ 0.8V, All Other Pins Not Under Test = 0V)		-10	10	μA	
I <sub>O(L)</sub>	OUTPUT LEAKAGE CURRENT (DOUT is disabled, 0V ≤ V <sub>OUT</sub> ≤ +5.5V)		-10	10	μA	
I <sub>TF</sub>	TEST FUNCTION INPUT CURRENT (V <sub>CC</sub> +4.5V ≤ V <sub>IN</sub> (TF) ≤ 10.5V)		-	1	mA	
V <sub>OH</sub>	OUTPUT LEVEL Output "H" Level Voltage (I <sub>OUT</sub> =-5mA)		2.4	-	V	
V <sub>OL</sub>	OUTPUT LEVEL Output "L" Level Voltage (I <sub>OUT</sub> =4.2mA)		-	0.4	V	

# TC511001P/J/Z-85, TC511001P/J/Z-10 TC511001P/J/Z-12

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V<sub>CC</sub>=5V±10%, Ta=0 ~ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC511001P/J/Z-85		TC511001P/J/Z-10		TC511001P/J/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t <sub>RC</sub>	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t <sub>RWC</sub>	Read-Write Cycle Time	190	-	220	-	255	-	ns	
t <sub>NC</sub>	Nibble Mode Cycle Time	40	-	40	-	50	-	ns	
t <sub>NRMW</sub>	Nibble Mode Read-Write Cycle Time	65	-	65	-	80	-	ns	
t <sub>RAC</sub>	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
t <sub>CAC</sub>	Access Time from $\overline{CAS}$	-	30	-	35	-	40	ns	8,13
t <sub>AA</sub>	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
t <sub>NCAC</sub>	Nibble Mode Access Time	-	20	-	20	-	25	ns	8
t <sub>CLZ</sub>	$\overline{CAS}$ to Output in Low-Z	.5	-	5	-	5	-	ns	8
t <sub>OFF</sub>	Output Buffer Turn-Off Delay	0	30	0	30	0	35	ns	9
t <sub>T</sub>	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t <sub>RP</sub>	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t <sub>RAS</sub>	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t <sub>RSH</sub>	$\overline{RAS}$ Hold Time	30	-	35	-	40	-	ns	
t <sub>CSH</sub>	$\overline{CAS}$ Hold Time	85	-	100	-	120	-	ns	
t <sub>CAS</sub>	$\overline{CAS}$ Pulse Width	30	10,000	35	10,000	40	10,000	ns	
t <sub>RCD</sub>	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	25	65	25	80	ns	13
t <sub>RAD</sub>	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t <sub>CRP</sub>	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t <sub>CPN</sub>	$\overline{CAS}$ Precharge Time	15	-	15	-	20	-	ns	
t <sub>ASR</sub>	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t <sub>RAH</sub>	Row Address Hold Time	15	-	15	-	15	-	ns	
t <sub>ASC</sub>	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t <sub>CAH</sub>	Column Address Hold Time	20	-	20	-	25	-	ns	
t <sub>AR</sub>	Column Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t <sub>RAL</sub>	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	
t <sub>RCS</sub>	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t <sub>RCH</sub>	Read Command Hold Time referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	10
t <sub>RRH</sub>	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t <sub>WCH</sub>	Write Command Hold Time	20	-	20	-	25	-	ns	
t <sub>WCR</sub>	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	

# TC511001P/J/Z-85, TC511001P/J/Z-10 TC511001P/J/Z-12

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC511001P/J/Z-85		TC511001P/J/Z-10		TC511001P/J/Z-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t <sub>WP</sub>	Write Command Pulse Width	20	-	20	-	25	-	ns	
t <sub>RWL</sub>	Write Command to $\overline{\text{RAS}}$ Lead Time	20	-	25	-	30	-	ns	
t <sub>CWL</sub>	Write Command to $\overline{\text{CAS}}$ Lead Time	20	-	25	-	30	-	ns	
t <sub>DS</sub>	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
t <sub>DH</sub>	Data-In Hold Time	20	-	20	-	25	-	ns	11
t <sub>DHR</sub>	Data-In Hold Time reference to $\overline{\text{RAS}}$	65	-	75	-	90	-	ns	
t <sub>REF</sub>	Refresh Period	-	8	-	8	-	8	ms	
t <sub>WCS</sub>	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t <sub>CWD</sub>	$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ Delay Time	30	-	35	-	40	-	ns	12
t <sub>RWD</sub>	$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ Delay Time	85	-	100	-	120	-	ns	12
t <sub>AWD</sub>	Column Address to $\overline{\text{WRITE}}$ Delay Time	45	-	50	-	60	-	ns	12
t <sub>CSR</sub>	$\overline{\text{CAS}}$ Set-Up Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	10	-	10	-	10	-	ns	
t <sub>CHR</sub>	$\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	30	-	30	-	30	-	ns	
t <sub>RPC</sub>	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	0	-	0	-	0	-	ns	
t <sub>CPT</sub>	$\overline{\text{CAS}}$ Precharge Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Counter Test)	50	-	50	-	60	-	ns	
t <sub>NCAS</sub>	Nibble Mode Pulse Width	20	-	20	-	25	-	ns	
t <sub>NCP</sub>	Nibble Mode $\overline{\text{CAS}}$ Precharge Time	10	-	10	-	15	-	ns	
t <sub>NRSH</sub>	Nibble Mode $\overline{\text{RAS}}$ Hold Time	20	-	20	-	25	-	ns	
t <sub>NCWD</sub>	Nibble Mode $\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ Delay Time	20	-	20	-	25	-	ns	
t <sub>NRWL</sub>	Nibble Mode $\overline{\text{WRITE}}$ Command to $\overline{\text{RAS}}$ Lead Time	20	-	20	-	25	-	ns	
t <sub>NCWL</sub>	Nibble Mode $\overline{\text{WRITE}}$ Command to $\overline{\text{CAS}}$ Lead Time	20	-	20	-	25	-	ns	
t <sub>TES</sub>	Test Mode Enable Set-Up Time referenced to $\overline{\text{RAS}}$	0	-	0	-	0	-	ns	
t <sub>TEH</sub>	Test Mode Enable Hold Time referenced to $\overline{\text{RAS}}$	0	-	0	-	0	-	ns	

CAPACITANCE ( $V_{CC}=5V\pm 10\%$ ,  $f=1\text{MHz}$ ,  $T_a=0\sim 70^\circ\text{C}$ )

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C11	Input Capacitance ( $A_0\sim A_9$ , $D_{IN}$ )	-	5	pF
C12	Input Capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WRITE}}$ , $\text{TF}$ )	-	7	pF
C0	Output Capacitance ( $D_{OUT}$ )	-	7	pF



# TC511001P/J/Z-85, TC511001P/J/Z-10 TC511001P/J/Z-12

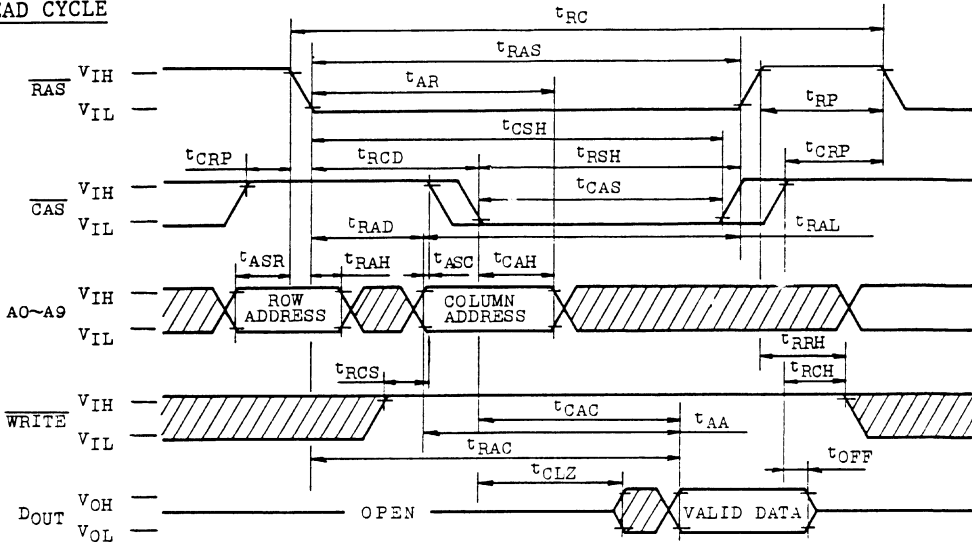
## NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltage are referenced to  $V_{SS}$ .
3.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ ,  $I_{CC6}$  depend on cycle rate.
4.  $I_{CC1}$ ,  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200 $\mu$ s is required after power-up followed by any 8  $\overline{RAS}$  cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{CAS}$  Before  $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
6. AC measurements assume  $t_T=5$ ns.
7.  $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9.  $t_{OFF}(\text{max.})$  defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
11. These parameters are referenced to  $\overline{CAS}$  leading edge in early write cycles and to  $\overline{WRITE}$  leading edge in read-write cycles.
12.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$  and  $t_{AWD} \geq t_{AWD}(\text{min.})$ , the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the  $t_{RCD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled by  $t_{CAC}$ .
14. Operation within the  $t_{RAD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only: If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled by  $t_{AA}$ .

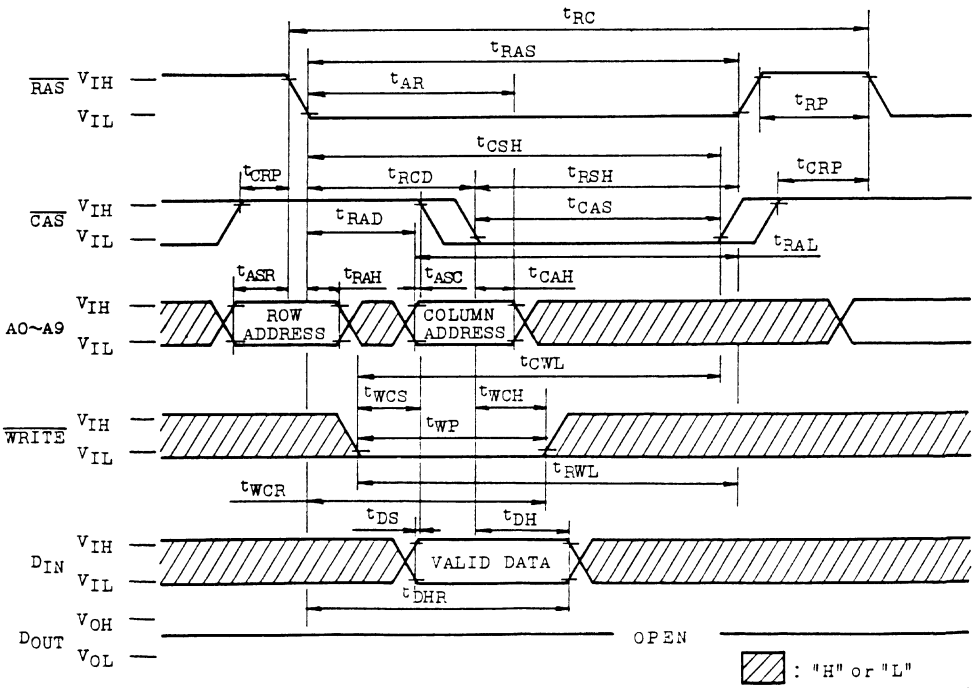
# TC511001P/J/Z-85, TC511001P/J/Z-10 TC511001P/J/Z-12

## TIMING WAVEFORMS

### READ CYCLE



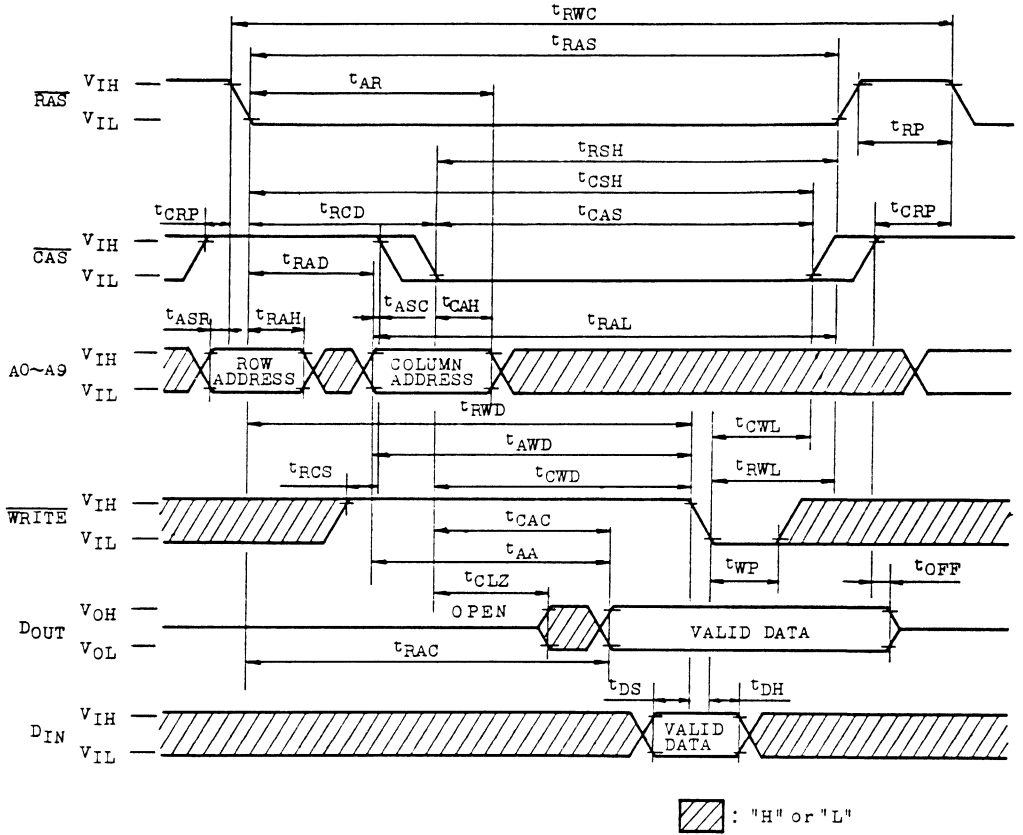
### WRITE CYCLE (EARLY WRITE)



NOTE: "TF" pin should be connected to V<sub>IL</sub> level or open, if "Test Mode" is not used.

# TC511001P/J/Z-85, TC511001P/J/Z-10 TC511001P/J/Z-12

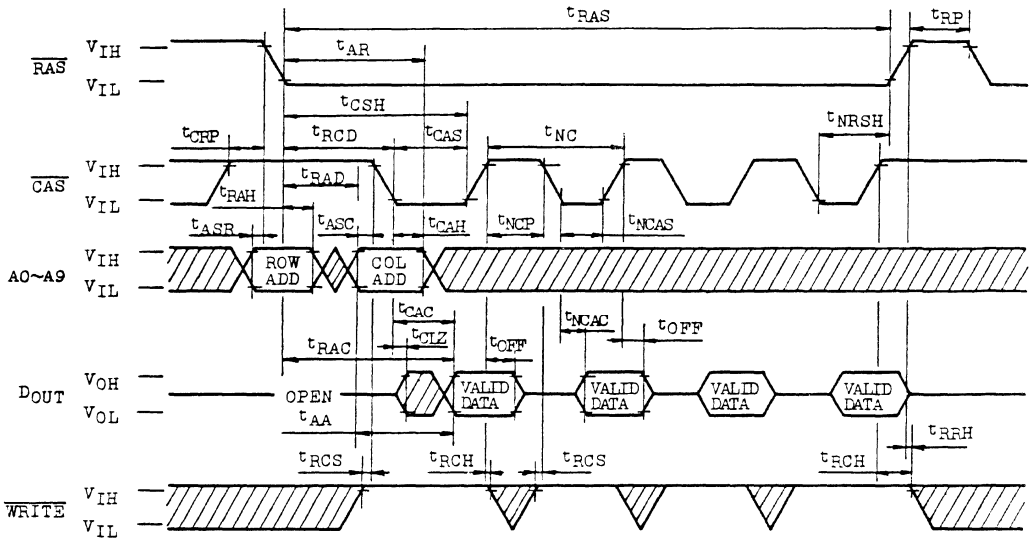
## READ-WRITE CYCLE



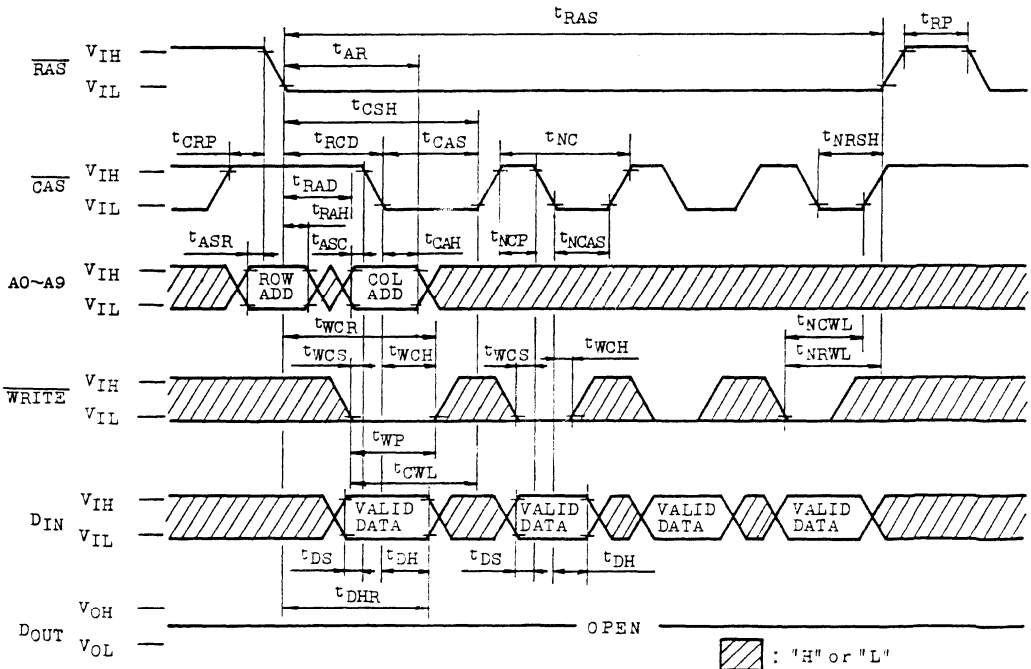
NOTE: "TF" pin should be connected to  $V_{IL}$  level or open, if "Test Mode" is not used.

# TC511001P/J/Z-85, TC511001P/J/Z-10 TC511001P/J/Z-12

## NIBBLE MODE READ CYCLE



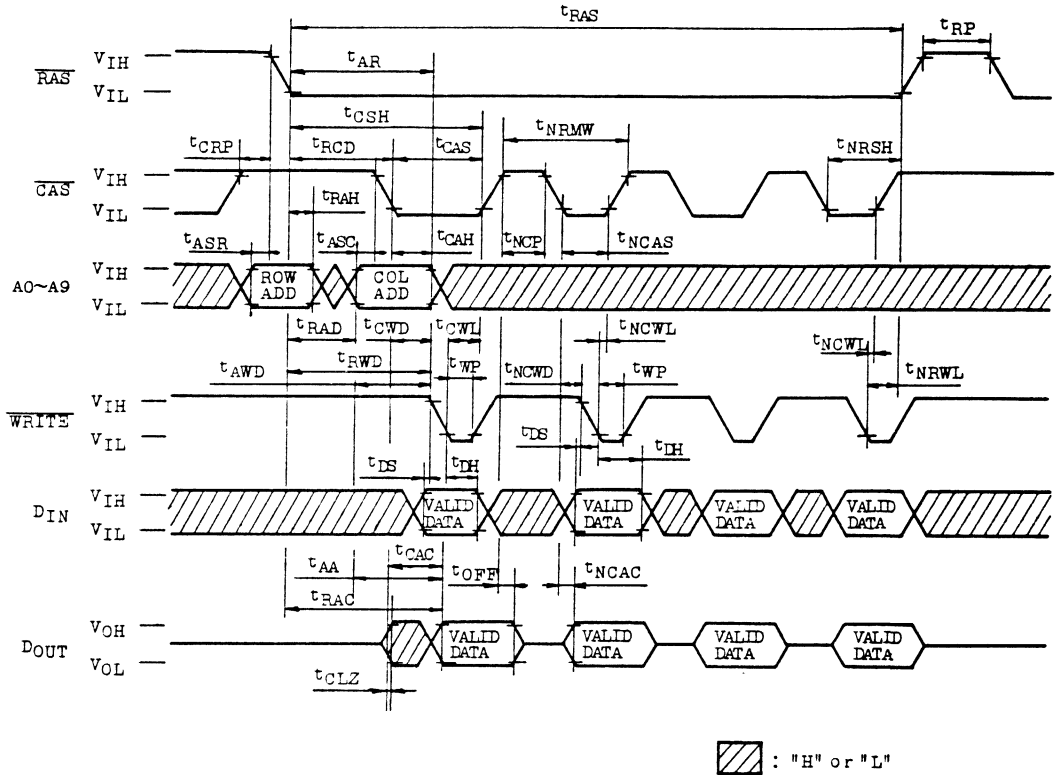
## NIBBLE MODE WRITE CYCLE (EARLY WRITE)



NOTE: "TF" pin should be connected to  $V_{IL}$  level or open.

# TC511001P/J/Z-85, TC511001P/J/Z-10 TC511001P/J/Z-12

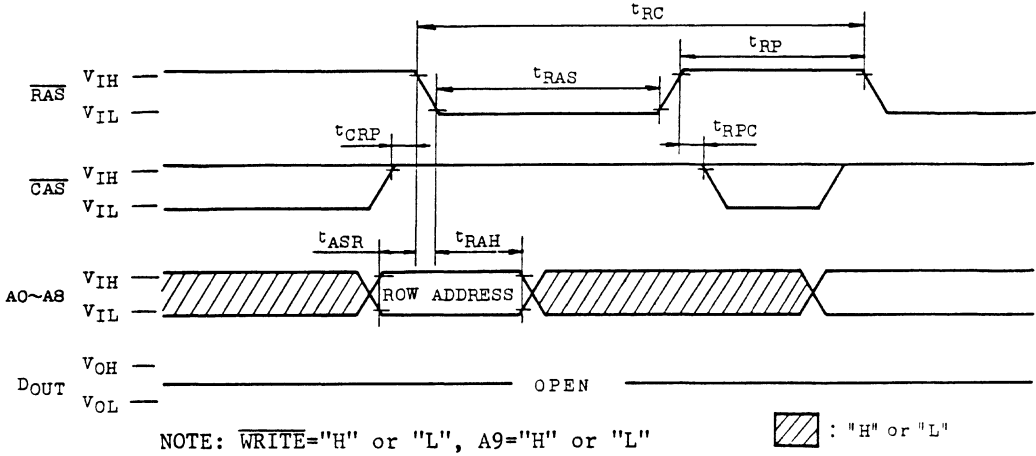
## NIBBLE MODE READ-WRITE CYCLE



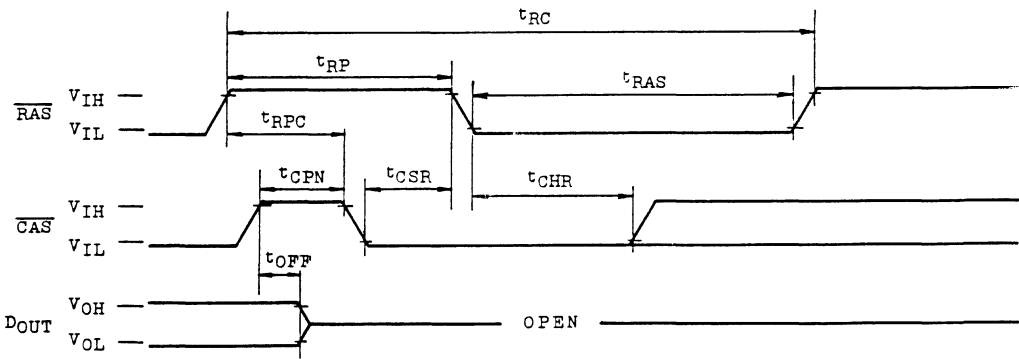
NOTE: "TF" pin should be connected to  $V_{IL}$  level or open.

**TC511001P/J/Z-85, TC511001P/J/Z-10  
TC511001P/J/Z-12**

RAS ONLY REFRESH CYCLE



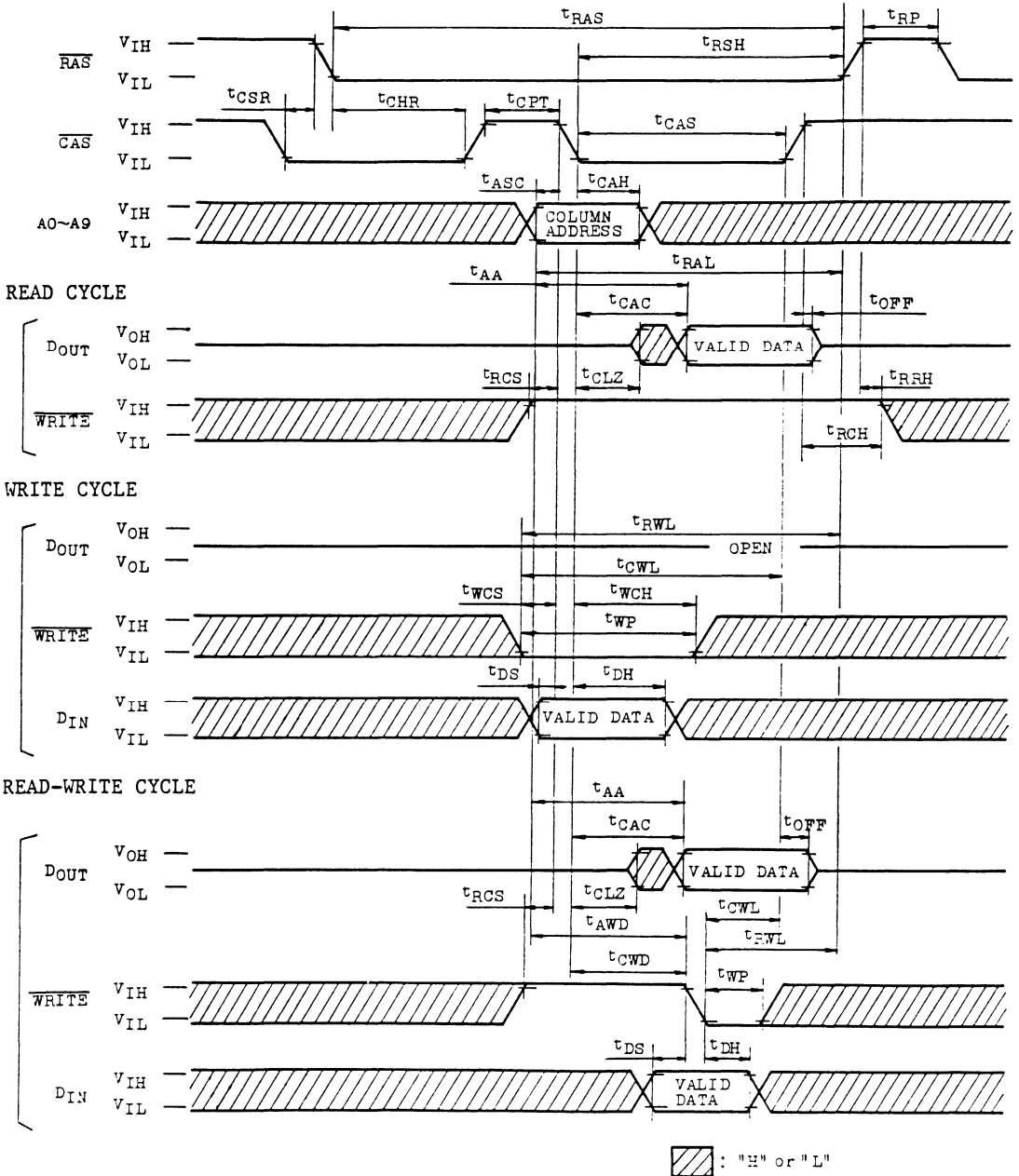
CAS BEFORE RAS REFRESH CYCLE



"TF" pin should be connected to  $V_{IL}$  level or open, if "Test Mode" is not used.

# TC511001P/J/Z-85, TC511001P/J/Z-10 TC511001P/J/Z-12

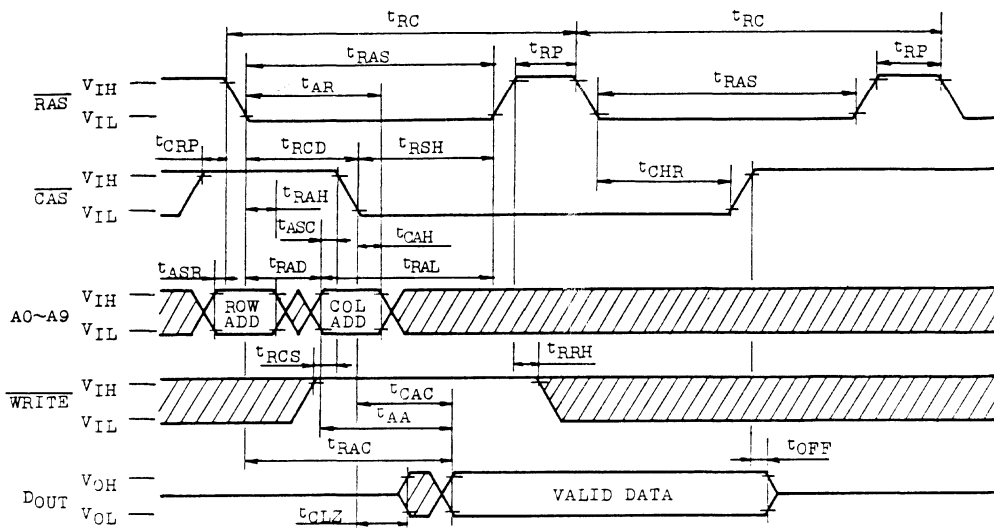
## CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



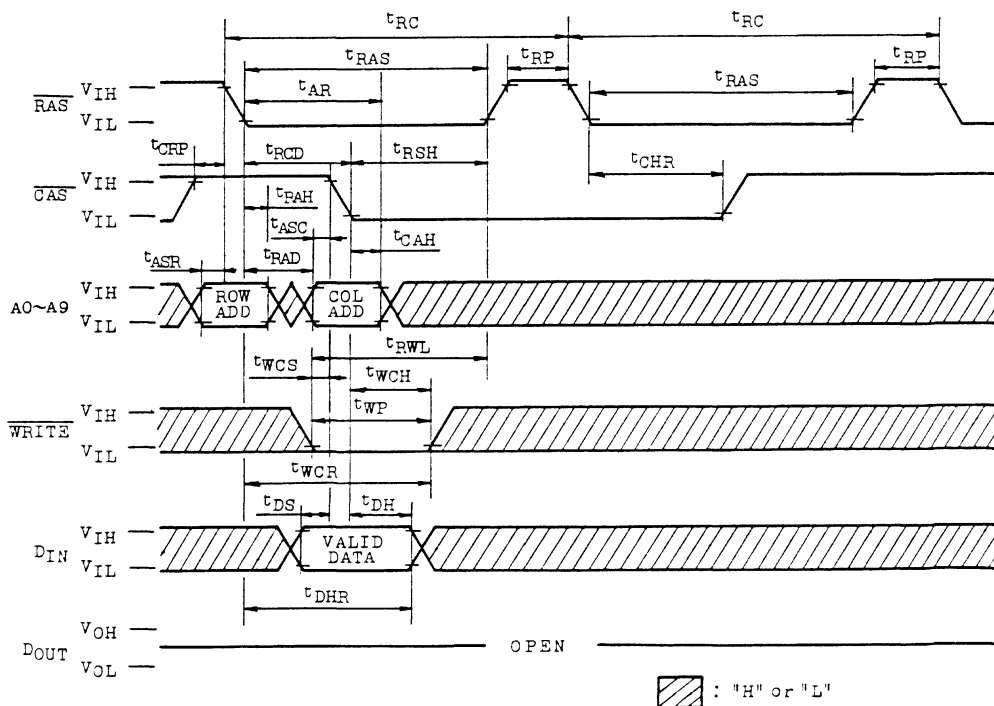
NOTE: "TF" pin should be connected to  $V_{IL}$  level or open, if "Test Mode" is not used.

# TC511001P/J/Z-85, TC511001P/J/Z-10 TC511001P/J/Z-12

## HIDDEN REFRESH CYCLE (READ)



## HIDDEN REFRESH CYCLE (WRITE)



NOTE: "TF" pin should be connected to  $V_{IL}$  level or open, if "Test Mode" is not used.



# TC511001P/J/Z-85, TC511001P/J/Z-10 TC511001P/J/Z-12

## APPLICATION INFORMATION

### ADDRESSING

The 20 address bits required to decode 1 of the 1,048,576 cell locations within the TC511001P/J/Z are multiplexed onto the 10 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ( $\overline{\text{RAS}}$ ), latches the 10 row address bits into the chip. The second clock, the Column Address Strobe ( $\overline{\text{CAS}}$ ), subsequently latches the 10 column address bits into the chip. Each of these signals,  $\overline{\text{RAS}}$ , and  $\overline{\text{CAS}}$ , triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the  $\overline{\text{CAS}}$  clock sequence are inhibited until the occurrence of a delayed signal derived from the  $\overline{\text{RAS}}$  clock chain. This "gated  $\overline{\text{CAS}}$ " feature allows the  $\overline{\text{CAS}}$  clock to be externally activated as soon as the Row Address Hold Time specification ( $t_{\text{RAH}}$ ) has been satisfied and the address inputs have been changed from Row address to Column address information.

### DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of  $\overline{\text{WRITE}}$  and  $\overline{\text{CAS}}$  while  $\overline{\text{RAS}}$  is active. The later of the signals ( $\overline{\text{WRITE}}$  or  $\overline{\text{CAS}}$ ) to make its negative transition is the strobe for the Data In ( $D_{\text{IN}}$ ) register. This permits several options in the write cycle timing. In a write cycle, if the  $\overline{\text{WRITE}}$  input is brought low (active) prior to  $\overline{\text{CAS}}$ , the  $D_{\text{IN}}$  is strobed by  $\overline{\text{CAS}}$  and the set-up and hold times are referenced to  $\overline{\text{CAS}}$ . If the input data is not available at  $\overline{\text{CAS}}$  time or if it is desired that the cycle be a read-write cycle, the  $\overline{\text{WRITE}}$  signal will be delayed until after  $\overline{\text{CAS}}$  has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of  $\overline{\text{WRITE}}$  rather than  $\overline{\text{CAS}}$ . (To illustrate this feature,  $D_{\text{IN}}$  is referenced to  $\overline{\text{WRITE}}$  in the timing diagrams depicting the read-write and nibble mode write cycles while the "early write" cycle diagram shows  $D_{\text{IN}}$  referenced to  $\overline{\text{CAS}}$ ).

Data is retrieved from the memory in a read cycle by maintaining  $\overline{\text{WRITE}}$  in the inactive or high state throughout the portion of the memory cycle in which  $\overline{\text{CAS}}$  is active (low). Data read from the selected cell will be available at the output within the specified access time.

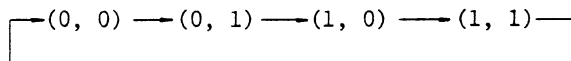
# TC511001P/J/Z-85, TC511001P/J/Z-10 TC511001P/J/Z-12

## DATA OUTPUT CONTROL

The normal condition of the Data Output (D<sub>OUT</sub>) of the TC511001P/J/Z is the high impedance (open circuit) state. This is to say, anytime  $\overline{\text{CAS}}$  is at a high level, the D<sub>OUT</sub> pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D<sub>OUT</sub> will remain valid from access time until  $\overline{\text{CAS}}$  is taken back to the inactive (high level) condition.

## NIBBLE MODE

Nibble mode operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at  $t_{\text{CAC}}$  time. By keeping  $\overline{\text{RAS}}$  low,  $\overline{\text{CAS}}$  can be cycled up and then down, to read or write the next three pages at high data rate (faster than  $t_{\text{CAC}}$ ). Row and column addresses need only be supplied for the first access of the cycles. From then on, the falling edge of  $\overline{\text{CAS}}$  will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Address A<sub>9</sub> determines the starting point of the circular 4 bits nibble. Row A<sub>9</sub> and column A<sub>9</sub> provide the two binary bits needed to select one of four bits. From then on, successive bits come out in a binary fashion; 00 → 01 → 10 → 11 with A<sub>9</sub> row being the least significant address.

A nibble cycle can be a read, write, or delayed write cycle. Any combinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as  $\overline{\text{RAS}}$  is kept low.

## $\overline{\text{RAS}}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 512 row address (A<sub>0</sub> ~ A<sub>8</sub>) within each 8 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with " $\overline{\text{RAS}}$ -only" cycles.

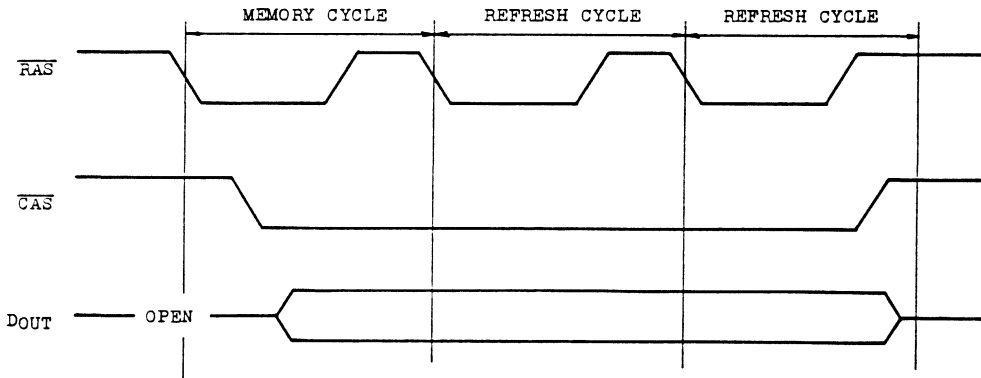
# TC511001P/J/Z-85, TC511001P/J/Z-10 TC511001P/J/Z-12

## $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH

$\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refreshing available on the TC511001P/J/Z offers an alternate refresh method. If  $\overline{\text{CAS}}$  is held on low for the specified period ( $t_{\text{CSR}}$ ) before  $\overline{\text{RAS}}$  goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh operation.

## HIDDEN REFRESH

An optional feature of the TC511001P/J/Z is that refresh cycles may be performed while maintaining valid data at the output pin. This referred to as Hidden Refresh. Hidden Refresh is performed by holding  $\overline{\text{CAS}}$  at  $V_{\text{IL}}$  and taking  $\overline{\text{RAS}}$  high and after a specified precharge period ( $t_{\text{RP}}$ ), executing a  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

# TC511001P/J/Z-85, TC511001P/J/Z-10 TC511001P/J/Z-12

## $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC511001P/J/Z can be tested by  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  cycles as initialization cycles. The test procedure is as follows.

- ① Write "0" into all the memory cells at normal write mode.
- ② Select one certain column address and read "0" out and write "1" in each cell by performing  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 512 times.
- ③ Check "1" out of 512 bits at normal read mode, which was written at ②.
- ④ Using the same column as ②, read "1" out and write "0" in each cell performing  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH COUNTER TEST. Repeat this operation 512 times.
- ⑤ Check "0" out of 512 bits at normal read mode, which was written at ④.
- ⑥ Perform the above ① to ⑤ the complement data.

# TC511001P/J/Z-85, TC511001P/J/Z-10 TC511001P/J/Z-12

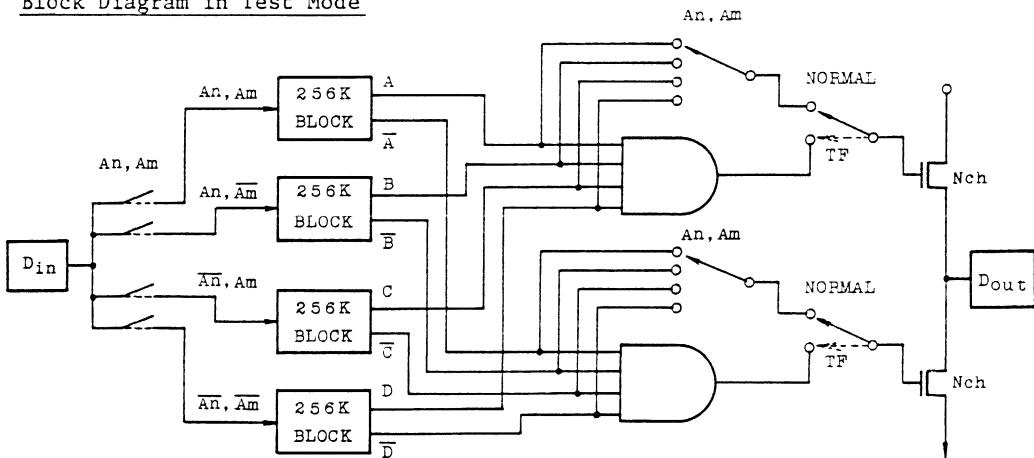
## DESCRIPTION OF THE TEST MODE FOR 1M DRAMS

The TC511000/1/2 is a CMOS DRAM organized as 1,048,576 words by 1-bit. It is internally organized as 262,144 words by 4-bits.

The "Test Mode" function allows for a 1M DRAM to be tested virtually as if it were a 256K DRAM. Figure 1 shows the block diagram of the "Test Mode" circuit. Data is written into the four 256K blocks in parallel and is retrieved the same way. A logical "and" operation is performed on the outputs of the four internal 256K blocks.

- o For a good device, the output data of the four internal blocks are identical to the input data (all "H" or all "L") and consequently the same data will appear on the output pin.
- o For a bad device, the output data of one or more of the internal blocks will differ from the input data and a high impedance state will be detected on the output pin.

### Block Diagram in Test Mode



TF Pin = Super Voltage; Test Mode  
TF Pin = Low Level or Hi-Z; Normal

### Truth Table in Test Mode Function

A	B	C	D	DOUT
0	0	0	0	0
1	1	1	1	1
Otherwise				Hi-Z

Fig. 1

# TC511001P/J/Z-85, TC511001P/J/Z-10 TC511001P/J/Z-12

## DESCRIPTION OF THE TEST MODE FOR 1M DRAMS (CONTINUED)

The "Test Mode" function is enabled by applying a "Super Voltage" ( $V_{CC}+4.5V$ , max. voltage= $10.5V$ ) on the "TF" pin for a specified period ( $t_{TES}$  and  $t_{TEH}$  as shown in figure 2) It can be used while operating in any mode, including static column mode. It achieves a 4:1 reduction in test time for N patterns and a 16:1 reduction in test time for  $N^2$  patterns. The A9 address input is ignored during the "Test Mode"

During normal operation or when the "Test Mode" function is not used, the "TF" pin must be connected to VSS or TTL Logic Low Level, or left unconnected on the printed wiring board.

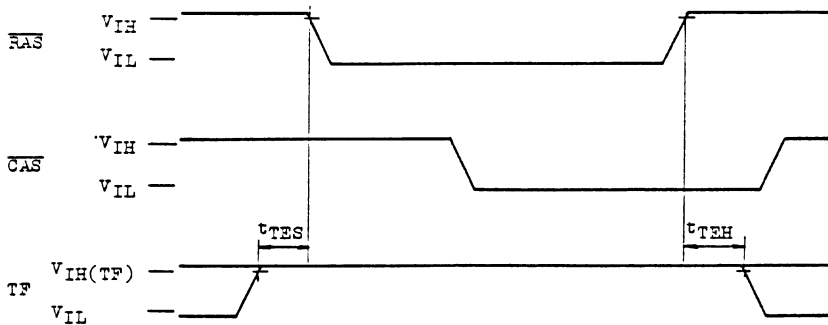


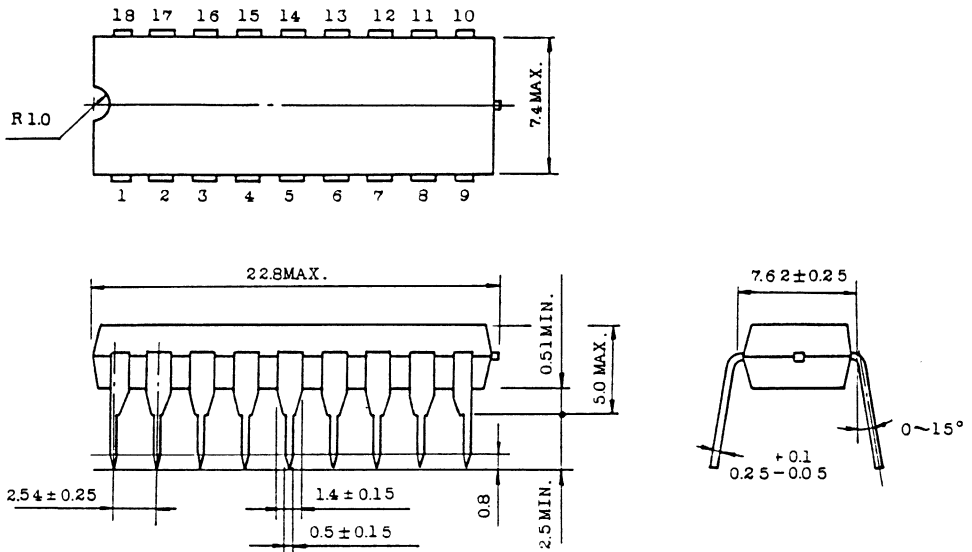
Fig.2 Test Mode Cycle

# TC511001P/J/Z-85, TC511001P/J/Z-10 TC511001P/J/Z-12

## OUTLINE DRAWINGS

- Plastic DIP

Unit in mm



Note: Each lead pitch is 2.54mm.

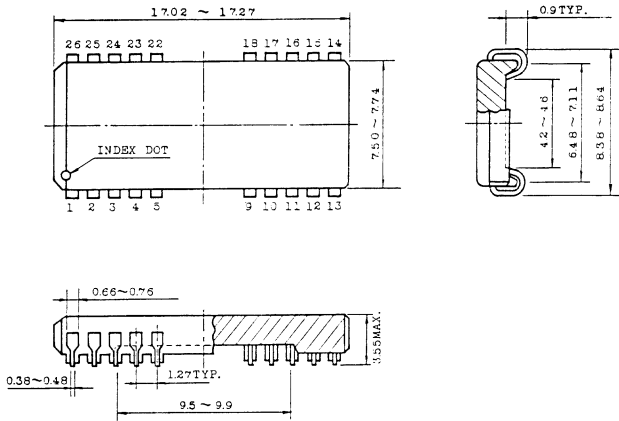
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.18 leads.

All dimensions are in millimeters.

# TC511001P/J/Z-85, TC511001P/J/Z-10 TC511001P/J/Z-12

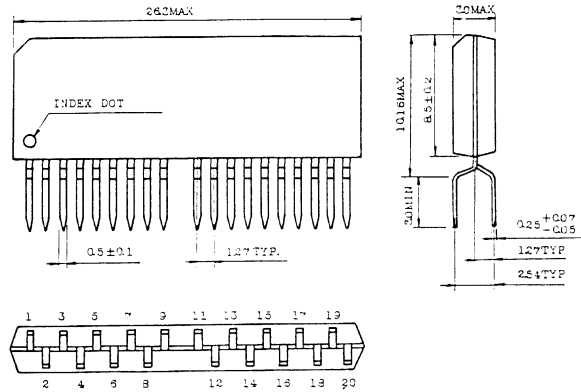
Plastic SOJ

Unit in mm



Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.

All dimensions are in millimeters.

Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.



# TOSHIBA MOS MEMORY PRODUCT

1,048,576 WORDS × 1 BIT DYNAMIC RAM  
SILICON GATE CMOS

TC511002P/J/Z-85, TC511002P/J/Z-10  
TC511002P/J/Z-12

## DESCRIPTION

The TC511002P/J/Z is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511002P/J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511002P/J/Z to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. "Test Mode" function is implemented from Revision C.

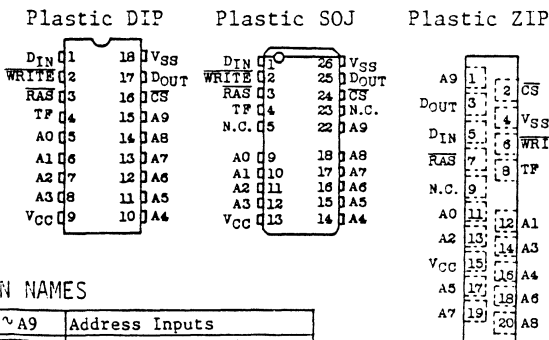
## FEATURES

- 1,048,576 words by 1 bit organization
- Fast access time and cycle time
- Low Power
  - 385mW MAX. Operating (TC511002P/J/Z-85)
  - 330mW MAX. Operating (TC511002P/J/Z-10)
  - 275mW MAX. Operating (TC511002P/J/Z-12)
  - 5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability
- Read-Modify-Write,  $\overline{CS}$  before  $\overline{RAS}$  refresh,  $\overline{RAS}$ -only refresh, Hidden refresh, Static Column Mode and Test Mode capability.
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Package
  - Plastic DIP: TC511002P
  - Plastic SOJ: TC511002J
  - Plastic ZIP: TC511002Z

	TC511002P/J/Z-85-10-12		
$t_{RAC}$ $\overline{RAS}$ Access Time	85ns	100ns	120ns
$t_{AA}$ Column Address Access Time	45ns	50ns	60ns
$t_{CAC}$ $\overline{CS}$ Access Time	25ns	25ns	30ns
$t_{RC}$ Cycle Time	165ns	190ns	220ns
$t_{SC}$ Static Column Mode Cycle Time	50ns	55ns	65ns

- Single power supply of 5V±10% with a built-in  $V_{BB}$  generator

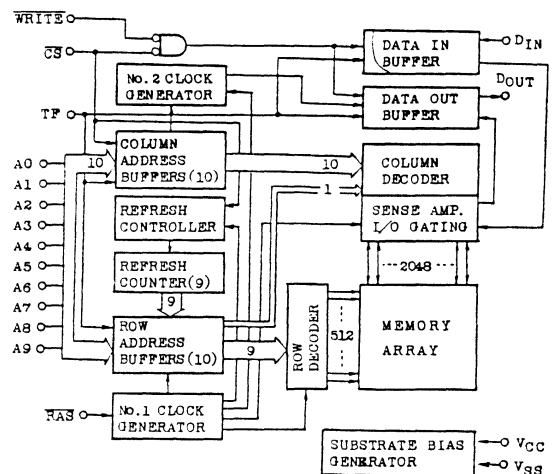
## PIN CONNECTION (TOP VIEW)



## PIN NAMES

A0 ~ A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
DIN	Data In
DOUT	Data Out
$\overline{CS}$	Chip Select Input
WRITE	Read/Write Input
VCC	Power (+5V)
VSS	Ground
TF	Test Function
N.C.	No Connection

## BLOCK DIAGRAM



# TC511002P/J/Z-85, TC511002P/J/Z-10 TC511002P/J/Z-12

## ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V <sub>IN</sub>	-1 ~ 7	V	1
Test Function Input Voltage	V <sub>IN(TF)</sub>	-1 ~ 10.5	V	1
Output Voltage	V <sub>OUT</sub>	-1 ~ 7	V	1
Power Supply Voltage	V <sub>CC</sub>	-1 ~ 7	V	1
Operating Temperature	TOPR	0 ~ 70	°C	1
Storage Temperature	TSTG	-55 ~ 150	°C	1
Soldering Temperature · Time	TSOLDER	260 · 10	°C · sec	1
Power Dissipation	P <sub>D</sub>	600	mW	1
Short Circuit Output Current	I <sub>OUT</sub>	50	mA	1

## RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V	2
V <sub>IH</sub>	Input High Voltage	2.4	-	6.5	V	2
V <sub>IL</sub>	Input Low Voltage	-1.0	-	0.8	V	2
V <sub>IH(TF)</sub>	Test Enable Input High Voltage	V <sub>CC</sub> +4.5	-	10.5	V	2

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5±10%, Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES	
I <sub>CC1</sub>	OPERATING CURRENT Average Power Supply Operating Current (R <sub>AS</sub> , C <sub>S</sub> , Address Cycling: t <sub>RC</sub> =t <sub>RC</sub> MIN.)	TC511002P/J/Z-85	-	70	mA	3, 4
		TC511002P/J/Z-10	-	60	mA	
		TC511002P/J/Z-12	-	50	mA	
I <sub>CC2</sub>	STANDBY CURRENT Power Supply Standby Current (R <sub>AS</sub> =C <sub>S</sub> =V <sub>IH</sub> )		-	2	mA	
I <sub>CC3</sub>	R <sub>AS</sub> ONLY REFRESH CURRENT Average Power Supply Current, R <sub>AS</sub> Only Mode (R <sub>AS</sub> Cycling, C <sub>S</sub> =V <sub>IH</sub> : t <sub>RC</sub> =t <sub>RC</sub> , MIN.)	TC511002P/J/Z-85	-	70	mA	3
		TC511002P/J/Z-10	-	60	mA	
		TC511002P/J/Z-12	-	50	mA	
I <sub>CC4</sub>	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode(R <sub>AS</sub> =C <sub>S</sub> =V <sub>IL</sub> , Address Cycling: t <sub>SC</sub> =t <sub>SC</sub> MIN.)	TC511002P/J/Z-85	-	50	mA	3, 4
		TC511002P/J/Z-10	-	40	mA	
		TC511002P/J/Z-12	-	30	mA	
I <sub>CC5</sub>	STANDBY CURRENT Power Supply Standby Current (R <sub>AS</sub> =C <sub>S</sub> =V <sub>CC</sub> -0.2V)		-	1	mA	
I <sub>CC6</sub>	C <sub>S</sub> BEFORE R <sub>AS</sub> REFRESH CURRENT Average Power Supply Current, C <sub>S</sub> Before R <sub>AS</sub> Mode (R <sub>AS</sub> , C <sub>S</sub> Cycling: t <sub>RC</sub> =t <sub>RC</sub> MIN.)	TC511002P/J/Z-85	-	70	mA	3
		TC511002P/J/Z-10	-	60	mA	
		TC511002P/J/Z-12	-	50	mA	
I <sub>I(L)</sub>	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input (0V ≤ V <sub>IH</sub> ≤ 6.5V, All Other Pins Not Under Test = 0V)	-10	10	μA		
I <sub>ITF(L)</sub>	INPUT LEAKAGE CURRENT (only TF) (0V ≤ V <sub>IN(TF)</sub> ≤ 0.8V, All Other Pins Not Under Test=0V)	-10	10	μA		
I <sub>O(L)</sub>	OUTPUT LEAKAGE CURRENT (D <sub>OUT</sub> is disabled, 0V ≤ V <sub>OUT</sub> ≤ +5.5V)	-10	10	μA		
I <sub>TF</sub>	TEST FUNCTION INPUT CURRENT (V <sub>CC</sub> +4.5V ≤ V <sub>IN(TF)</sub> ≤ 10.5V)	-	1	mA		
V <sub>OH</sub>	OUTPUT LEVEL Output "H" Level Voltage (I <sub>OUT</sub> =-5mA)	2.4	-	V		
V <sub>OL</sub>	OUTPUT LEVEL Output "L" Level Voltage (I <sub>OUT</sub> =4.2mA)	-	0.4	V		

# TC511002P/J/Z-85, TC511002P/J/Z-10 TC511002P/J/Z-12

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V<sub>CC</sub>=5V±10%, T<sub>a</sub>=0 ~ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC511002P/J/Z-85		TC511002P/J/Z-10		TC511002P/J/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t <sub>RC</sub>	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t <sub>RWC</sub>	Read-Write Cycle Time	190	-	220	-	255	-	ns	
t <sub>SC</sub>	Static Column Mode Cycle Time	50	-	55	-	65	-	ns	
t <sub>SRWC</sub>	Static Column Mode Read Write Cycle Time	90	-	100	-	120	-	ns	
t <sub>RAC</sub>	Access Time from $\overline{\text{RAS}}$	-	85	-	100	-	120	ns	8,13
t <sub>CAC</sub>	Access Time from $\overline{\text{CS}}$	-	25	-	25	-	30	ns	8,13
t <sub>AA</sub>	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
t <sub>ALW</sub>	Access Time from Last Write	-	85	-	95	-	115	ns	8,15
t <sub>CLZ</sub>	$\overline{\text{CS}}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
t <sub>OFF</sub>	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
t <sub>AOH</sub>	Output Data Hold Time from Column Address	5	-	5	-	5	-	ns	
t <sub>OW</sub>	Output Data Enable Time from $\overline{\text{WRITE}}$	-	30	-	30	-	35	ns	
t <sub>WOH</sub>	Output Data Hold Time from $\overline{\text{WRITE}}$	0	-	0	-	0	-	ns	
t <sub>T</sub>	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t <sub>RP</sub>	$\overline{\text{RAS}}$ Precharge Time	70	-	80	-	90	-	ns	
t <sub>RAS</sub>	$\overline{\text{RAS}}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t <sub>RASC</sub>	$\overline{\text{RAS}}$ Pulse Width (Static Column Mode)	85	100,000	100	100,000	120	100,000	ns	
t <sub>RS</sub>	$\overline{\text{CS}}$ to $\overline{\text{RAS}}$ Hold Time	25	-	25	-	30	-	ns	
t <sub>CS</sub>	$\overline{\text{RAS}}$ to $\overline{\text{CS}}$ Hold Time	85	-	100	-	120	-	ns	
t <sub>CS</sub>	$\overline{\text{CS}}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t <sub>CSC</sub>	$\overline{\text{CS}}$ Pulse Width (Static Column Mode)	25	100,000	25	100,000	30	100,000	ns	
t <sub>RCD</sub>	$\overline{\text{RAS}}$ to $\overline{\text{CS}}$ Delay Time	25	60	25	75	25	90	ns	13
t <sub>RAD</sub>	$\overline{\text{RAS}}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t <sub>CRP</sub>	$\overline{\text{CS}}$ to $\overline{\text{RAS}}$ Precharge Time	10	-	10	-	10	-	ns	
t <sub>CP</sub>	$\overline{\text{CS}}$ Precharge Time (Static Column Mode)	10	-	10	-	15	-	ns	
t <sub>ASR</sub>	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t <sub>RAH</sub>	Row Address Hold Time	15	-	15	-	15	-	ns	
t <sub>ASC</sub>	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t <sub>CAH</sub>	Column Address Hold Time	20	-	20	-	25	-	ns	
t <sub>AWR</sub>	Write Address Hold Time referenced to $\overline{\text{RAS}}$	65	-	75	-	90	-	ns	
t <sub>AR</sub>	Column Address Hold Time referenced to $\overline{\text{RAS}}$	100	-	115	-	140	-	ns	
t <sub>RAL</sub>	Column Address to $\overline{\text{RAS}}$ Lead Time	45	-	50	-	60	-	ns	

**TC511002P/J/Z-85, TC511002P/J/Z-10  
TC511002P/J/Z-12**

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (continued)

SYMBOL	PARAMETER	TC511002P/J/Z-85		TC511002P/J/Z-10		TC511002P/J/Z-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$t_{AH}$	Column Address Hold Time referenced to $\overline{RAS}$ Rise	10	-	10	-	15	-	ns	16
$t_{CWL}$	Write Command to $\overline{CS}$ Lead Time	20	-	25	-	30	-	ns	
$t_{LWAD}$	Last Write to Column Address Delay Time	25	40	25	45	30	55	ns	15
$t_{AHLW}$	Last Write to Column Address Hold Time	85	-	95	-	115	-	ns	
$t_{RCS}$	Read Command Set-Up Time referenced to $\overline{CS}$	0	-	0	-	0	-	ns	
$t_{RCH}$	Read Command Hold Time referenced to $\overline{CS}$	0	-	0	-	0	-	ns	10
$t_{RRH}$	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
$t_{WH}$	Write Command Hold Time (Output Data Disable)	0	-	0	-	0	-	ns	12
$t_{WCR}$	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
$t_{WP}$	Write Command Pulse Width	20	-	20	-	25	-	ns	
$t_{WI}$	Write Command Inactive Time	10	-	10	-	15	-	ns	
$t_{RWL}$	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
$t_{DS}$	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
$t_{DH}$	Data-In Hold Time	20	-	20	-	25	-	ns	11
$t_{DHR}$	Data-In Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
$t_{REF}$	Refresh Period	-	8	-	8	-	8	ms	
$t_{WS}$	Write Command Set-Up Time (Output Data Disable)	0	-	0	-	0	-	ns	12
$t_{CWD}$	$\overline{CS}$ to $\overline{WRITE}$ Delay Time (READ-WRITE CYCLE)	25	-	25	-	30	-	ns	12
$t_{RWD}$	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time (READ-WRITE CYCLE)	85	-	100	-	120	-	ns	12
$t_{AWD}$	Column Address to $\overline{WRITE}$ Delay Time	45	-	50	-	60	-	ns	12
$t_{CSR}$	$\overline{CS}$ Set-Up Time ( $\overline{CS}$ before $\overline{RAS}$ )	10	-	10	-	10	-	ns	
$t_{CHR}$	$\overline{CS}$ Hold Time ( $\overline{CS}$ before $\overline{RAS}$ )	30	-	30	-	30	-	ns	
$t_{RPC}$	$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	0	-	0	-	0	-	ns	
$t_{CPT}$	$\overline{CS}$ Precharge Time ( $\overline{CS}$ before $\overline{RAS}$ Counter Test)	50	-	50	-	60	-	ns	
$t_{CPN}$	$\overline{CS}$ Precharge Time	15	-	15	-	20	-	ns	
$t_{TES}$	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	
$t_{TEH}$	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	

# TC511002P/J/Z-85, TC511002P/J/Z-10 TC511002P/J/Z-12

CAPACITANCE ( $V_{CC}=5V\pm 10\%$ ,  $f=1\text{MHz}$ ,  $T_a=0\sim 70^\circ\text{C}$ )

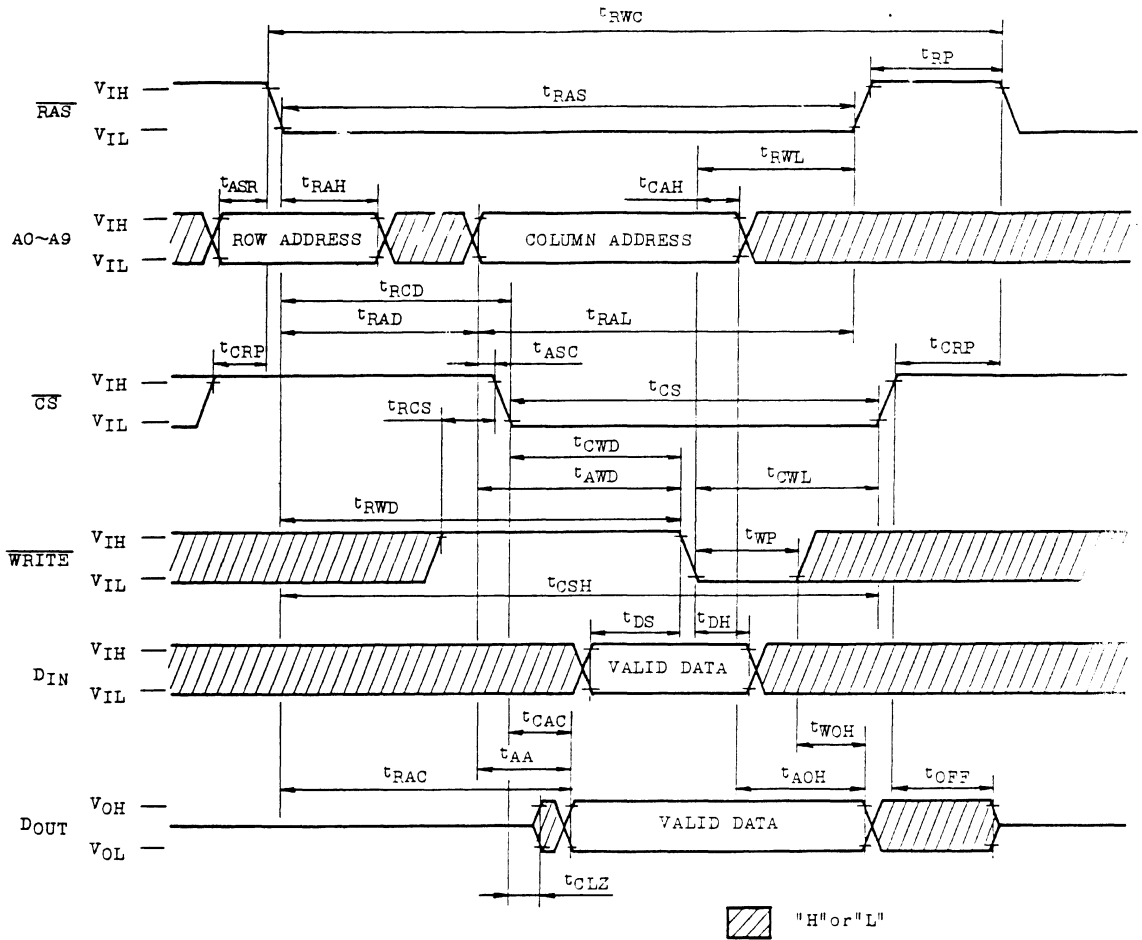
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance ( $A_0 \sim A_9$ , $D_{IN}$ )	-	5	pF
CI2	Input Capacitance ( $\overline{RAS}$ , $\overline{CS}$ , $\overline{WRITE}$ , TF)	-	7	
CO	Output Capacitance ( $D_{OUT}$ )	-	7	

## NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to  $V_{SS}$ .
3.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ ,  $I_{CC6}$  depend on cycle rate.
4.  $I_{CC1}$ ,  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200  $\mu\text{s}$  is required after power-up followed by any 8  $\overline{RAS}$  cycles before proper device operation is achieved.  
In case of using internal refresh counter, a minimum of 8  $\overline{CS}$  Before  $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
6. AC measurements assume  $t_T=5\text{ns}$ .
7.  $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9.  $t_{OFF}(\text{max.})$  defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
11. These parameters are referenced to  $\overline{CS}$  leading edge in early write cycles and to  $\overline{WRITE}$  leading edge in read-write cycles.
12.  $t_{WS}$ ,  $t_{WH}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WS} \geq t_{WS}(\text{min.})$  and  $t_{WH} \geq t_{WH}(\text{min.})$ , the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycles; If  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$  and  $t_{AWD} \geq t_{AWD}(\text{min.})$ , the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither or the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the  $t_{RCD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled by  $t_{CAC}$ .
14. Operation within the  $t_{RAD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only: If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled exclusively by  $t_{AA}$ .
15. Operation within the  $t_{LWAD}(\text{max.})$  limit insures that  $t_{ALW}(\text{max.})$  can be met.  $t_{LWAD}(\text{max.})$  is specified as a reference point only: If  $t_{LWAD}$  is greater than the specified  $t_{LWAD}(\text{max.})$  limit, then access time is controlled exclusively by  $t_{AA}$ .
16.  $t_{AH}$  is the condition to latch column address when  $\overline{RAS}$  has risen up.

# TC511002P/J/Z-85, TC511002P/J/Z-10 TC511002P/J/Z-12

## READ-WRITE CYCLE

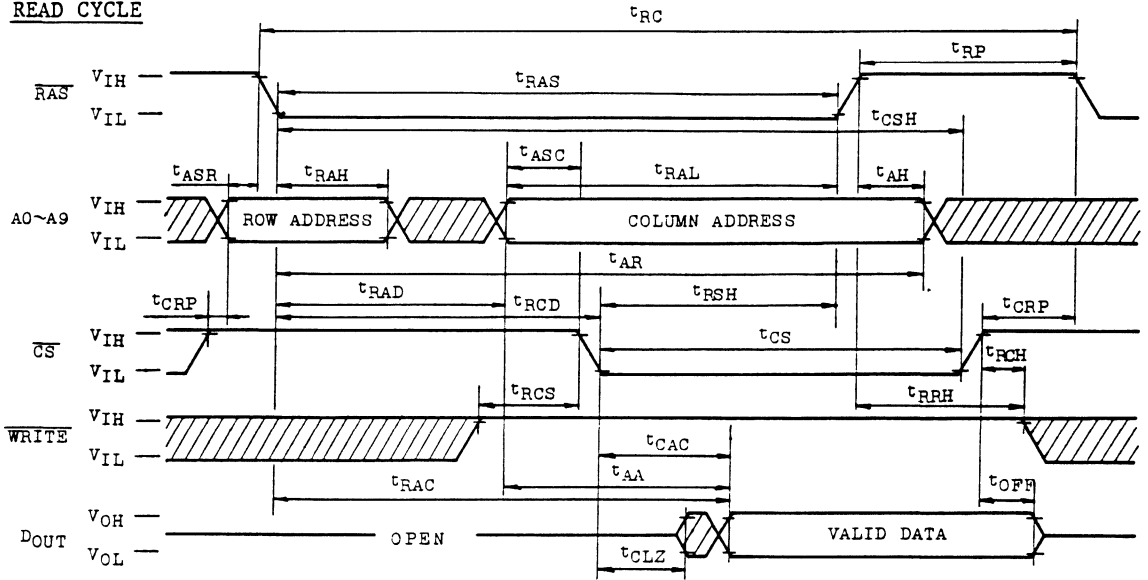


NOTE: "TF" pin should be connected to  $V_{IL}$  level or open, if "Test Mode" is not used.

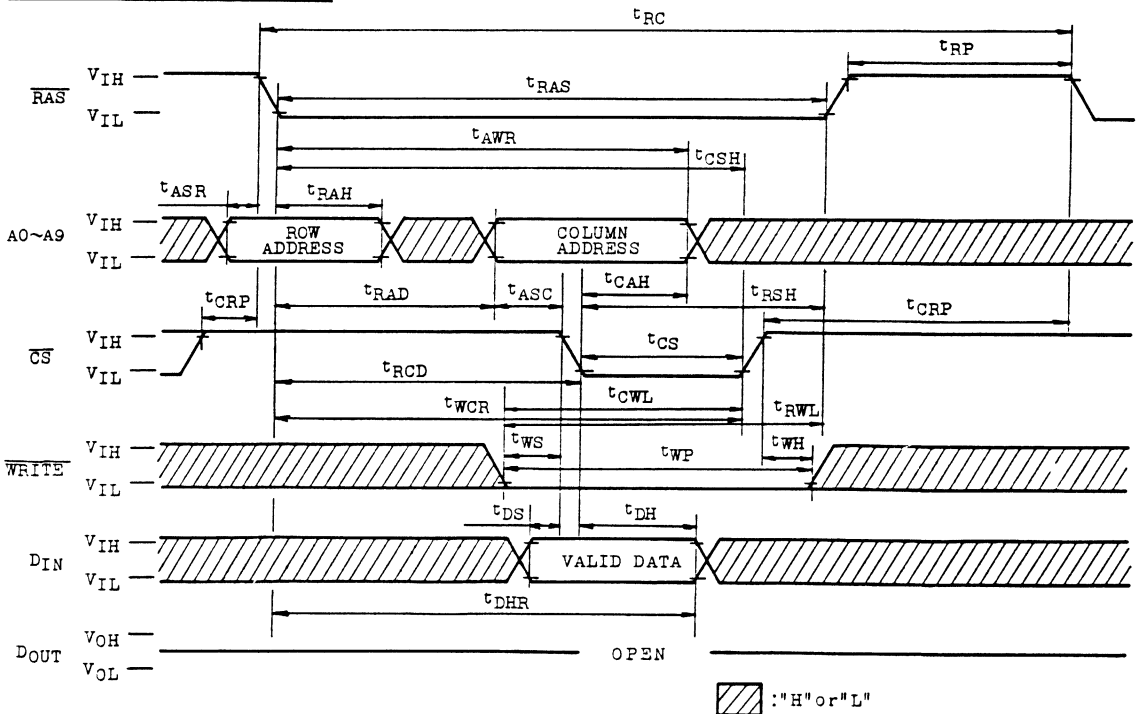
# TC511002P/J/Z-85, TC511002P/J/Z-10 TC511002P/J/Z-12

## TIMING WAVEFORMS

### READ CYCLE



### WRITE CYCLE (EARLY WRITE)

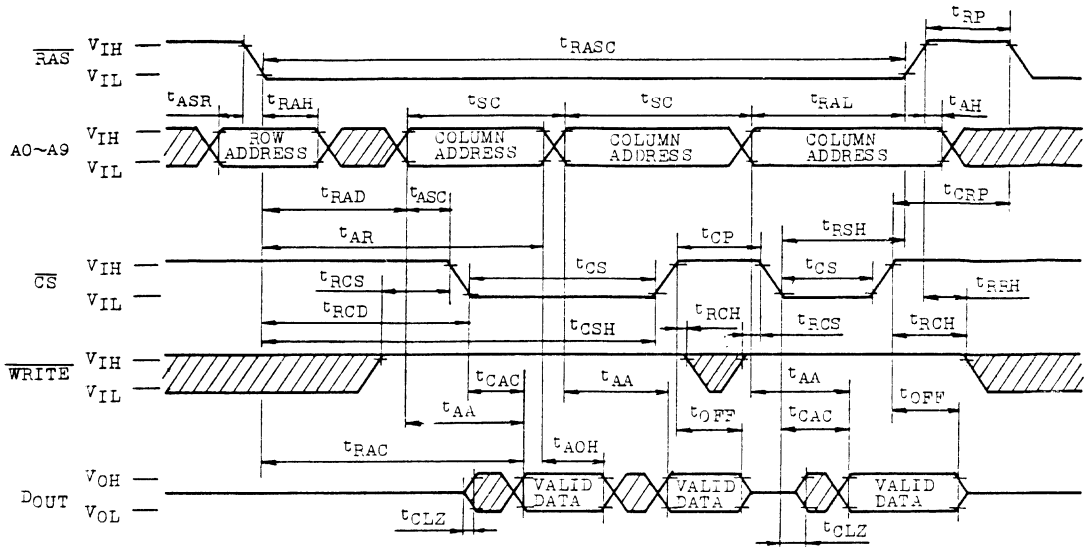


▨ : "H" or "L"

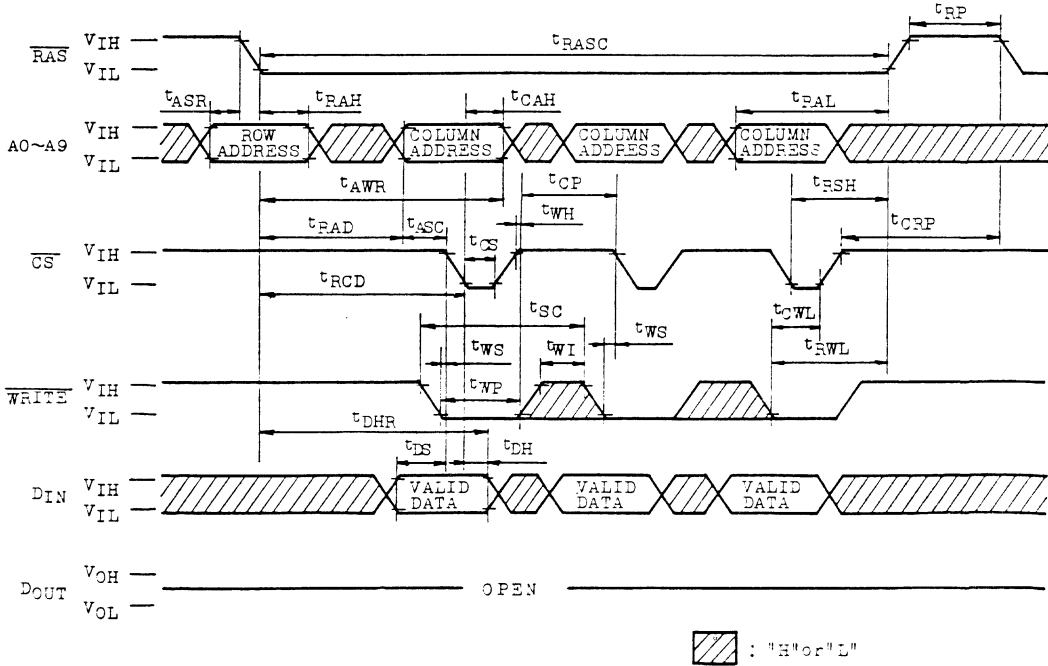
NOTE: "TF" pin should be connected to  $V_{IL}$  level or open, if "Test Mode" is not used.

# TC511002P/J/Z-85, TC511002P/J/Z-10 TC511002P/J/Z-12

## STATIC COLUMN MODE READ CYCLE



## STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



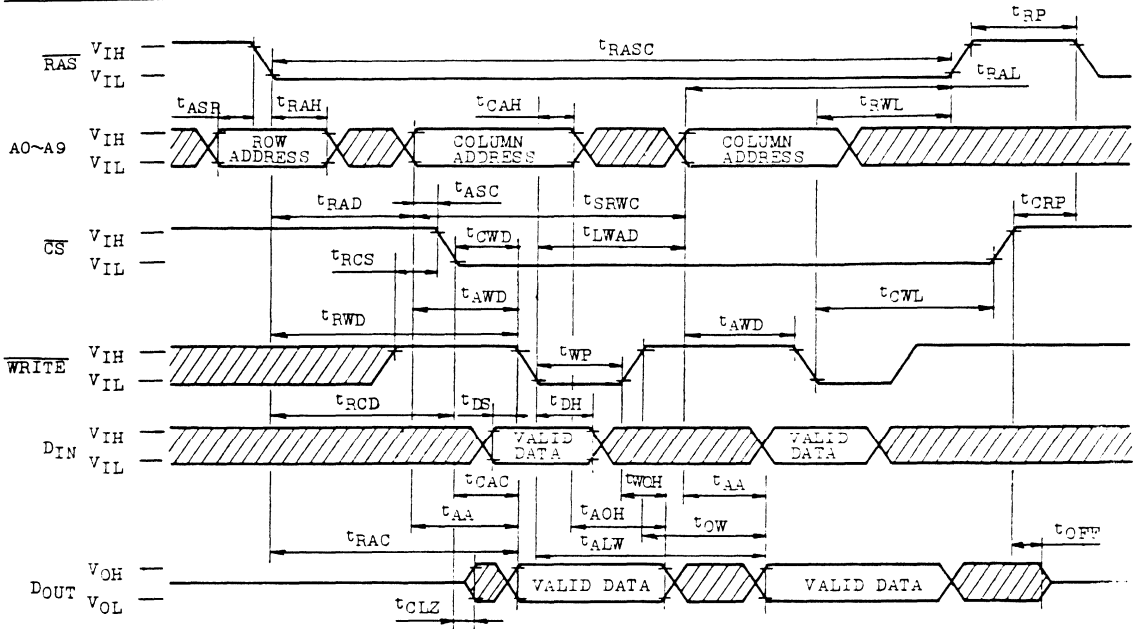
▨ : "R" or "L"

NOTE: "TF" pin should be connected to  $V_{IL}$  level or open, if "Test Mode" is not used.

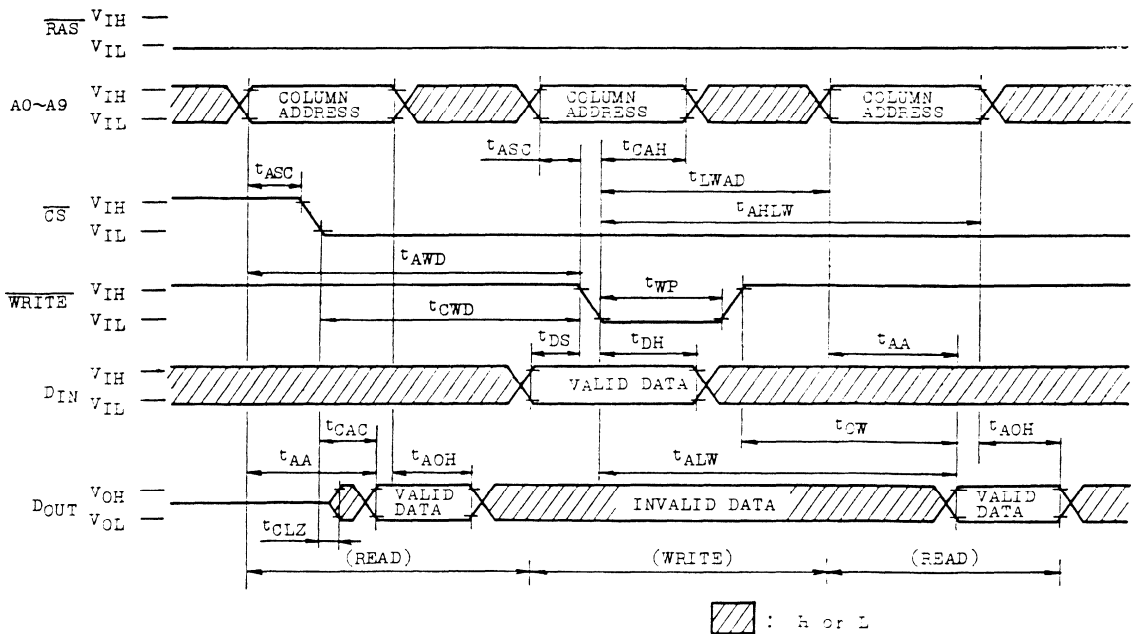


# TC511002P/J/Z-85, TC511002P/J/Z-10 TC511002P/J/Z-12

## STATIC COLUMN MODE READ-WRITE CYCLE



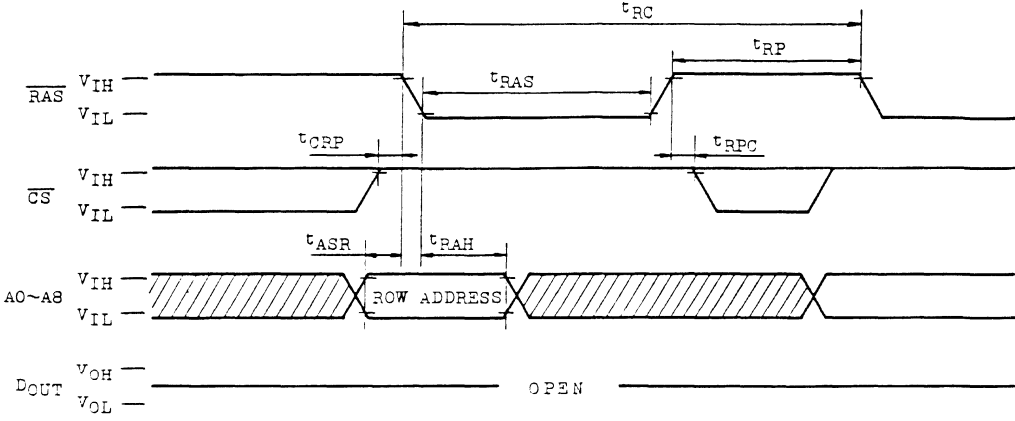
## STATIC COLUMN MODE READ/WRITE MIXED CYCLE



NOTE: "TF" pin should be connected to  $V_{IL}$  level or open, if "Test Mode" is not used.

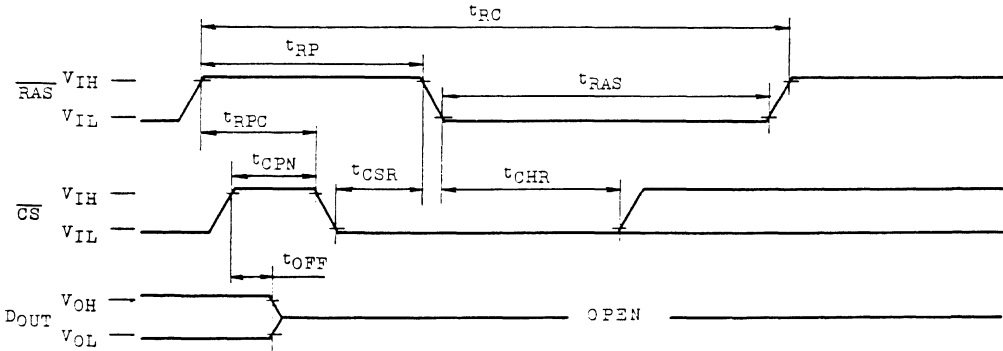
**TC511002P/J/Z-85, TC511002P/J/Z-10  
TC511002P/J/Z-12**

RAS ONLY REFRESH CYCLE



NOTE:  $\overline{\text{WRITE}}$ ="H" or "L", A9="H" or "L"  : "H" or "L"

CS BEFORE RAS REFRESH CYCLE

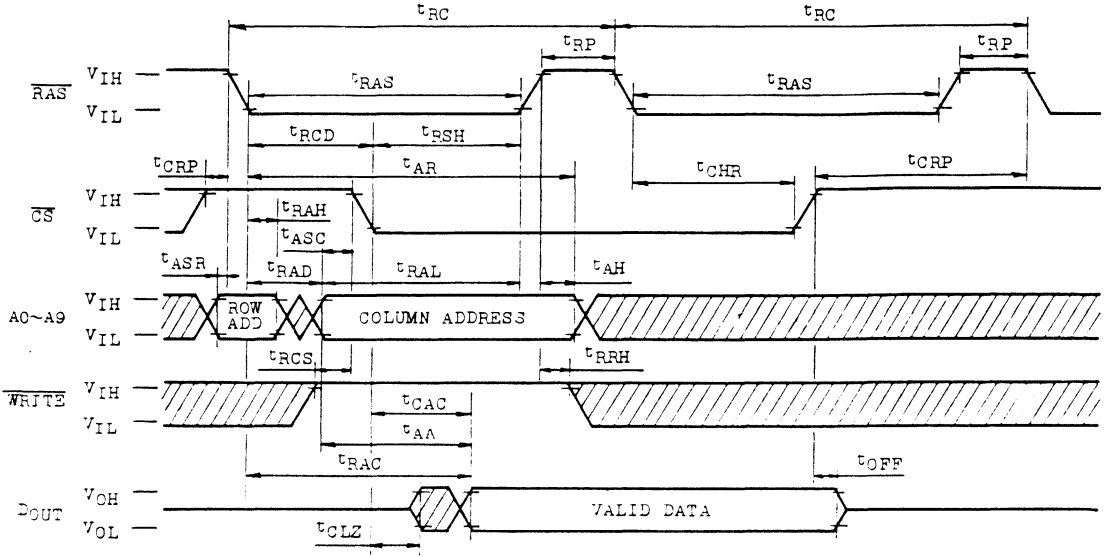


NOTE:  $\overline{\text{WRITE}}$ ="H" or "L", A0~A9="H" or "L"

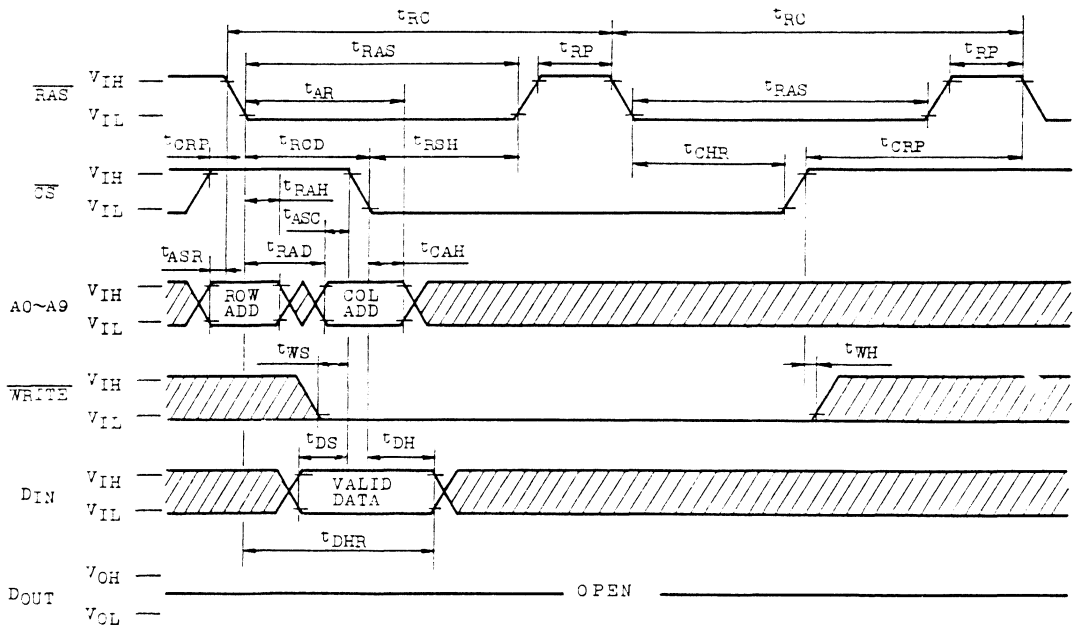
"TF" pin should be connected to VIL level or open, if "Test Mode" is not used.

# TC511002P/J/Z-85, TC511002P/J/Z-10 TC511002P/J/Z-12

## HIDDEN REFRESH CYCLE (READ)



## HIDDEN REFRESH CYCLE (WRITE)

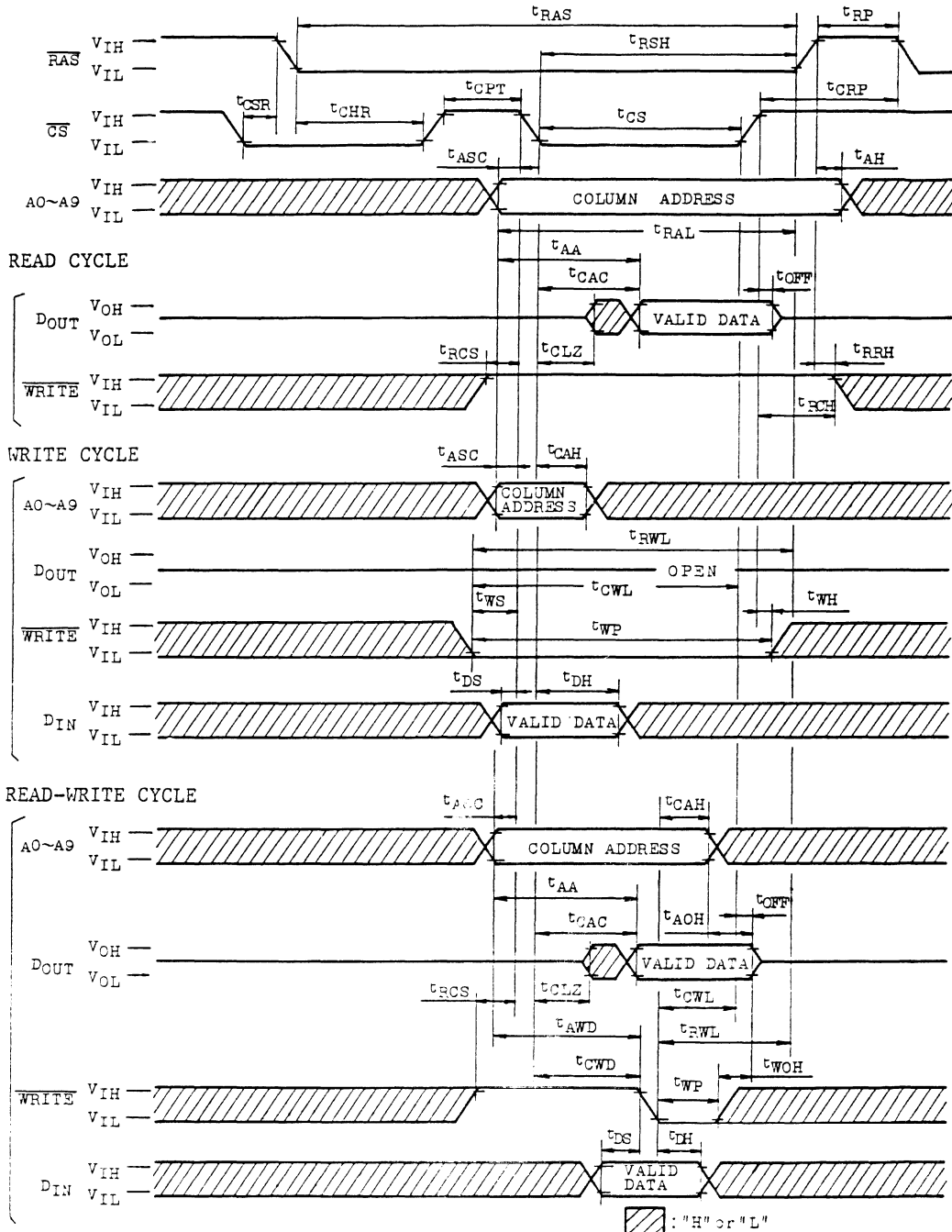


"H" or "L"

NOTE: "TF" pin should be connected to  $V_{IL}$  level or open, if "Test Mode" is not used.

# TC511002P/J/Z-85, TC511002P/J/Z-10 TC511002P/J/Z-12

## CS BEFORE RAS REFRESH COUNTER TEST CYCLE



NOTE: "TF" pin should be connected to VIL level or open, if "Test Mode" is not used.

# TC511002P/J/Z-85, TC511002P/J/Z-10 TC511002P/J/Z-12

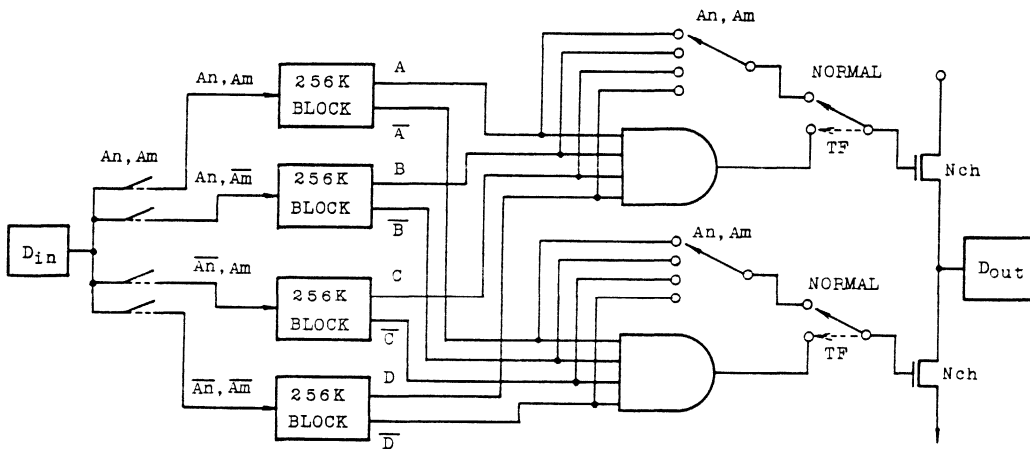
## DESCRIPTION OF THE TEST MODE FOR 1M DRAMS

The TC511000/1/2 is a CMOS DRAM organized as 1,048,576 words by 1-bit. It is internally organized as 262,144 words by 4-bits.

The "Test Mode" function allows for a 1M DRAM to be tested virtually as if it were a 256K DRAM. Figure 1 shows the block diagram of the "Test Mode" circuit. Data is written into the four 256K blocks in parallel and is retrieved the same way. A logical "and" operation is performed on the outputs of the four internal 256K blocks.

- o For a good device, the output data of the four internal blocks are identical to the input data (all "H" or all "L") and consequently the same data will appear on the output pin.
- o For a bad device, the output data of one or more of the internal blocks will differ from the input data and a high impedance state will be detected on the output pin.

### Block Diagram in Test Mode



TF Pin = Super voltage; Test Mode

TF Pin = Low level or Hi-Z; Normal

### Truth Table in Test Mode Function

A	B	C	D	DOUT
0	0	0	0	0
1	1	1	1	1
Otherwise				Hi-Z

Fig. 1

# TC511002P/J/Z-85, TC511002P/J/Z-10 TC511002P/J/Z-12

## DESCRIPTION OF THE TEST MODE FOR 1M DRAMS (CONTINUED)

The "Test Mode" function is enabled by applying a "Super Voltage" ( $V_{CC}+4.5V$ , max. voltage=10.5V) on the "TF" pin for a specified period ( $t_{TES}$  and  $t_{TEH}$  as shown in figure 2). It can be used while operating in any mode, including static column mode. It achieves a 4:1 reduction in test time for N patterns and a 16:1 reduction in test time for  $N^2$  patterns. The A9 address input is ignored during the "Test Mode"

During normal operation or when the "Test Mode" function is not used, the "TF" pin must be connected to VSS or TTL Logic Low Level, or left unconnected on the printed wiring board.

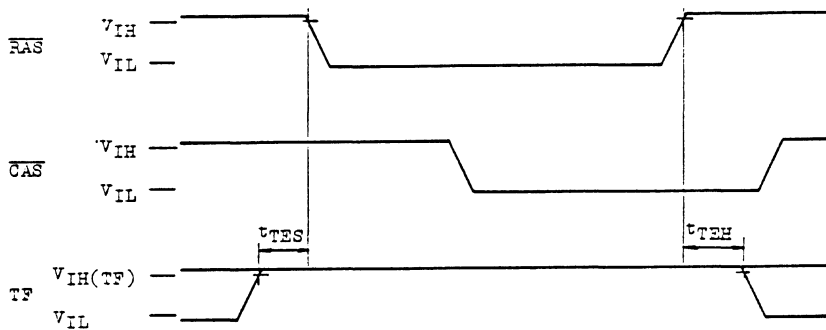


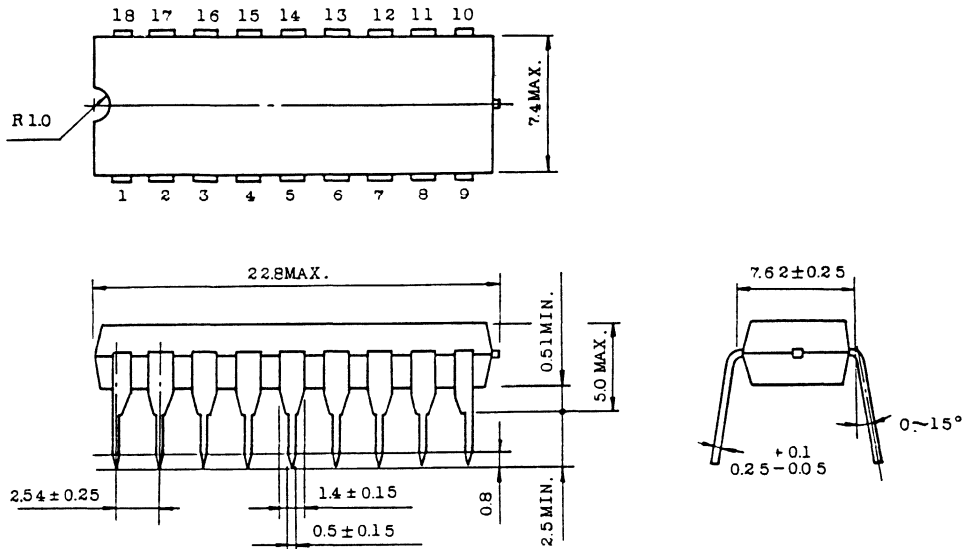
Fig.2 Test Mode Cycle

**TC511002P/J/Z-85, TC511002P/J/Z-10  
TC511002P/J/Z-12**

OUTLINE DRAWINGS

Plastic DIP

Unit in mm

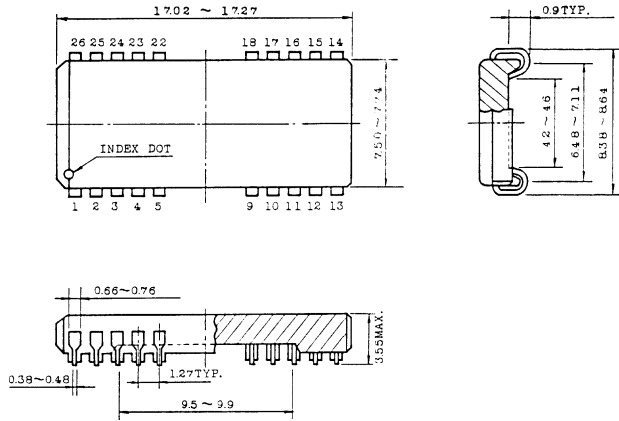


Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.18 leads. All dimensions are in millimeters.

# TC511002P/J/Z-85, TC511002P/J/Z-10 TC511002P/J/Z-12

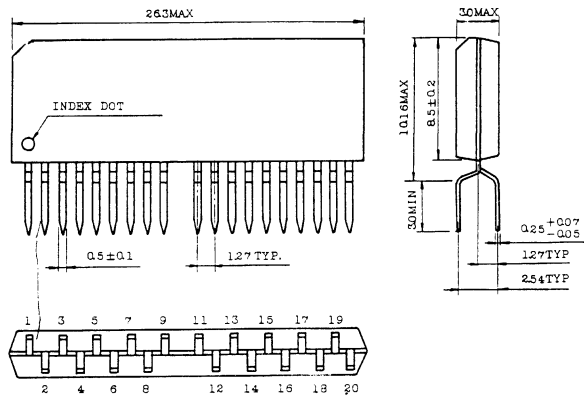
Plastic SOJ

Unit in mm



Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.

All dimensions are in millimeters.

Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.



# TOSHIBA MOS MEMORY PRODUCT

262,144 WORDS × 4 BIT DYNAMIC RAM  
SILICON GATE CMOS

TC514256P/J/Z-85, TC514256P/J/Z-10  
TC514256P/J/Z-12

## DESCRIPTION

The TC514256P/J/Z is the new generation dynamic RAM organized 262,144 words by 4 bit. The TC514256P/J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514256P/J/Z to be packaged in a standard 20 pin plastic DIP and 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

## FEATURES

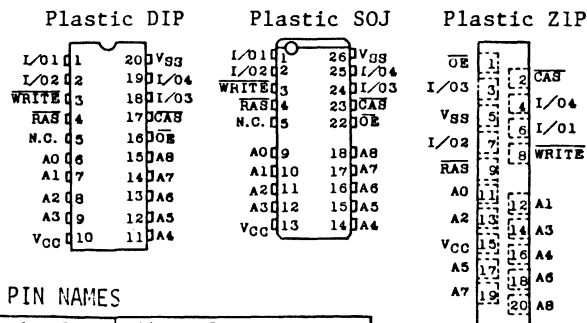
- 262,144 words by 4 bit organization
- Fast access time and cycle time

	TC514256P/J/Z-85-10-12
t <sub>RAC</sub> RAS Access Time	85ns 100ns 120ns
t <sub>AA</sub> Column Address Access Time	45ns 50ns 60ns
t <sub>CAC</sub> CAS Access Time	30ns 30ns 35ns
t <sub>RC</sub> Cycle Time	165ns 190ns 220ns
t <sub>PC</sub> Fast Page Mode Cycle Time	50ns 55ns 70ns

- Single power supply of 5V±10% with a built-in V<sub>BB</sub> generator

- Low Power  
413mW MAX. Operating (TC514256P/J/Z-85)  
358mW MAX. Operating (TC514256P/J/Z-10)  
303mW MAX. Operating (TC514256P/J/Z-12)  
5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, CAS before RAS refresh, RAS-only refresh, Hidden refresh, and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- Package Plastic DIP: TC514256P  
Plastic SOJ: TC514256J  
Plastic ZIP: TC514256Z

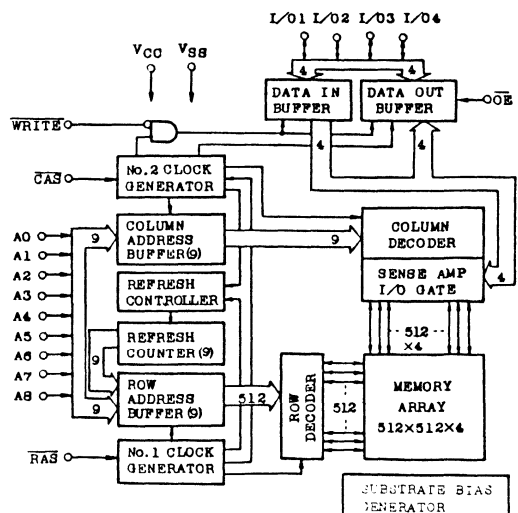
## PIN CONNECTION (TOP VIEW)



## PIN NAMES

A0 ~ A8	Address Inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
WRITE	Read/Write Input
OE	Output Enable
I/O1 ~ I/O4	Data Input/Output
VCC	Power (+5V)
VSS	Ground
N.C.	No Connection

## BLOCK DIAGRAM



# TC514256P/J/Z-85, TC514256P/J/Z-10 TC514256P/J/Z-12

## ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V <sub>IN</sub>	-1 ~ 7	V	1
Output Voltage	V <sub>OUT</sub>	-1 ~ 7	V	1
Power Supply Voltage	V <sub>CC</sub>	-1 ~ 7	V	1
Operating Temperature	T <sub>OPR</sub>	0 ~ 70	°C	1
Storage Temperature	T <sub>STG</sub>	-55 ~ 150	°C	1
Soldering Temperature • Time	T <sub>SOLDER</sub>	260 • 10	°C • sec	1
Power Dissipation	P <sub>D</sub>	600	mW	1
Short Circuit Output Current	I <sub>OUT</sub>	50	mA	1

## RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V	2
V <sub>IH</sub>	Input High Voltage	2.4	-	6.5	V	2
V <sub>IL</sub>	Input Low Voltage	-1.0	-	0.8	V	2

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10%, Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES	
I <sub>CC1</sub>	OPERATING CURRENT Average Power Supply Operating Current ( $\overline{RAS}$ , $\overline{CAS}$ , Address Cycling: $t_{RC}=t_{RC}$ MIN.)	TC514256P/J/Z-85	-	75	mA	3,4
		TC514256P/J/Z-10	-	65		
		TC514256P/J/Z-12	-	55		
I <sub>CC2</sub>	STANDBY CURRENT Power Supply Standby Current ( $\overline{RAS}=\overline{CAS}=V_{IH}$ )	-	2	mA		
I <sub>CC3</sub>	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ( $\overline{RAS}$ Cycling, $\overline{CAS}=V_{IH}$ : $t_{RC}=t_{RC}$ MIN.)	TC514256P/J/Z-85	-	75	mA	3
		TC514256P/J/Z-10	-	65		
		TC514256P/J/Z-12	-	55		
I <sub>CC4</sub>	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ( $\overline{RAS}=V_{IL}$ , $\overline{CAS}$ , Address Cycling: $t_{PC}=t_{PC}$ MIN.)	TC514256P/J/Z-85	-	55	mA	3,4
		TC514256P/J/Z-10	-	45		
		TC514256P/J/Z-12	-	35		
I <sub>CC5</sub>	STANDBY CURRENT Power Supply Standby Current ( $\overline{RAS}=\overline{CAS}=V_{CC}-0.2V$ )	-	1	mA		
I <sub>CC6</sub>	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ( $\overline{RAS}$ , $\overline{CAS}$ Cycling: $t_{RC}=t_{RC}$ MIN.)	TC514256P/J/Z-85	-	75	mA	3
		TC514256P/J/Z-10	-	65		
		TC514256P/J/Z-12	-	55		
I <sub>I(L)</sub>	INPUT LEAKAGE CURRENT Input Leakage Current, any input ( $0V \leq V_{IN} \leq 6.5V$ , All Other Pins Not Under Test=0V)	-10	10	μA		
I <sub>O(L)</sub>	OUTPUT LEAKAGE CURRENT (D <sub>OUT</sub> is disabled, $0V \leq V_{OUT} \leq V_{CC}$ )	-10	10	μA		
V <sub>OH</sub>	OUTPUT LEVEL Output "H" Level VOLTAGE (I <sub>OUT</sub> =-5mA)	2.4	-	V		
V <sub>OL</sub>	OUTPUT LEVEL Output "L" Level VOLTAGE (I <sub>OUT</sub> =4.2mA)	-	0.4	V		

# TC514256P/J/Z-85, TC514256P/J/Z-10 TC514256P/J/Z-12

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

( $V_{CC}=5V\pm 10\%$ ,  $T_a=0\sim 70^\circ C$ ) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC514256P/J/Z -85		TC514256P/J/Z -10		TC514256P/J/Z -12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$t_{RC}$	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
$t_{RMW}$	Read-Modify-Write Cycle Time	225	-	255	-	295	-	ns	
$t_{PC}$	Fast Page Mode Cycle Time	50	-	55	-	70	-	ns	
$t_{PRMW}$	Fast Page Mode Read-Modify-Write Cycle Time	110	-	115	-	140	-	ns	
$t_{RAC}$	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
$t_{CAC}$	Access Time from $\overline{CAS}$	-	30	-	30	-	35	ns	8,13
$t_{AA}$	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
$t_{CPA}$	Access Time from $\overline{CAS}$ Precharge	-	45	-	50	-	65	ns	8,14
$t_{CLZ}$	$\overline{CAS}$ to output in Low-Z	5	-	5	-	5	-	ns	5
$t_{OFF}$	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
$t_T$	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
$t_{RP}$	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
$t_{RAS}$	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
$t_{RASP}$	$\overline{RAS}$ Pulse Width (Fast Page Mode)	85	100,000	100	100,000	120	100,000	ns	
$t_{RSH}$	$\overline{RAS}$ Hold Time	30	-	30	-	35	-	ns	
$t_{RSH}$	$\overline{CAS}$ Hold Time	85	-	100	-	120	-	ns	
$t_{CAS}$	$\overline{CAS}$ Pulse Width	30	10,000	30	10,000	35	10,000	ns	
$t_{RCD}$	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	25	70	25	85	ns	13
$t_{RAD}$	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
$t_{CRP}$	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
$t_{CPN}$	$\overline{CAS}$ Precharge Time	15	-	15	-	20	-	ns	
$t_{CP}$	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	-	10	-	15	-	ns	
$t_{ASR}$	Row Address Set-Up Time	0	-	0	-	0	-	ns	
$t_{RAH}$	Row Address Hold Time	15	-	15	-	15	-	ns	
$t_{ASC}$	Column Address Set-Up Time	0	-	0	-	0	-	ns	
$t_{CAH}$	Column Address Hold Time	20	-	20	-	25	-	ns	
$t_{AR}$	Column Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
$t_{RAL}$	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	
$t_{RCS}$	Read Command Set-Up Time	0	-	0	-	0	-	ns	10
$t_{RCH}$	Read Command Hold Time	0	-	0	-	0	-	ns	10

**TC514256P/J/Z-85, TC514256P/J/Z-10  
TC514256P/J/Z-12**

SYMBOL	PARAMETER	TC514256P/J/Z -85		TC514256P/J/Z -10		TC514256P/J/Z -12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$t_{RRH}$	Read Command Hold Time referenced to RAS	0	-	0	-	0	-	ns	10
$t_{WCH}$	Write Command Hold Time	20	-	20	-	25	-	ns	
$t_{WCR}$	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
$t_{WP}$	Write Command Pulse Width	20	-	20	-	25	-	ns	
$t_{RWL}$	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
$t_{CWL}$	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	30	-	ns	
$t_{DS}$	Data Set-Up Time	0	-	0	-	0	-	ns	11
$t_{DH}$	Data Hold Time	20	-	20	-	25	-	ns	11
$t_{DHR}$	Data Hold Time Referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
$t_{REF}$	Refresh Period	-	8	-	8	-	8	ms	
$t_{WCS}$	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
$t_{CWD}$	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	65	-	65	-	75	-	ns	12
$t_{RWD}$	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	120	-	135	-	160	-	ns	12
$t_{AWD}$	Column Address to $\overline{WRITE}$ Delay Time	80	-	85	-	100	-	ns	12
$t_{CSR}$	$\overline{CAS}$ Set-Up Time ( $\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
$t_{CHR}$	$\overline{CAS}$ Hold Time ( $\overline{CAS}$ before $\overline{RAS}$ cycle)	30	-	30	-	30	-	ns	
$t_{RPC}$	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
$t_{CPT}$	$\overline{CAS}$ Precharge Time ( $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50	-	50	-	60	-	ns	
$t_{ROH}$	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	20	-	20	-	20	-	ns	
$t_{OEA}$	$\overline{OE}$ Access Time	-	25	-	25	-	30	ns	
$t_{OED}$	$\overline{OE}$ to Data Delay	25	-	25	-	30	-	ns	
$t_{OEZ}$	Output buffer turn off Delay Time from OE	0	25	0	25	0	30	ns	
$t_{OEH}$	$\overline{OE}$ Command Hold Time	25	-	25	-	30	-	ns	

CAPACITANCE ( $V_{CC} = 5V \pm 10\%$ ,  $f = 1MHz$ ,  $T_a = 0 \sim 70^\circ C$ )

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C11	Input Capacitance ( $A_0 - A_8$ )	-	5	pF
C12	Input Capacitance ( $\overline{RAS}, \overline{CAS}, \overline{WRITE}, \overline{OE}$ )	-	7	pF
C0	Output Capacitance ( $I/O_1 - I/O_4$ )	-	7	pF

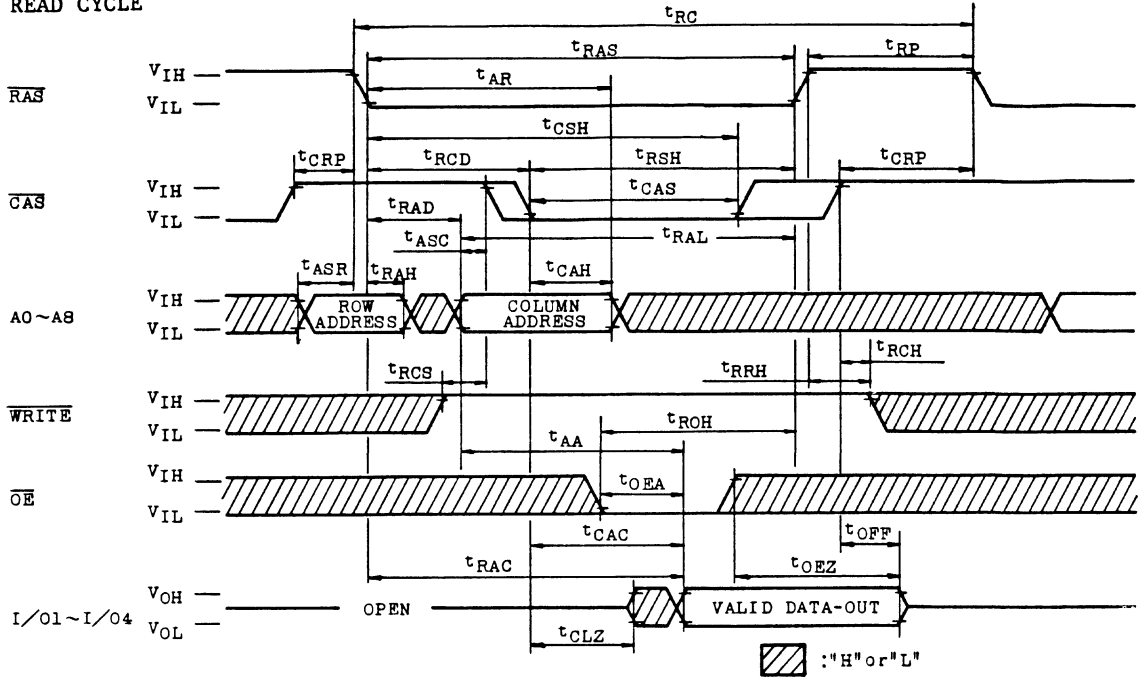
# TC514256P/J/Z-85, TC514256P/J/Z-10 TC514256P/J/Z-12

## NOTES:

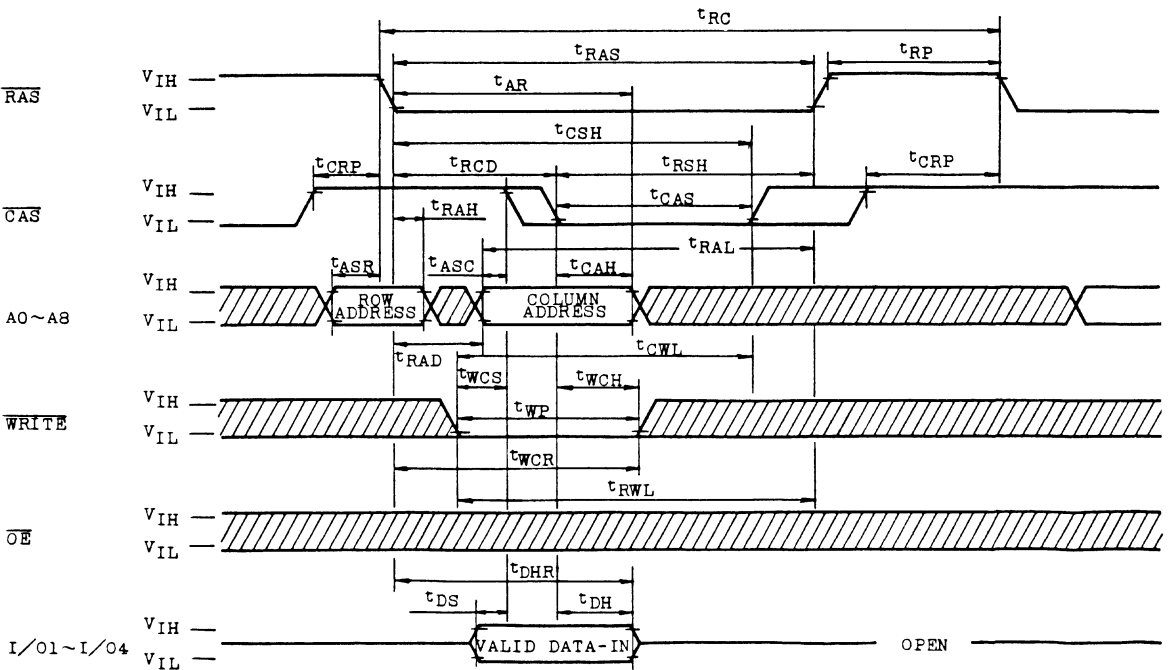
1. Stresses greater than those listed under "Absolute Maximum Ratings" May cause permanent damage to the device.
2. All voltage are reference to  $V_{SS}$ .
3.  $I_{cc1}$ ,  $I_{cc3}$ ,  $I_{cc4}$ ,  $I_{cc6}$  depend on cycle rate.
4.  $I_{cc1}$ ,  $I_{cc4}$  depend on output loading. Specified value are obtained with the output open.
5. An initial pause of 200 $\mu$ s is required after power-up followed by 8  $\overline{RAS}$  cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{CAS}$  Before  $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
6. AC measurements assume  $t_T=5$ ns.
7.  $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
8. Measurement with a load equivalent to 2 TTL loads and 100pF.
9.  $t_{OFF}(\text{max.})$  and  $t_{OEZ}(\text{max.})$  define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
11. These parameters are referenced to  $\overline{CAS}$  leading edge in early write cycles and to  $\overline{WRITE}$  leading edge in read-modify-write cycles.
12.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$  the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$  and  $t_{AWD} \geq t_{AWD}(\text{min.})$ , the cycle is a read-modify-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the  $t_{RCD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled by  $t_{CAC}$ .
14. Operation within the  $t_{RAD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only: If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled by  $t_{AA}$ .

**TC514256P/J/Z-85, TC514256P/J/Z-10  
TC514256P/J/Z-12**

**READ CYCLE**

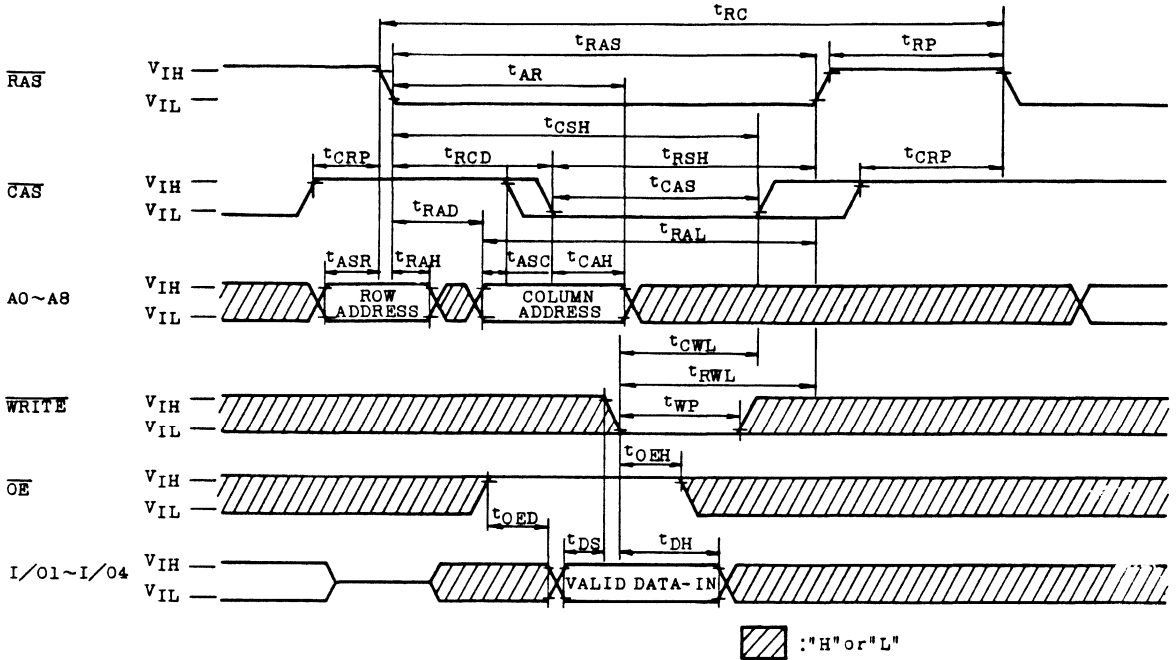


**WRITE CYCLE (EARLY WRITE)**

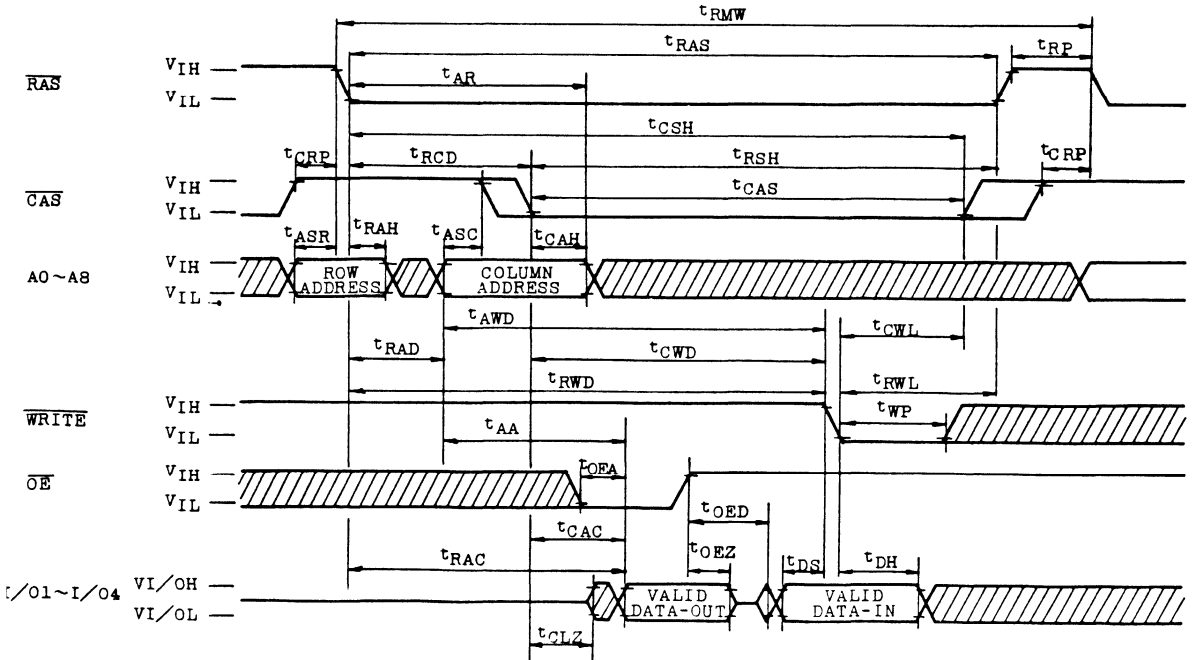


# TC514256P/J/Z-85, TC514256P/J/Z-10 TC514256P/J/Z-12

## WRITE CYCLE ( $\overline{OE}$ CONTROLLED WRITE)

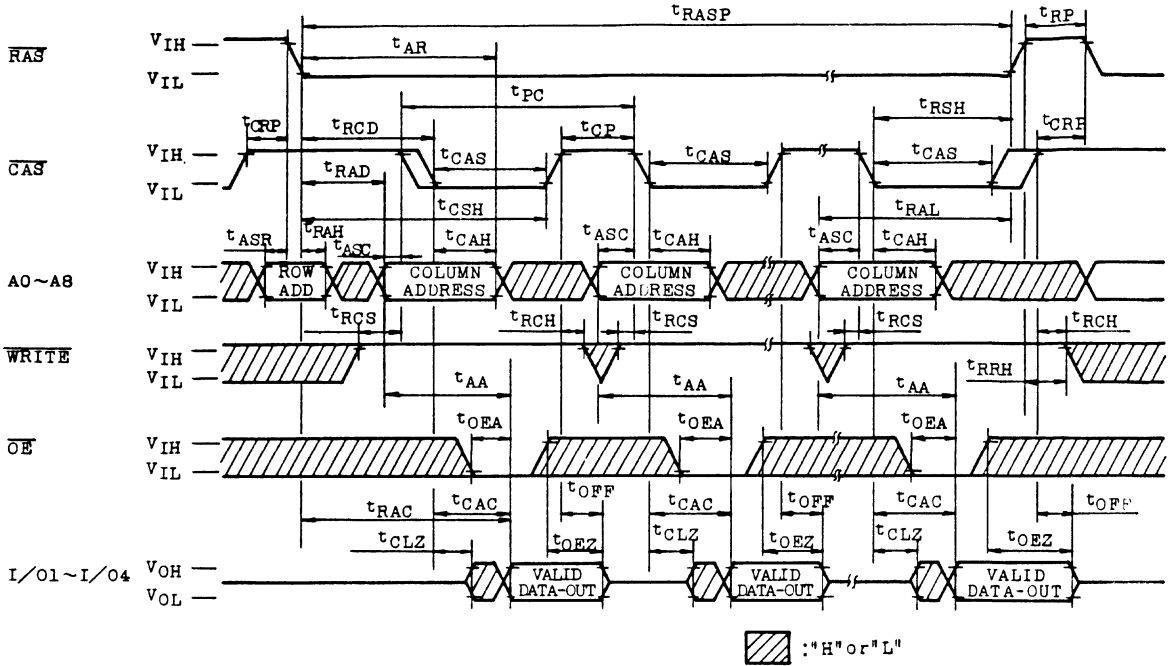


## READ-MODIFY-WRITE CYCLE

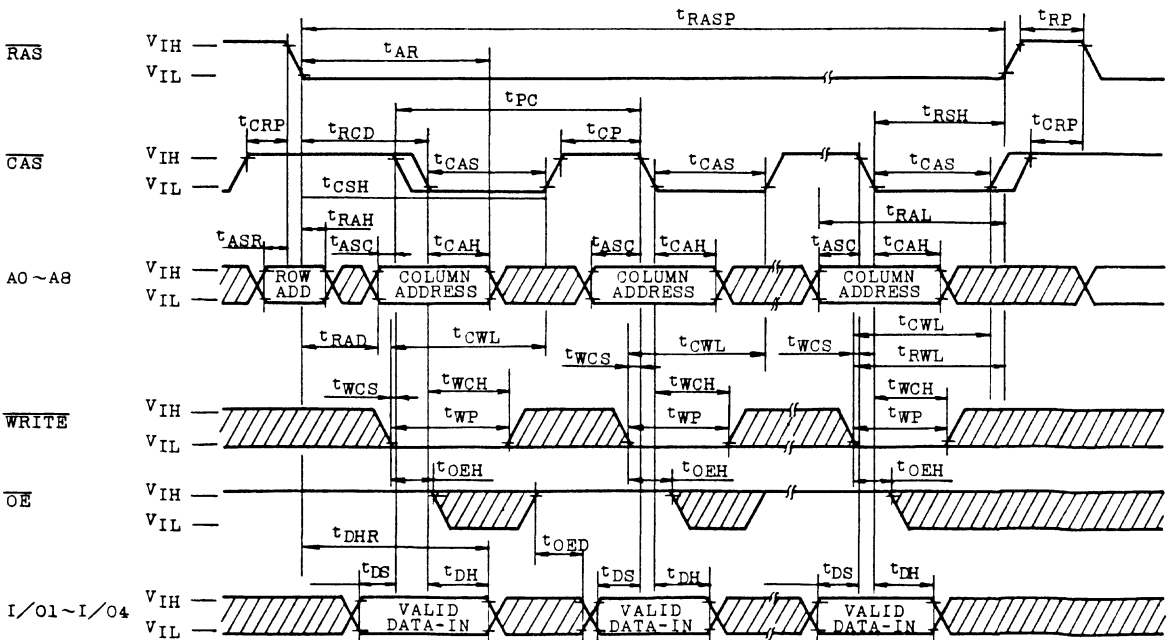


# TC514256P/J/Z-85, TC514256P/J/Z-10 TC514256P/J/Z-12

## FAST PAGE MODE READ CYCLE



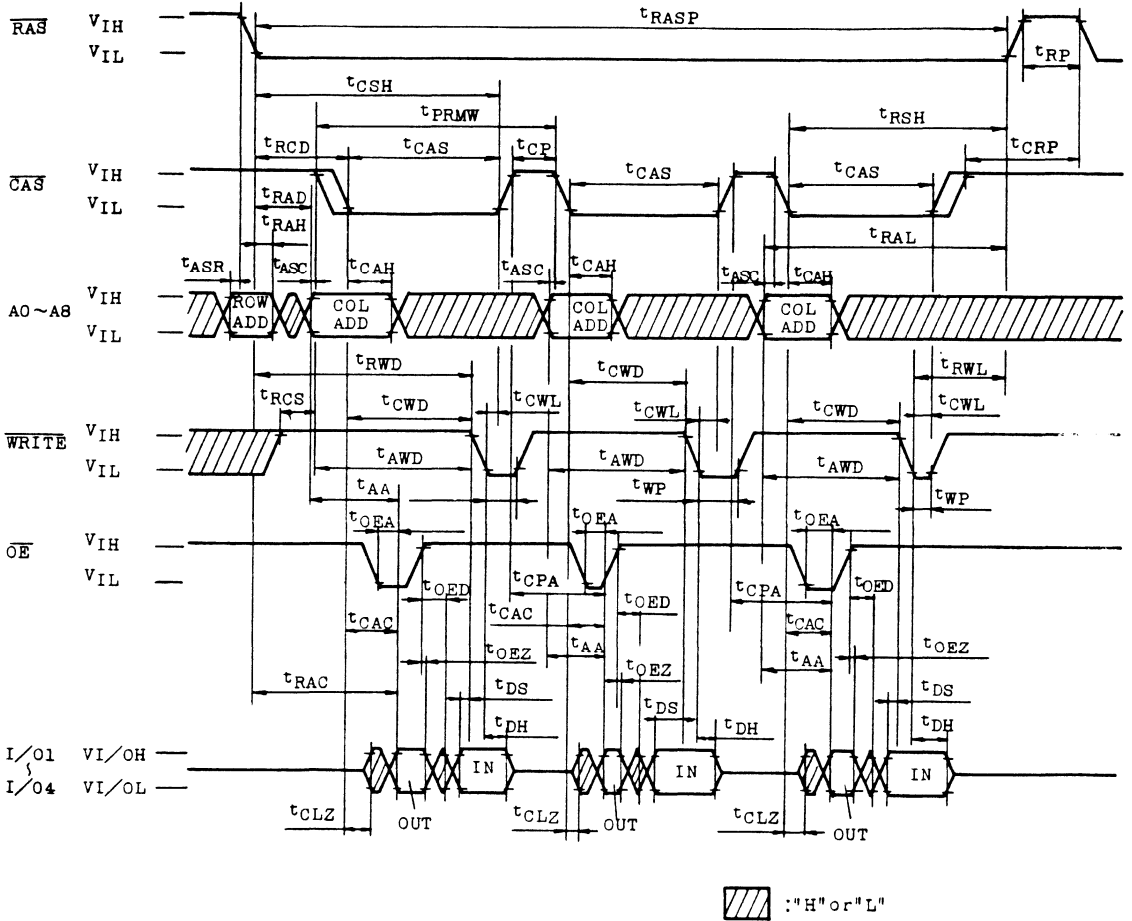
## FAST PAGE MODE WRITE CYCLE





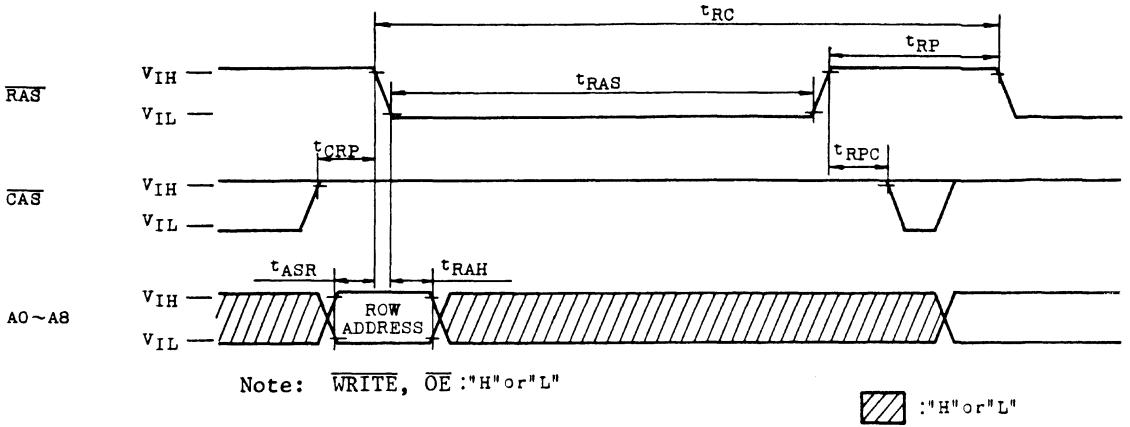
# TC514256P/J/Z-85, TC514256P/J/Z-10 TC514256P/J/Z-12

## FAST PAGE MODE READ-MODIFY-WRITE CYCLE

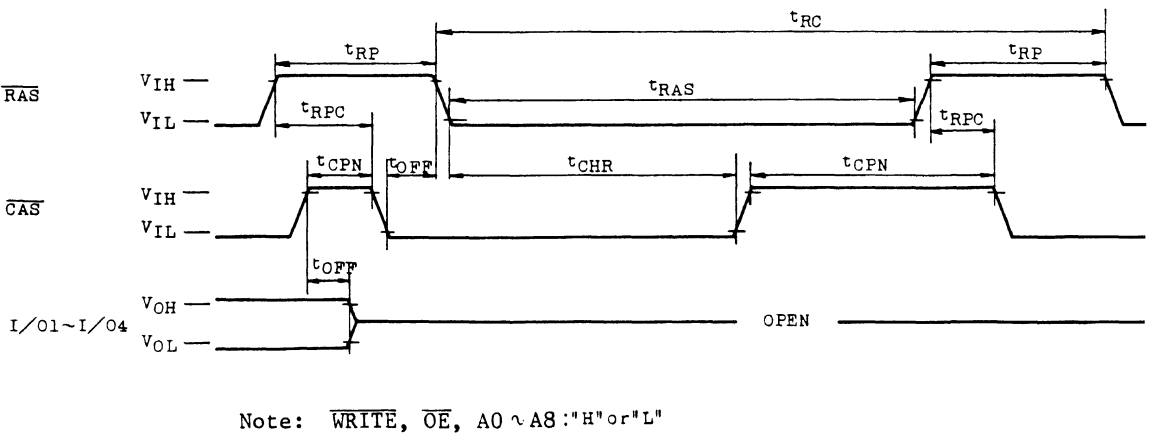


**TC514256P/J/Z-85, TC514256P/J/Z-10  
TC514256P/J/Z-12**

**RAS ONLY REFRESH CYCLE**

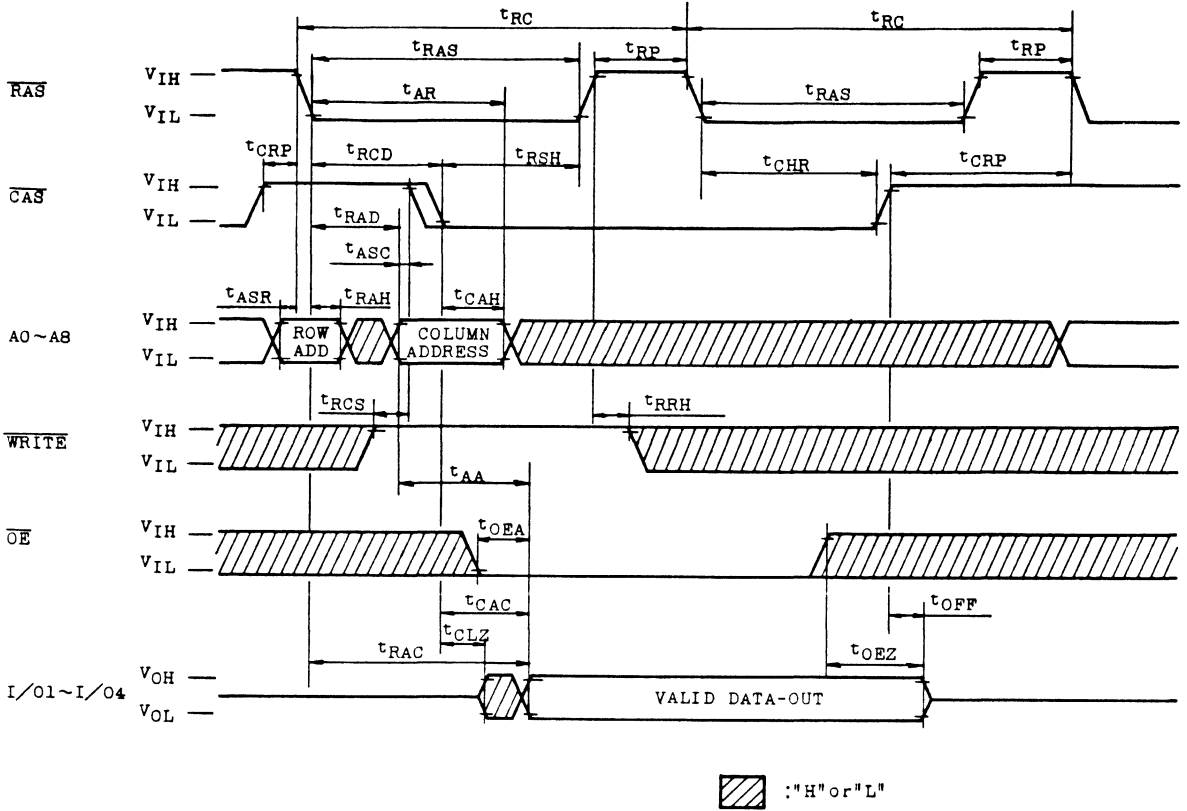


**CAS BEFORE RAS REFRESH CYCLE**



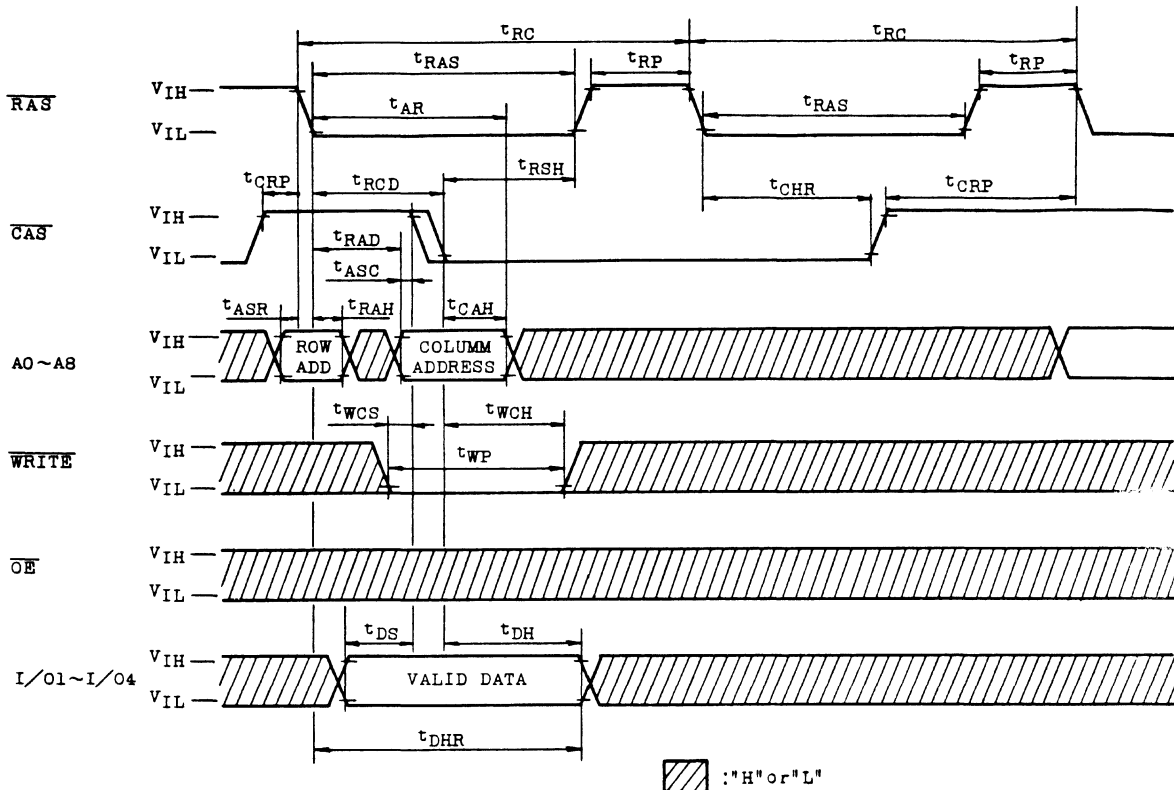
# TC514256P/J/Z-85, TC514256P/J/Z-10 TC514256P/J/Z-12

## HIDDEN REFRESH CYCLE (READ)



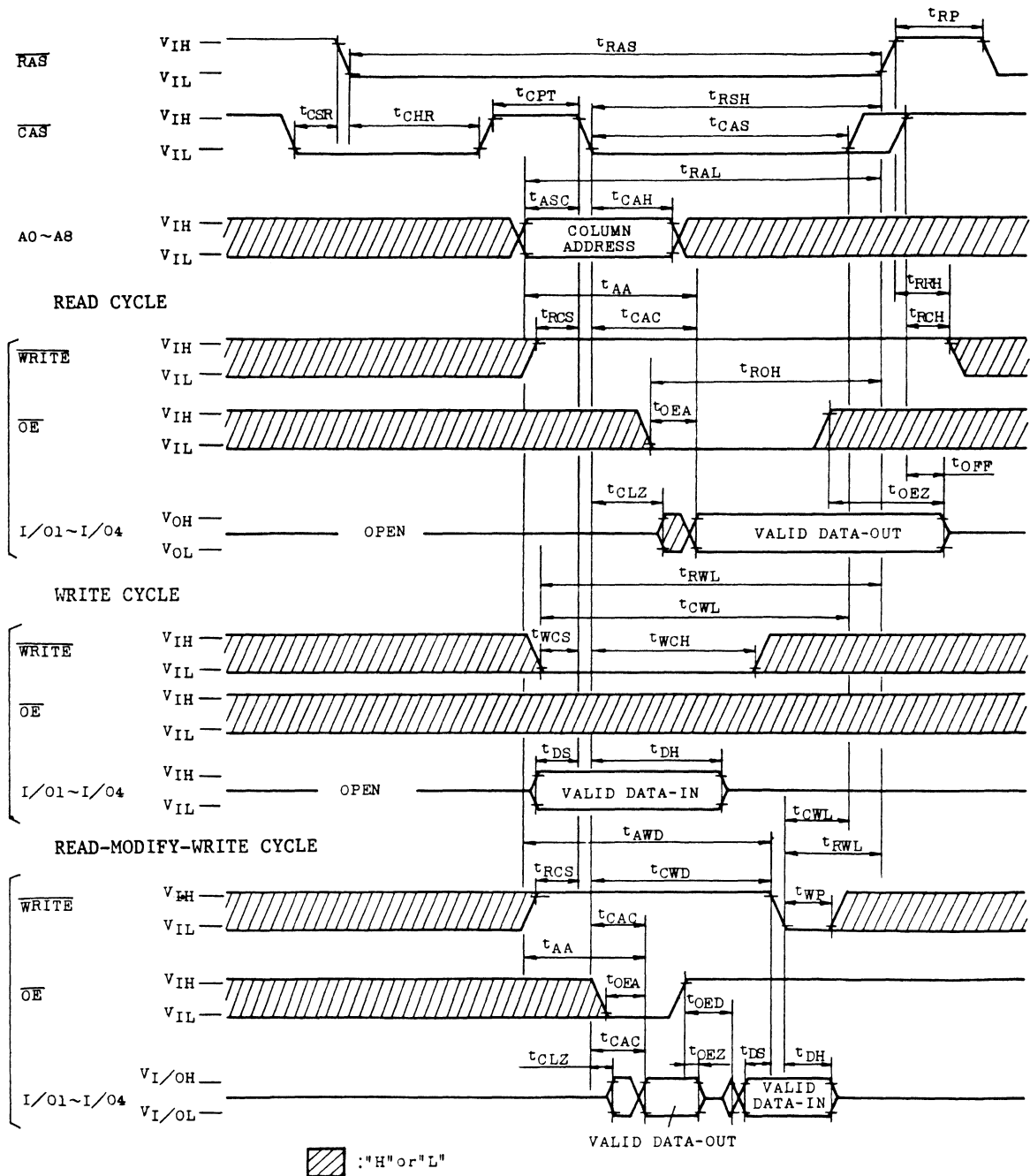
# TC514256P/J/Z-85, TC514256P/J/Z-10 TC514256P/J/Z-12

## HIDDEN REFRESH CYCLE (WRITE)



# TC514256P/J/Z-85, TC514256P/J/Z-10 TC514256P/J/Z-12

CAS BEFORE RAS REFRESH COUNTER TEST CYCLE

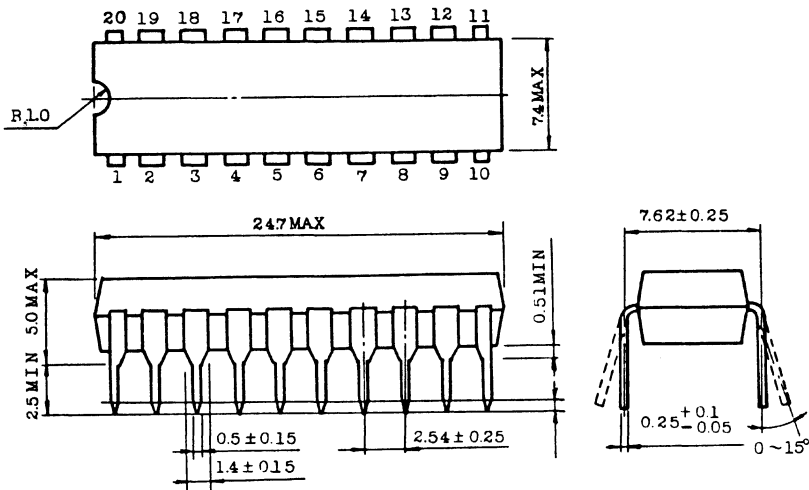


**TC514256P/J/Z-85, TC514256P/J/Z-10  
TC514256P/J/Z-12**

OUTLINE DRAWINGS

- Plastic DIP

Unit in mm



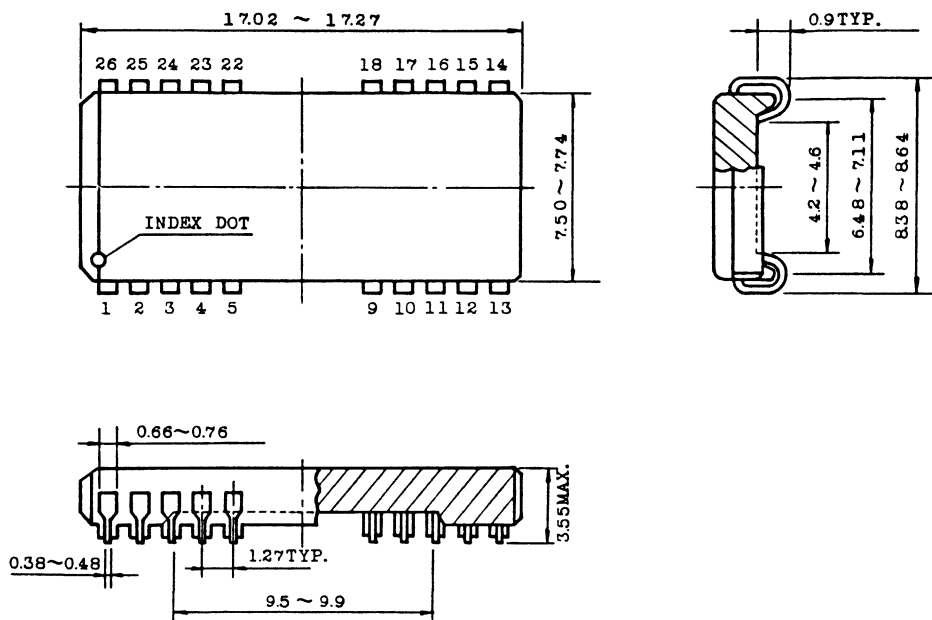
Note: Each lead pitch is 2.54mm.

All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.20 leads.

All dimensions are in millimeters.

# TC514256P/J/Z-85, TC514256P/J/Z-10 TC514256P/J/Z-12

• Plastic SOJ



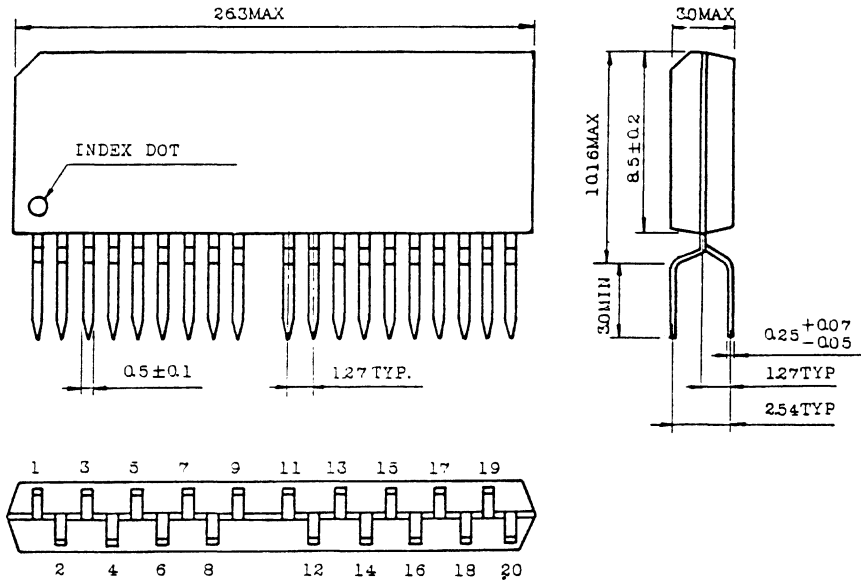
Note: Each lead pitch 1.27mm.

All dimensions are in millimeters.

**TC514256P/J/Z-85, TC514256P/J/Z-10  
TC514256P/J/Z-12**

• Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.

All dimensions are in millimeters.

Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.



# TOSHIBA MOS MEMORY PRODUCT

262,144 WORDS × 4 BIT DYNAMIC RAM  
SILICON GATE CMOS

TC514258P/J/Z-85, TC514258P/J/Z-10  
TC514258P/J/Z-12

## DESCRIPTION

The TC514258P/J/Z is the new generation dynamic RAM organized 262,144 words by 4 bit. The TC514258P/J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514258P/J/Z to be packaged in a standard 20 pin plastic DIP and 20/26 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

## FEATURES

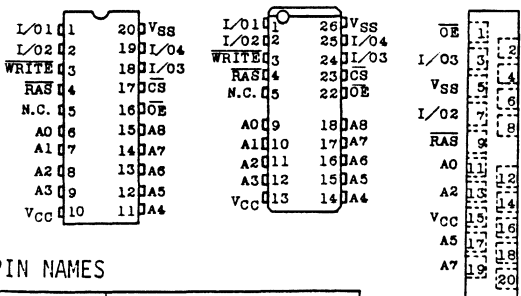
- 262,144 words by 4 bit organization
- Fast access time and cycle time
- Low Power
  - 413mW MAX. Operating (TC514258P/J/Z-85)
  - 358mW MAX. Operating (TC514258P/J/Z-10)
  - 303mW MAX. Operating (TC514258P/J/Z-12)
  - 5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write,  $\overline{CS}$  before  $\overline{RAS}$  refresh, RAS-only refresh, Hidden refresh and Static Column Mode capability
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- Package Plastic DIP: TC514258P  
Plastic SOJ: TC514258J  
Plastic ZIP: TC514258Z

	TC514258P/J/Z-85-10-12		
$t_{RAC}$ $\overline{RAS}$ Access Time	85ns	100ns	120ns
$t_{AA}$ Column Address Access Time	45ns	50ns	60ns
$t_{CAC}$ $\overline{CS}$ Access Time	30ns	30ns	35ns
$t_{RC}$ Cycle Time	165ns	190ns	220ns
$t_{SC}$ Static Column Mode Cycle Time	50ns	55ns	65ns

- Single power supply of 5V±10% with a built-in  $V_{BB}$  generator

## PIN CONNECTION (TOP VIEW)

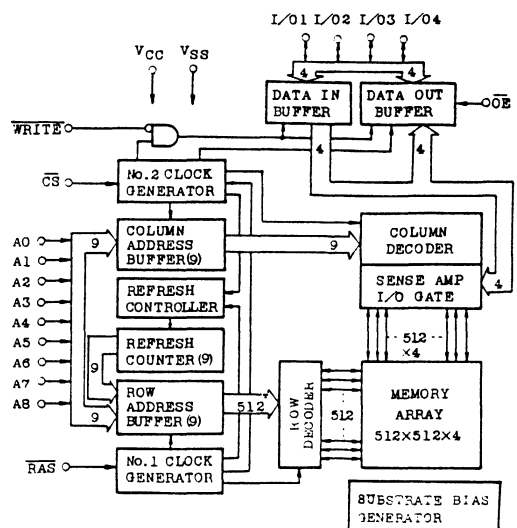
- Plastic DIP
- Plastic SOJ
- Plastic ZIP



## PIN NAMES

A0 ~ A8	Address Inputs
RAS	Row Address Strobe
$\overline{CS}$	Chip Select
WRITE	Read/Write Input
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Input/Output
VCC	Power (+5V)
VSS	Ground
N.C.	No Connection

## BLOCK DIAGRAM



# TC514258P/J/Z-85, TC514258P/J/Z-10 TC514258P/J/Z-12

## ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V <sub>IN</sub>	-1 ~ 7	V	1
Output Voltage	V <sub>OUT</sub>	-1 ~ 7	V	1
Power Supply Voltage	V <sub>CC</sub>	-1 ~ 7	V	1
Operating Temperature	T <sub>OPR</sub>	0 ~ 70	°C	1
Storage Temperature	T <sub>STG</sub>	-55 ~ 150	°C	1
Soldering Temperature • Time	T <sub>SOLDER</sub>	260 • 10	°C • sec	1
Power Dissipation	P <sub>D</sub>	600	mW	1
Short Circuit Output Current	I <sub>OUT</sub>	50	mA	1

## RECOMMENDED DC OPERATING CONDITIONS (T<sub>a</sub>=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V	2
V <sub>IH</sub>	Input High Voltage	2.4	-	6.5	V	2
V <sub>IL</sub>	Input Low Voltage	-1.0	-	0.8	V	2

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10%, T<sub>a</sub>=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	UNIT	UNITS	NOTES	
I <sub>CC1</sub>	OPERATING CURRENT Average Power Supply Operating Current ( $\overline{RAS}$ , $\overline{CS}$ , Address Cycling: $t_{RC}=t_{RC}$ MIN.)	TC514258P/J/Z-85	-	75	mA	3, 4
		TC514258P/J/Z-10	-	65		
		TC514258P/J/Z-12	-	55		
I <sub>CC2</sub>	STANDBY CURRENT Power Supply Standby Current ( $\overline{RAS}=\overline{CS}=V_{IH}$ )	-	2	mA		
I <sub>CC3</sub>	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ( $\overline{RAS}$ Cycling, $\overline{CS}=V_{IH}$ : $t_{RC}=t_{RC}$ MIN.)	TC514258P/J/Z-85	-	75	mA	3
		TC514258P/J/Z-10	-	65		
		TC514258P/J/Z-12	-	55		
I <sub>CC4</sub>	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode ( $\overline{RAS}=\overline{CS}=V_{IL}$ , Address Cycling: $t_{SC}=t_{SC}$ MIN.)	TC514258P/J/Z-85	-	75	mA	3, 4
		TC514258P/J/Z-10	-	65		
		TC514258P/J/Z-12	-	55		
I <sub>CC5</sub>	STANDBY CURRENT Power Supply Standby Current ( $\overline{RAS}=\overline{CS}=V_{CC}-0.2V$ )	-	1	mA		
I <sub>CC6</sub>	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ( $\overline{RAS}$ , $\overline{CS}$ Cycling: $t_{RC}=t_{RC}$ MIN.)	TC514258P/J/Z-85	-	75	mA	3
		TC514258P/J/Z-10	-	65		
		TC514258P/J/Z-12	-	55		
I <sub>I(L)</sub>	INPUT LEAKAGE CURRENT Input Leakage Current, any input ( $0V \leq V_{IN} \leq 6.5V$ , All Other Pins Not Under Test = 0V)	-10	10	$\mu A$		
I <sub>O(L)</sub>	OUTPUT LEAKAGE CURRENT (DOUT is disable, $0V \leq V_{OUT} \leq 5.5V$ )	-10	10	$\mu A$		
V <sub>OH</sub>	OUTPUT LEVEL Output "H" Level Voltage (I <sub>OUT</sub> =-5mA)	2.4	-	V		
V <sub>OL</sub>	OUTPUT LEVEL Output "L" Level Voltage (I <sub>OUT</sub> =4.2mA)	-	0.4	V		

# TC514258P/J/Z-85, TC514258P/J/Z-10 TC514258P/J/Z-12

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

( $V_{CC}=5V\pm 10\%$ ,  $T_a=0\sim 70^\circ C$ ) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC514258P/J/Z-85		TC514258P/J/Z-10		TC514258P/J/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$t_{RC}$	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
$t_{RMW}$	Read-Modify-Write Cycle Time	225	-	255	-	295	-	ns	
$t_{SC}$	Static Column Mode Cycle Time	50	-	55	-	65	-	ns	
$t_{SRMW}$	Static Column Mode Read-Modify-Write Cycle Time	110	-	115	-	135	-	ns	
$t_{RAC}$	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
$t_{CAC}$	Access Time from $\overline{CS}$	-	30	-	30	-	35	ns	8,13
$t_{AA}$	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
$t_{ALW}$	Access Time from Last Write	-	85	-	95	-	115	ns	8,15
$t_{CLZ}$	$\overline{CS}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
$t_{OFF}$	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
$t_{AOH}$	Output Data Hold Time from Column Address	5	-	5	-	5	-	ns	
$t_{OW}$	Output Data Enable Time from $\overline{WRITE}$	-	30	-	30	-	35	ns	
$t_T$	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
$t_{RP}$	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
$t_{RAS}$	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
$t_{RASC}$	$\overline{RAS}$ Pulse Width (Static Column Mode)	85	100,000	100	100,000	120	100,000	ns	
$t_{RSH}$	$\overline{CS}$ to $\overline{RAS}$ Hold Time	30	-	30	-	35	-	ns	
$t_{CSH}$	$\overline{RAS}$ to $\overline{CS}$ Hold Time	85	-	100	-	120	-	ns	
$t_{CS}$	$\overline{CS}$ Pulse Width	30	10,000	30	10,000	35	10,000	ns	
$t_{CSC}$	$\overline{CS}$ Pulse Width (Static Column Mode)	30	100,000	30	100,000	35	100,000	ns	
$t_{RCD}$	$\overline{RAS}$ to $\overline{CS}$ Delay Time	25	55	25	70	25	85	ns	13
$t_{RAD}$	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
$t_{CRP}$	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
$t_{CPN}$	$\overline{CS}$ Precharge Time	15	-	15	-	20	-	ns	
$t_{CP}$	$\overline{CS}$ Precharge Time (Static Column Mode)	10	-	10	-	15	-	ns	
$t_{ASR}$	Row Address Set-up Time	0	-	0	-	0	-	ns	
$t_{RAH}$	Row Address Hold Time	15	-	15	-	15	-	ns	
$t_{ASC}$	Column Address Set-up Time	0	-	0	-	0	-	ns	
$t_{CAH}$	Column Address Hold Time	20	-	20	-	25	-	ns	
$t_{AWR}$	Write Address Hold Time Referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
$t_{AR}$	Column Address Hold Time Referenced to $\overline{RAS}$	100	-	115	-	140	-	ns	
$t_{RAL}$	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	
$t_{AH}$	Column Address Hold Time Referenced to $\overline{RAS}$ Rise	10	-	10	-	15	-	ns	16
$t_{LWAD}$	Last Write to Column Address Delay Time	25	40	25	45	30	55	ns	17

**TC514258P/J/Z-85, TC514258P/J/Z-10  
TC514258P/J/Z-12**

SYMBOL	PARAMETER	TC514258P/J/Z-85		TC514258P/J/Z-10		TC514258P/J/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t <sub>AHLW</sub>	Last Write to Column Address Hold Time	85	-	95	-	115	-	ns	
t <sub>RCS</sub>	Read Command Set-up Time Referenced to $\overline{CS}$	0	-	0	-	0	-	ns	
t <sub>RCH</sub>	Read Command Hold Time Referenced to $\overline{CS}$	0	-	0	-	0	-	ns	10
t <sub>RRH</sub>	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t <sub>WH</sub>	Write Command Hold Time (Output Data Disable)	0	-	0	-	0	-	ns	12
t <sub>WCR</sub>	Write Command Hold Time Referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t <sub>WP</sub>	$\overline{WRITE}$ Pulse Width	20	-	20	-	25	-	ns	
t <sub>WI</sub>	$\overline{WRITE}$ Inactive Time	10	-	10	-	15	-	ns	
t <sub>RWL</sub>	$\overline{WRITE}$ Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t <sub>CWL</sub>	$\overline{WRITE}$ Command to $\overline{CS}$ Lead Time	20	-	25	-	30	-	ns	
t <sub>DS</sub>	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
t <sub>DH</sub>	Data-In Hold Time	20	-	20	-	25	-	ns	11
t <sub>DHR</sub>	Data-In Hold Time Referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t <sub>REF</sub>	Refresh Period	-	8	-	8	-	8	ms	
t <sub>WS</sub>	$\overline{WRITE}$ Command Set-Up Time (Output Data Disable)	0	-	0	-	0	-	ns	12
t <sub>CWD</sub>	$\overline{CS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	65	-	65	-	75	-	ns	12
t <sub>RWD</sub>	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	120	-	135	-	160	-	ns	12
t <sub>AWD</sub>	Column Address to $\overline{WRITE}$ Delay Time	80	-	85	-	100	-	ns	12
t <sub>CSR</sub>	$\overline{CS}$ Set-Up Time ( $\overline{CS}$ before $\overline{RAS}$ )	10	-	10	-	10	-	ns	
t <sub>CHR</sub>	$\overline{CS}$ Hold Time ( $\overline{CS}$ before $\overline{RAS}$ )	30	-	30	-	30	-	ns	
t <sub>RPC</sub>	$\overline{RAS}$ to $\overline{CS}$ Precharge Time	0	-	0	-	0	-	ns	
t <sub>CPT</sub>	$\overline{CS}$ Precharge Time ( $\overline{CS}$ before $\overline{RAS}$ counter Test Cycle)	50	-	50	-	60	-	ns	
t <sub>ROH</sub>	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	20	-	20	-	20	-	ns	
t <sub>OEA</sub>	$\overline{OE}$ Access Time	-	30	-	35	-	45	ns	
t <sub>OED</sub>	$\overline{OE}$ to Data Delay	25	-	25	-	30	-	ns	
t <sub>OEZ</sub>	Output Buffer turn off Delay Time from $\overline{OE}$	0	25	0	25	0	30	ns	9
t <sub>OEH</sub>	$\overline{OE}$ Command Hold Time	25	-	25	-	30	-	ns	

# TC514258P/J/Z-85, TC514258P/J/Z-10 TC514258P/J/Z-12

CAPACITANCE ( $V_{CC}=5V\pm 10\%$ ,  $f=1\text{MHz}$ ,  $T_a=0\sim 70^\circ\text{C}$ )

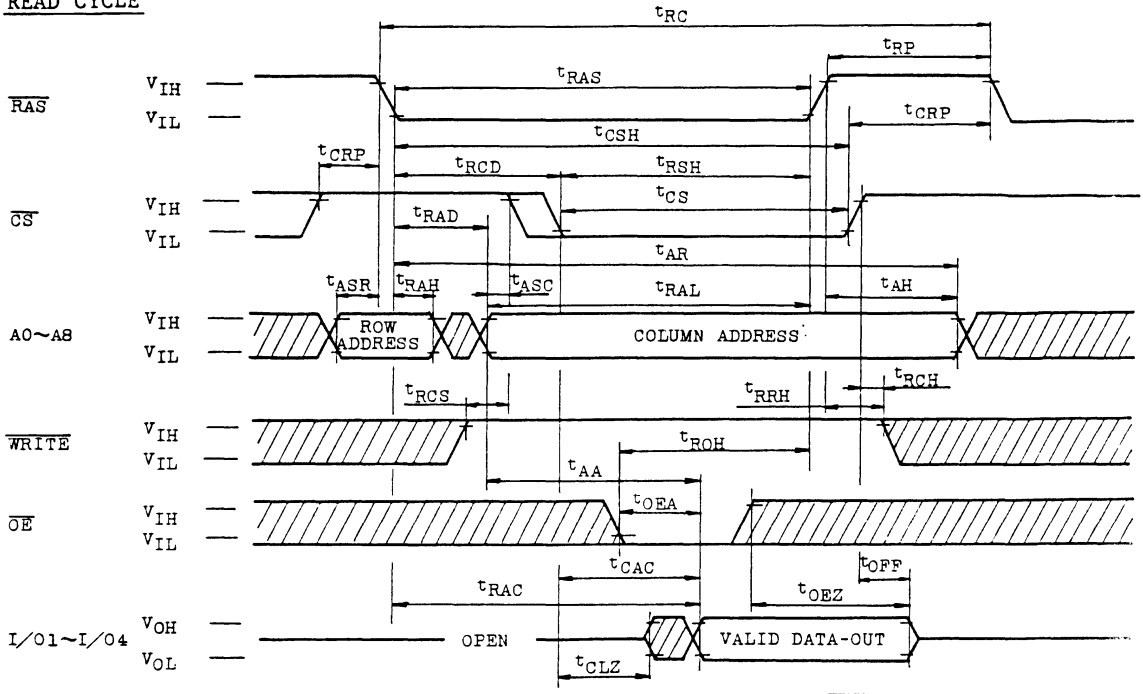
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C <sub>I1</sub>	Input Capacitance ( $A_0 \sim A_8$ )	-	5	pF
C <sub>I2</sub>	Input Capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CS}}$ , $\overline{\text{WRITE}}$ , $\overline{\text{OE}}$ )	-	7	
C <sub>O</sub>	Output Capacitance ( $I/O_1 \sim I/O_4$ )	-	7	

## NOTES:

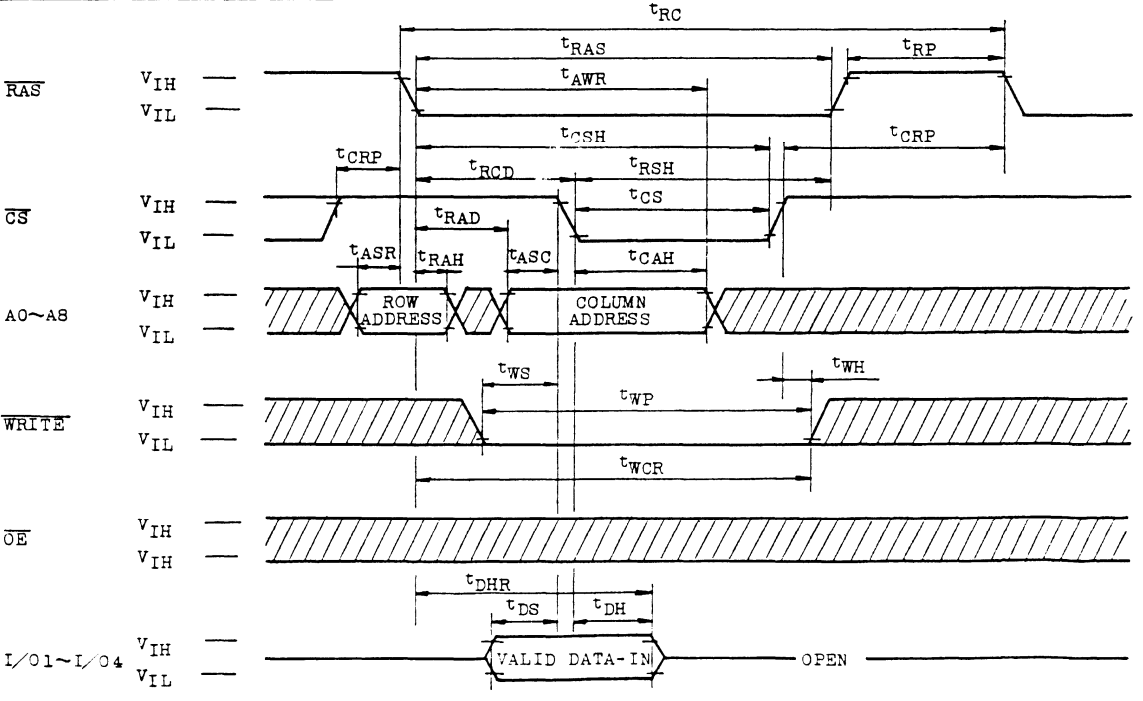
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltage are referenced to  $V_{SS}$ .
3.  $I_{cc1}$ ,  $I_{cc3}$ ,  $I_{cc4}$ ,  $I_{cc6}$  depend on cycle rate.
4.  $I_{cc1}$ ,  $I_{cc4}$  depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200 $\mu\text{s}$  is required after power-up followed by 8  $\overline{\text{RAS}}$  cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{\text{CS}}$  Before  $\overline{\text{RAS}}$  initialization cycles instead of 8  $\overline{\text{RAS}}$  cycles are required.
6. AC measurements assume  $t_T=5\text{ns}$ .
7.  $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$  are reference levels for measuring timing of input signals.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9.  $t_{OFF}(\text{max.})$  and  $t_{OEZ}(\text{max.})$  define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
11. These parameters are referenced to  $\overline{\text{CS}}$  leading edge in early write cycles and to  $\overline{\text{WRITE}}$  leading edge in Read-Modify-Write cycles.
12.  $t_{WS}$ ,  $t_{WH}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If  $t_{WS}\geq t_{WS}(\text{min.})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If  $t_{RWD}\geq t_{RWD}(\text{min.})$ ,  $t_{CWD}\geq t_{CWD}(\text{min.})$  and  $t_{AWD}\geq t_{AWD}(\text{min.})$ , the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the  $t_{RCD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled by  $t_{CAC}$ .
14. Operation within the  $t_{RAD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only: If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled by  $t_{AA}$ .
15. Operation within the  $t_{LWAD}(\text{max.})$  limit insures that  $t_{ALW}(\text{max.})$  can be met.  $t_{LWAD}(\text{max.})$  is specified as a reference point only: If  $t_{LWAD}$  is greater than the specified  $t_{LWAD}(\text{max.})$  limit, then access time is controlled exclusively by  $t_{AA}$ .
16.  $t_{AH}$  is the condition to latch column address when  $\overline{\text{RAS}}$  has risen up.

# TC514258P/J/Z-85, TC514258P/J/Z-10 TC514258P/J/Z-12

## READ CYCLE

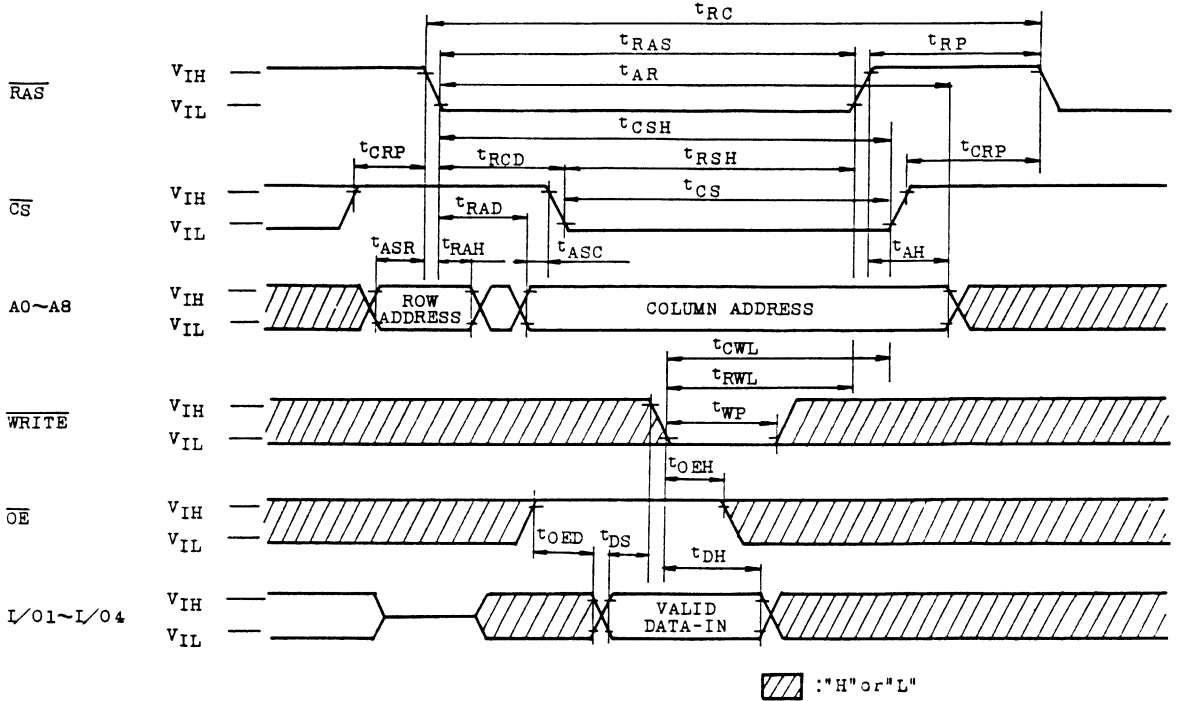


## WRITE CYCLE (EARLY WRITE)

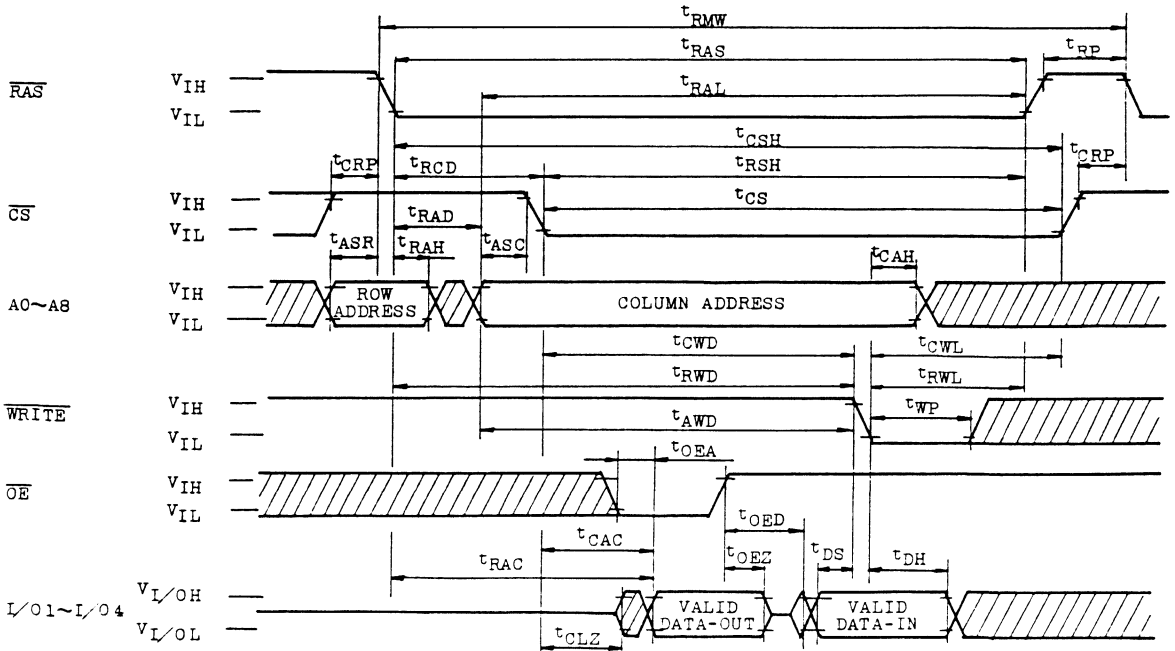


# TC514258P/J/Z-85, TC514258P/J/Z-10 TC514258P/J/Z-12

## WRITE CYCLE ( $\overline{OE}$ CONTROLLED WRITE)

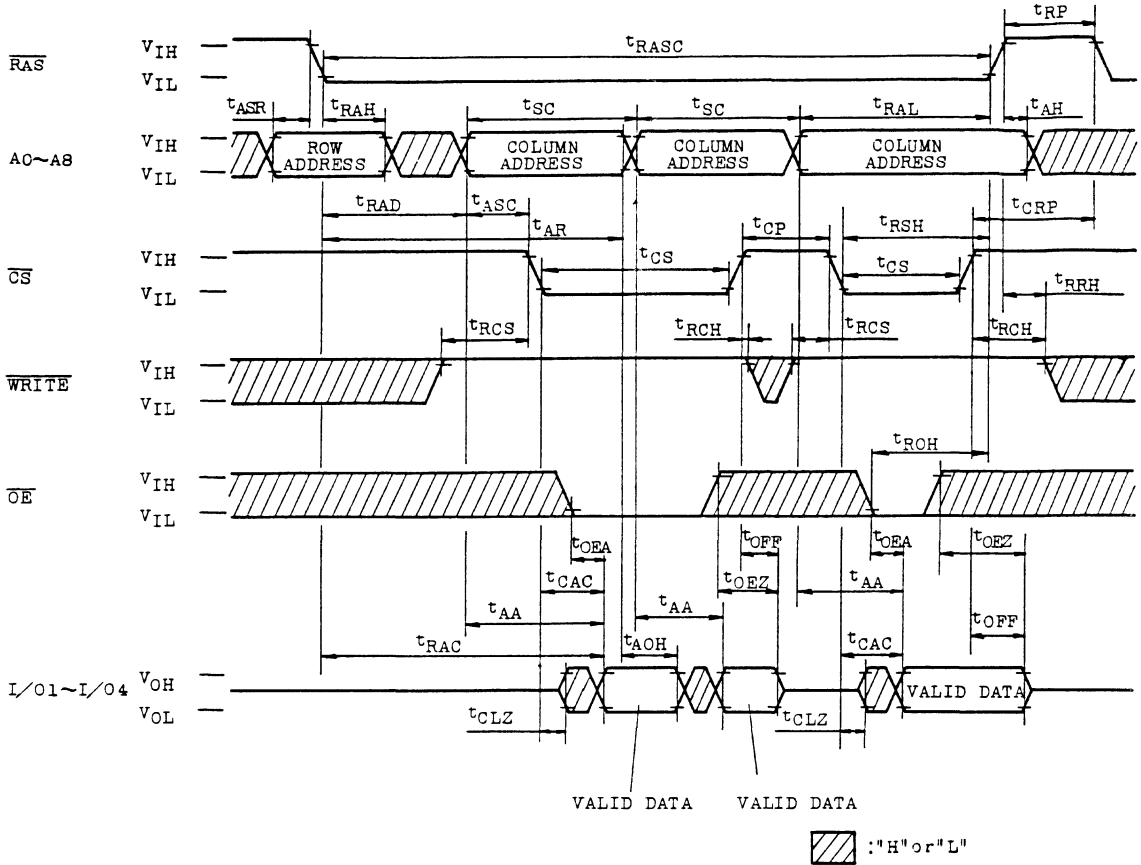


## READ-MODIFY-WRITE CYCLE



# TC514258P/J/Z-85, TC514258P/J/Z-10 TC514258P/J/Z-12

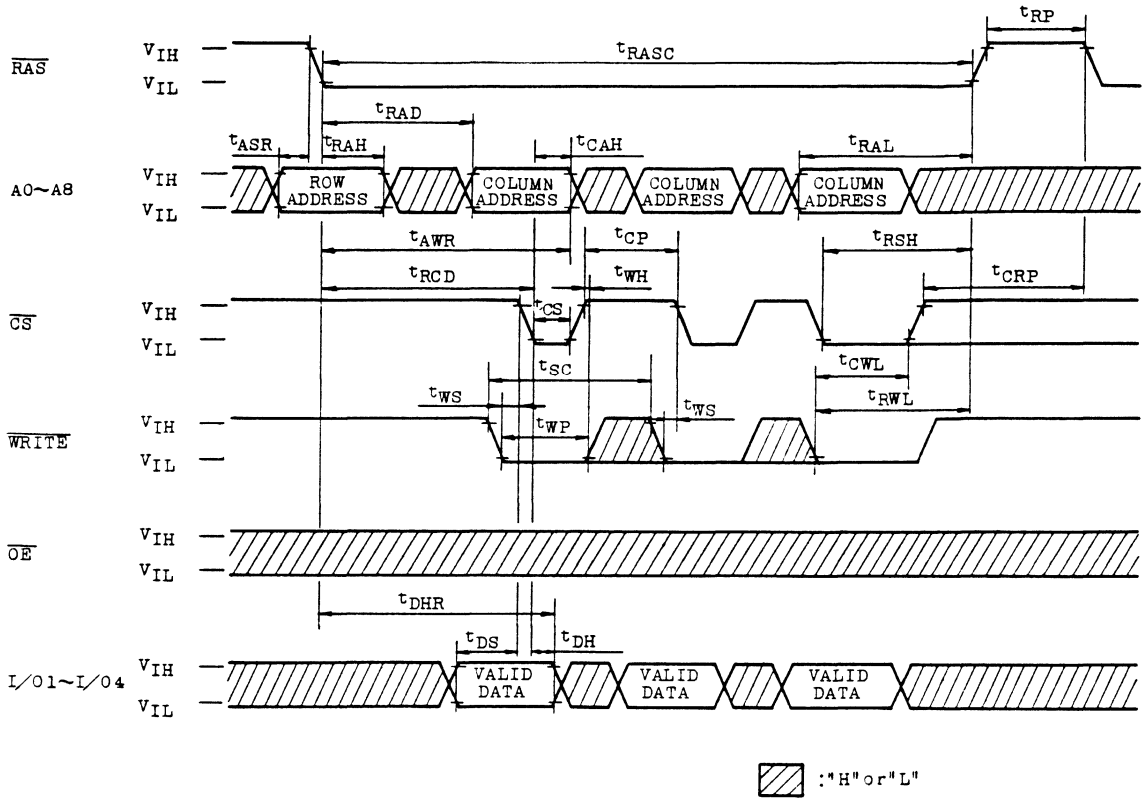
## STATIC COLUMN MODE READ CYCLE





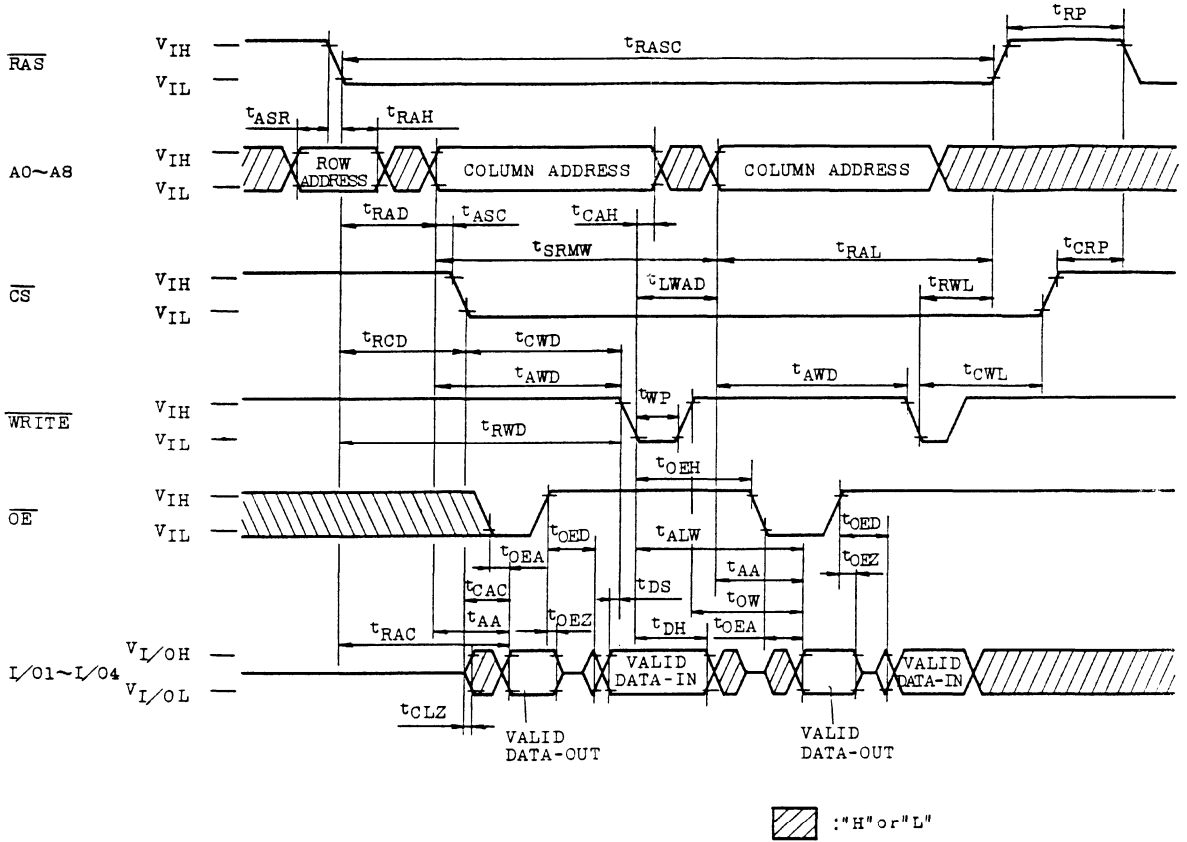
# TC514258P/J/Z-85, TC514258P/J/Z-10 TC514258P/J/Z-12

## STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



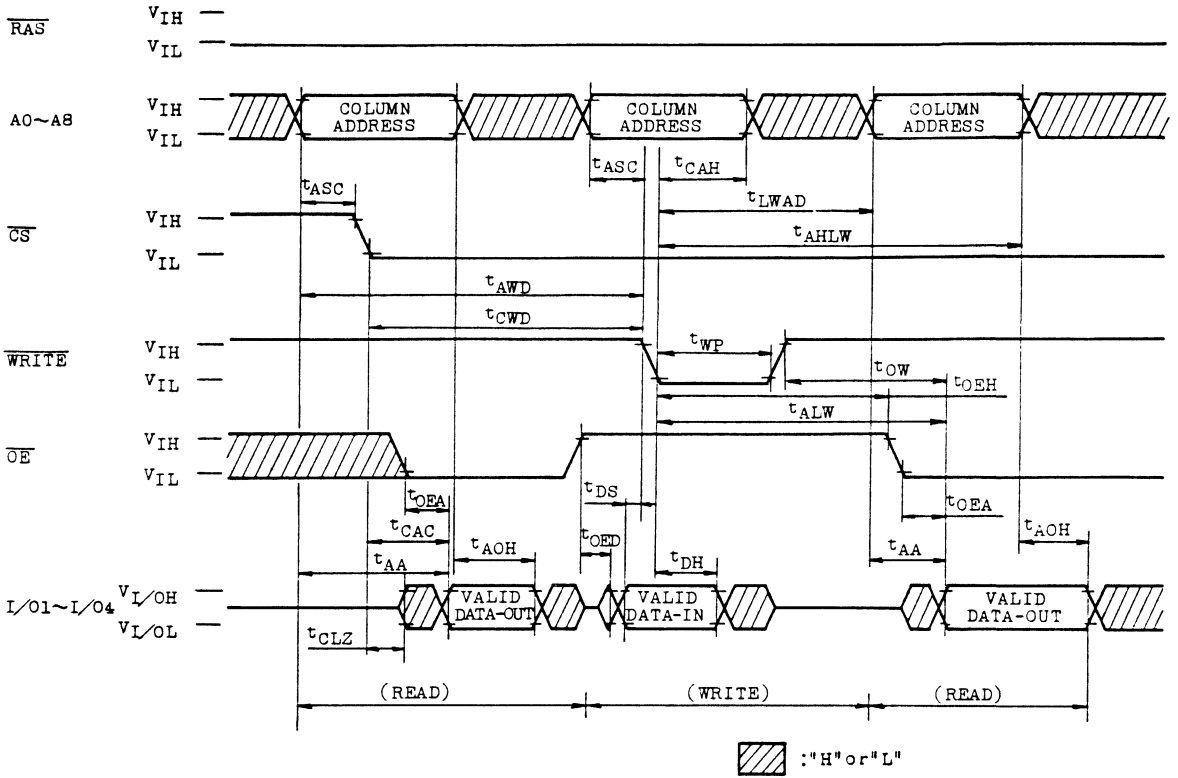
# TC514258P/J/Z-85, TC514258P/J/Z-10 TC514258P/J/Z-12

## STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



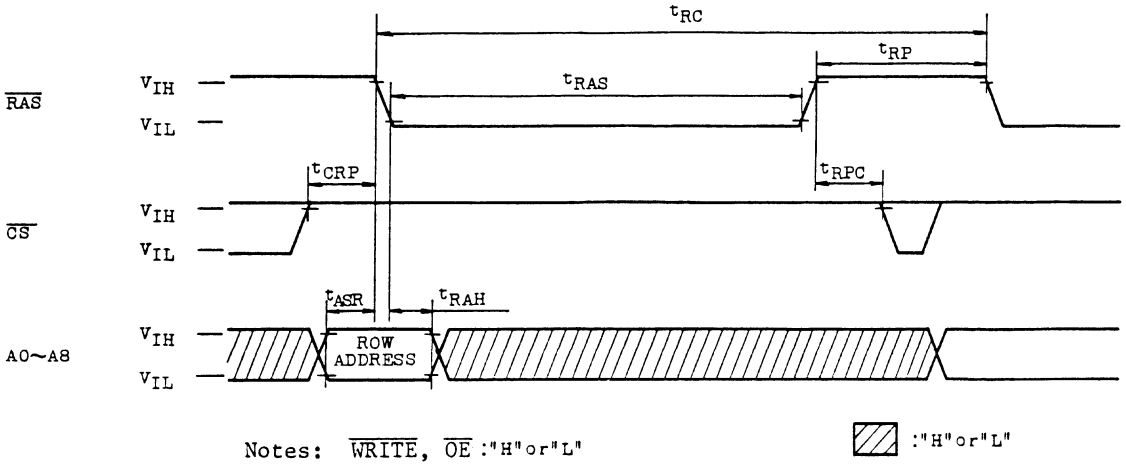
# TC514258P/J/Z-85, TC514258P/J/Z-10 TC514258P/J/Z-12

## STATIC COLUMN MODE READ/WRITE MIXED CYCLE

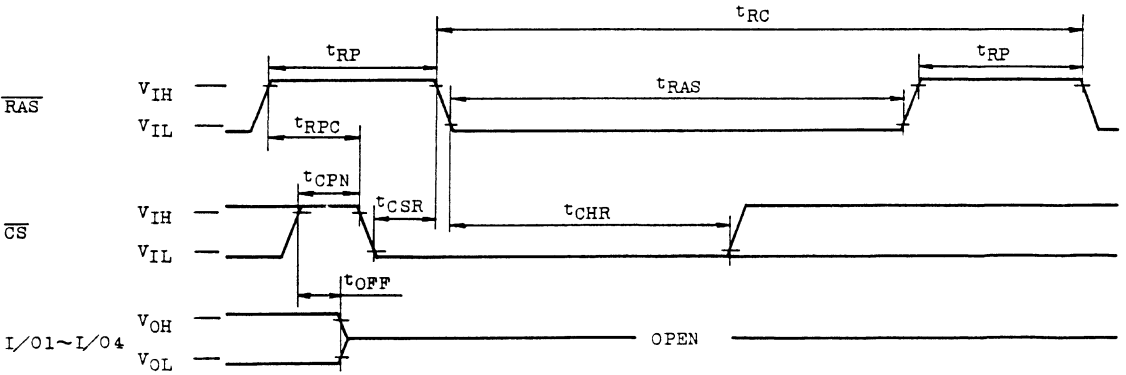


# TC514258P/J/Z-85, TC514258P/J/Z-10 TC514258P/J/Z-12

## RAS ONLY REFRESH CYCLE

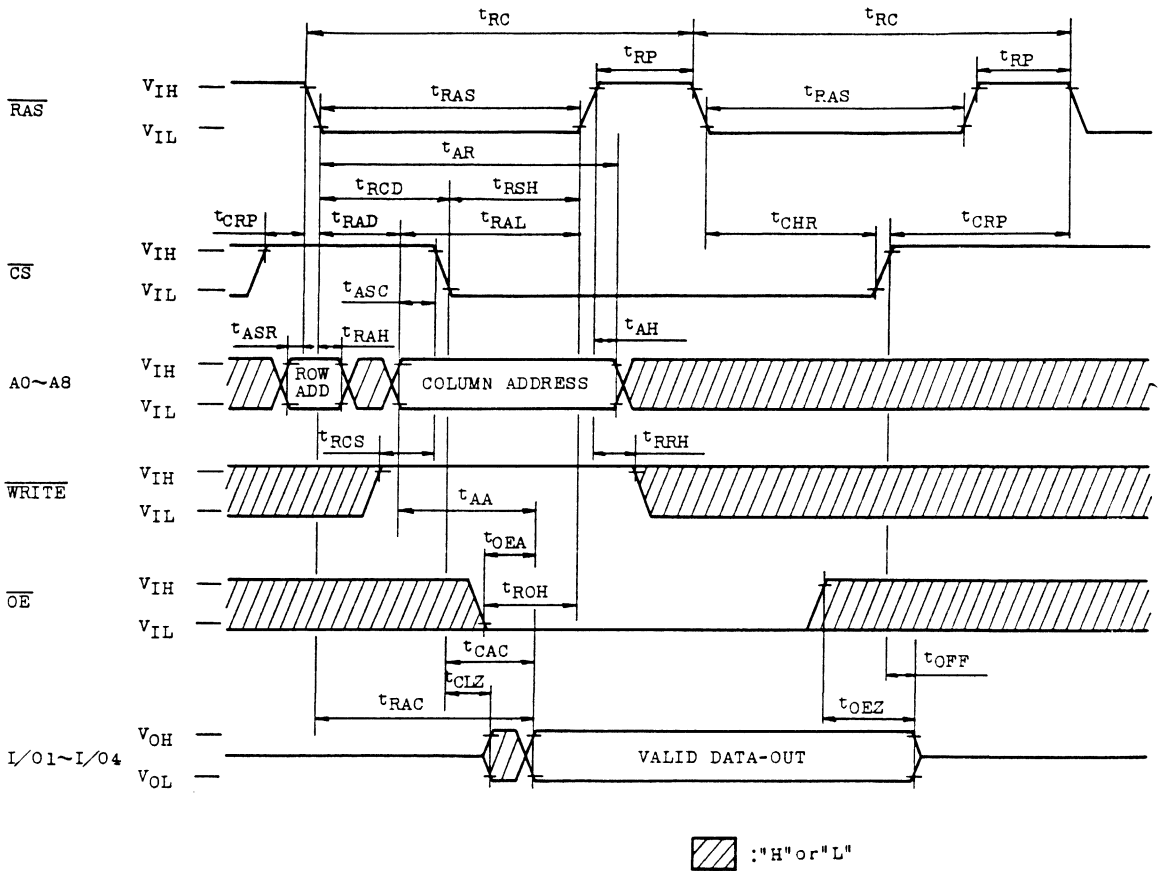


## CS BEFORE RAS REFRESH CYCLE



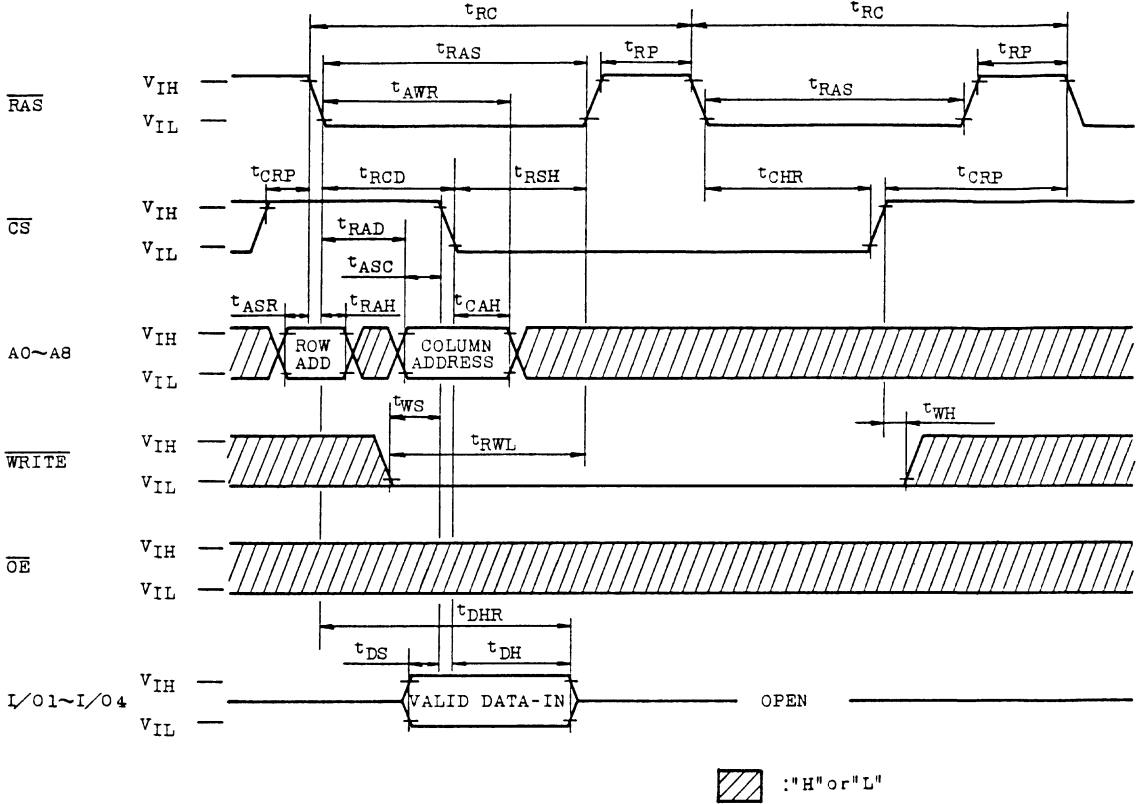
# TC514258P/J/Z-85, TC514258P/J/Z-10 TC514258P/J/Z-12

## HIDDEN REFRESH CYCLE (READ)



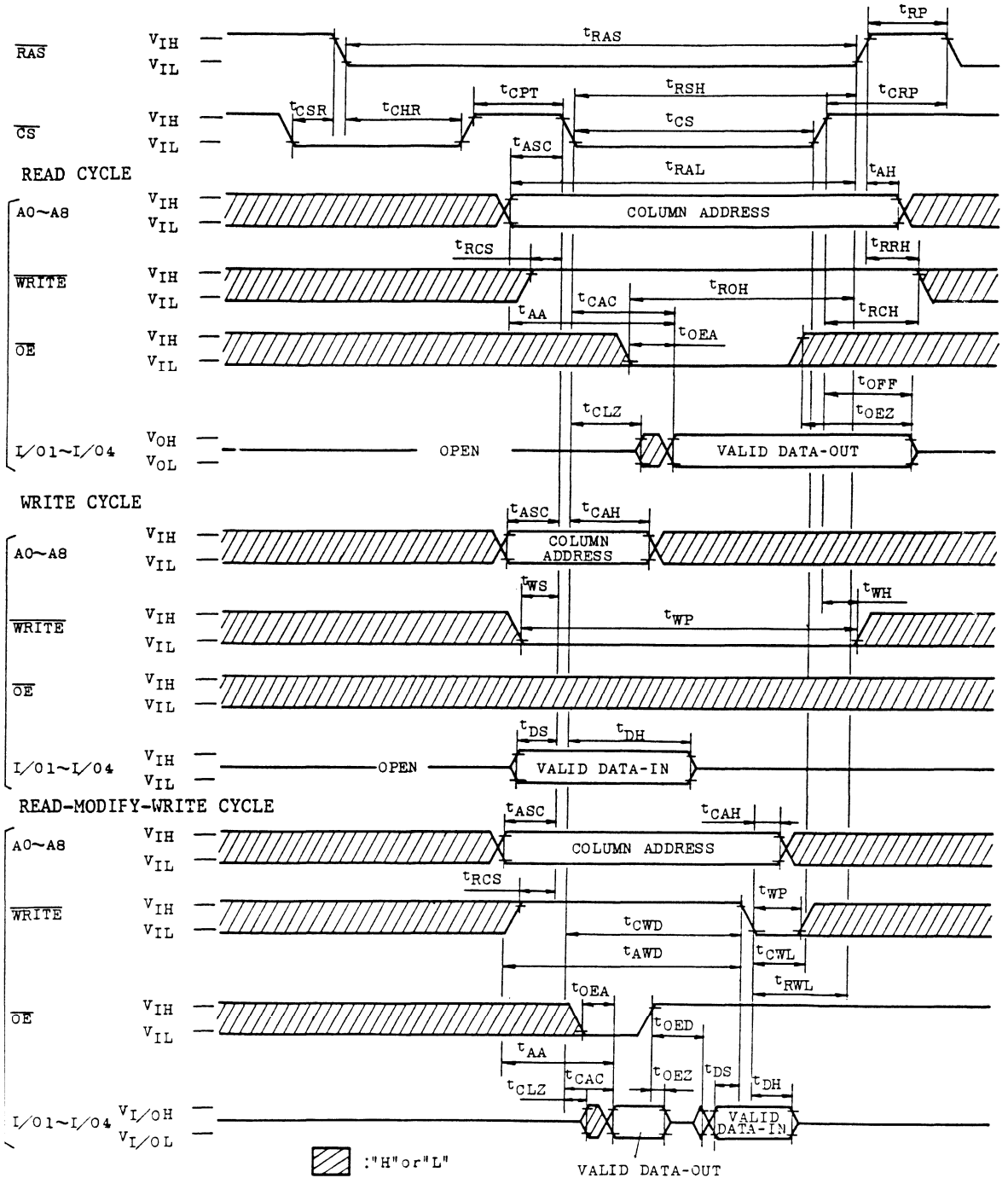
# TC514258P/J/Z-85, TC514258P/J/Z-10 TC514258P/J/Z-12

## HIDDEN REFRESH CYCLE (WRITE)



# TC514258P/J/Z-85, TC514258P/J/Z-10 TC514258P/J/Z-12

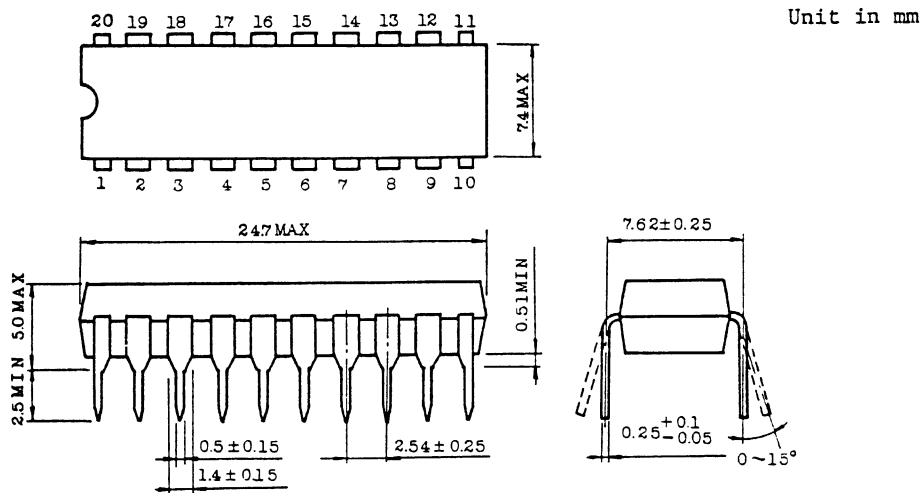
## CS BEFORE RAS REFRESH COUNTER TEST CYCLE



# TC514258P/J/Z-85, TC514258P/J/Z-10 TC514258P/J/Z-12

## OUTLINE DRAWINGS

- Plastic DIP



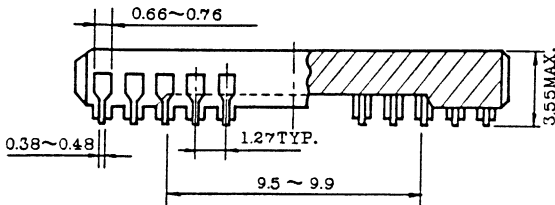
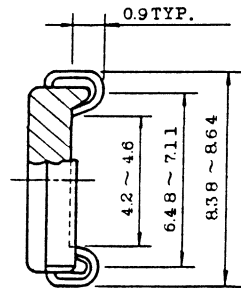
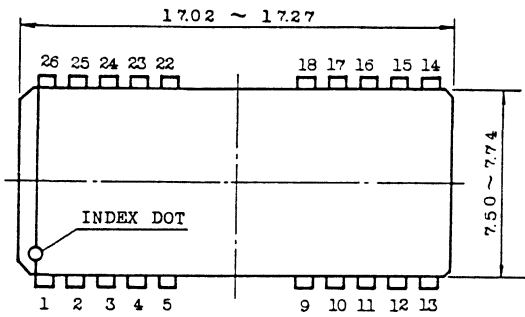
Note: Each lead pitch is 2.54mm.  
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.20 leads.  
All dimensions are in millimeters.



# TC514258P/J/Z-85, TC514258P/J/Z-10 TC514258P/J/Z-12

• Plastic SOJ

Unit in mm



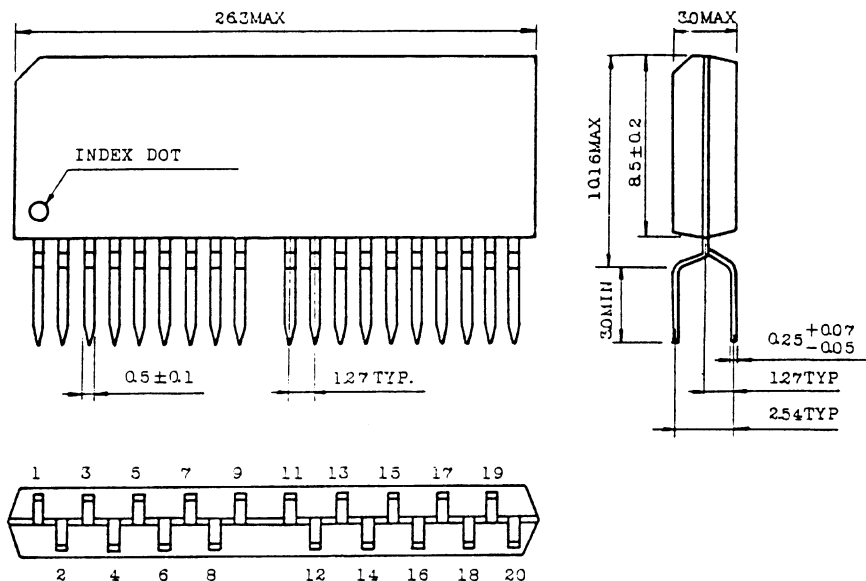
Note: Each lead pitch 1.27mm. All dimensions are in millimeters.

Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

# TC514258P/J/Z-85, TC514258P/J/Z-10 TC514258P/J/Z-12

• Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.

All dimensions are in millimeters.

Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

# TOSHIBA MOS MEMORY PRODUCT

1,048,576 WORDS × 8 BIT  
DYNAMIC RAM MODULE

THM81000S/L-10/12

## DESCRIPTION

The THM81000S/L is a 1,048,576 words by 8 bits dynamic RAM module which assembled 8 pcs of TC511000J on the printed circuit board.

The THM81000S/L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

## FEATURES

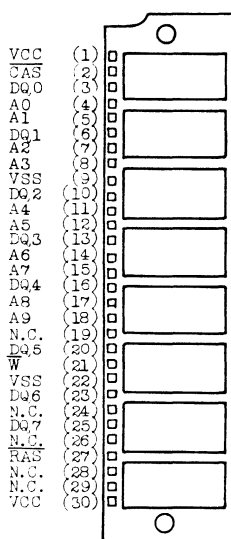
- 1,048,576 words by 8 bits organization
- Fast access time

	THM81000S/L-10	THM81000S/L-12
$t_{RAC}$ $\overline{RAS}$ Access Time	100ns	120ns
$t_{AA}$ Column Address Access Time	50ns	60ns
$t_{CAC}$ $\overline{CAS}$ Access Time	35ns	45ns
$t_{RC}$ Cycle Time	190ns	220ns
$t_{PC}$ Fast Page Mode Cycle Time	55ns	70ns

- Single power supply of 5V±10%
- Low power
  - 2,640mW MAX. Operating (THM81000S/L-10)
  - 2,200mW MAX. Operating (THM81000S/L-12)
  - 44mW MAX. Standby
- $\overline{CAS}$  before  $\overline{RAS}$  refresh,  $\overline{RAS}$  only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms

## PIN CONNECTION

(TOP VIEW)

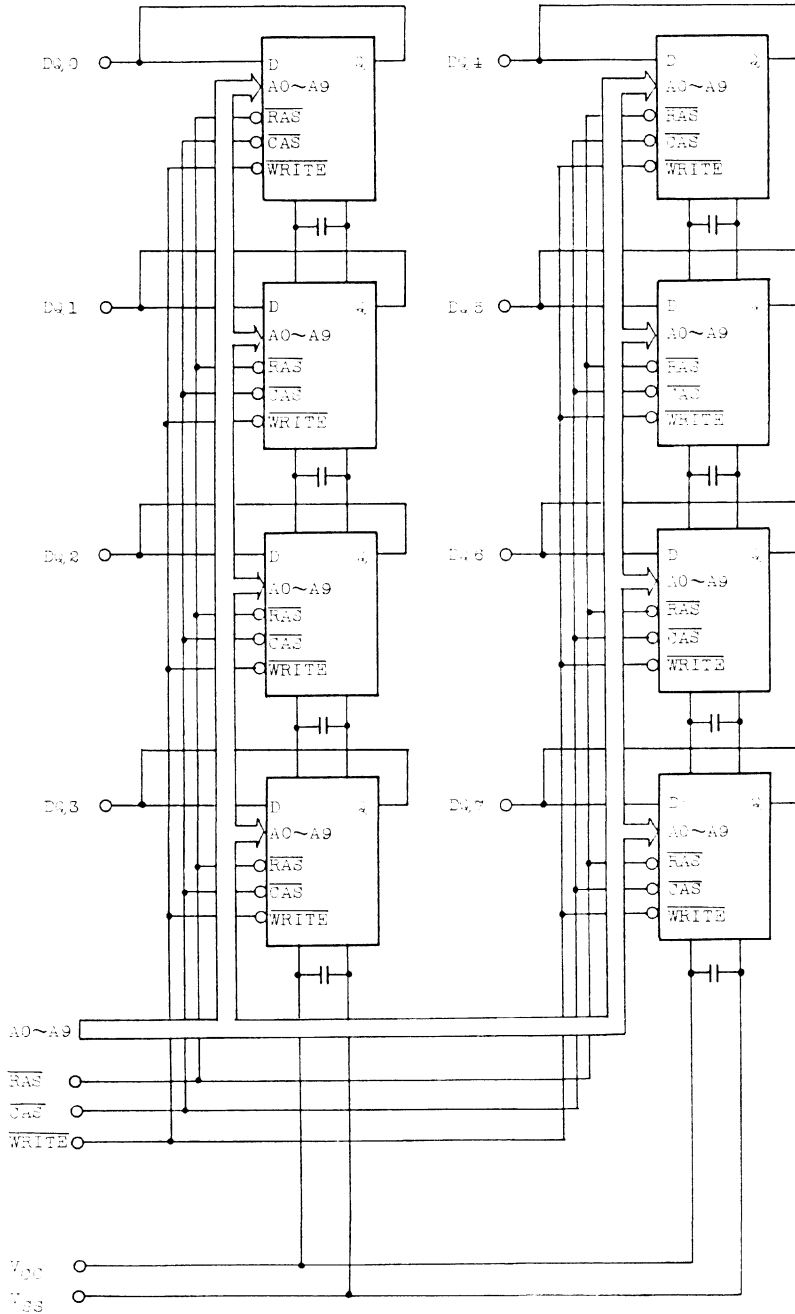


## PIN NAMES

A0 ~ 9	Address Inputs
DQ0 ~ 7	Data Input/Outputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
VCC	Power (+5V)
VSS	Ground
N.C.	No Connection

# THM81000S/L-10/12

BLOCK DIAGRAM



# THM81000S/L-10/12

## ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	$V_{IN}$	-1 ~ 7	V	1
Output Voltage	$V_{OUT}$	-1 ~ 7	V	1
Power Supply Voltage	$V_{CC}$	-1 ~ 7	V	1
Operating Temperature	$T_{OPR}$	0 ~ 70	°C	1
Storage Temperature	$T_{STG}$	-55 ~ 125	°C	1
Soldering Temperature . Time	$T_{SOLDER}$	260 · 10	°C · sec	1
Power Dissipation	$P_D$	4.8	W	1
Short Circuit Output Current	$I_{OUT}$	50	mA	1

## RECOMMENDED DC OPERATING CONDITIONS ( $T_a=0 \sim 70^\circ\text{C}$ )

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
$V_{CC}$	Supply Voltage	4.5	5.0	5.5	V	2
$V_{IH}$	Input High Voltage	2.4		6.5	V	2
$V_{IL}$	Input Low Voltage	-1.0		0.8	V	2

## DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ , $T_a=0 \sim 70^\circ\text{C}$ )

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES	
$I_{CC1}$	OPERATING CURRENT Average Power Supply Operating Current ( $\overline{RAS}$ , $\overline{CAS}$ , Address Cycling: $t_{RC}=t_{RC \text{ MIN.}}$ )	THM81000S/L-10	-	480	mA	3, 4
		THM81000S/L-12	-	400		
$I_{CC2}$	STANDBY CURRENT Power Supply Standby Current ( $\overline{RAS}=\overline{CAS}=V_{IH}$ )		-	16	mA	
$I_{CC3}$	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ( $\overline{RAS}$ Cycling, $\overline{CAS}=V_{IH}$ : $t_{RC}=t_{RC \text{ MIN.}}$ )	THM81000S/L-10	-	480	mA	3
		THM81000S/L-12	-	400		
$I_{CC4}$	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ( $\overline{RAS}=V_{IL}$ , $\overline{CAS}$ Address Cycling: $t_{PC}=t_{PC \text{ MIN.}}$ )	THM81000S/L-10	-	320	mA	3, 4
		THM81000S/L-12	-	240		
$I_{CC5}$	STANDBY CURRENT Power Supply Standby Current ( $\overline{RAS}=\overline{CAS}=V_{CC}-0.2V$ )		-	8	mA	
$I_{CC6}$	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ( $\overline{RAS}$ , $\overline{CAS}$ Cycling: $t_{RC}=t_{RC \text{ MIN.}}$ )	THM81000S/L-10	-	480	mA	3
		THM81000S/L-12	-	400		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input ( $0V \leq V_{IN} \leq 6.5V$ , All Other Pins not under Test=0V)		-80	80	$\mu\text{A}$	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT ( $\overline{DOUT}$ is disabled, $0V \leq V_{OUT} \leq 5.5V$ )		-20	20	$\mu\text{A}$	
$V_{OH}$	OUTPUT LEVEL Output "H" Level Voltage ( $I_{OUT}=-5\text{mA}$ )		2.4	-	V	
$V_{OL}$	OUTPUT LEVEL Output "L" Level Voltage ( $I_{OUT}=4.2\text{mA}$ )		-	0.4	V	

# THM81000S/L-10/12

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

( $V_{CC}=5V\pm 10\%$ ,  $T_a=0\sim 70^\circ C$ ) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM81000S/L-10		THM81000S/L-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
$t_{RC}$	Random Read or Write Cycle Time	190		220		ns	
$t_{PC}$	Fast Page Mode Cycle Time	55		70		ns	
$t_{RAC}$	Access Time from $\overline{RAS}$		100		120	ns	8, 13
$t_{CAC}$	Access Time from $\overline{CAS}$		35		45	ns	8, 13
$t_{AA}$	Access Time from Column Address		50		60	ns	8, 14
$t_{CPA}$	Access Time from $\overline{CAS}$ Precharge		50		65	ns	8
$t_{CLZ}$	$\overline{CAS}$ to Output in Low-Z	5		5		ns	8
$t_{OFF}$	Output Buffer Turn-off Delay	0	30	0	35	ns	9
$t_T$	Transition Time (Rise and Fall)	3	50	3	50	ns	7
$t_{RP}$	$\overline{RAS}$ Precharge Time	80		90		ns	
$t_{RAS}$	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000	ns	
$t_{RASP}$	$\overline{RAS}$ Pulse Width (Fast Page Mode)	100	100,000	120	100,000	ns	
$t_{RSH}$	$\overline{RAS}$ Hold Time	35		45		ns	
$t_{CSH}$	$\overline{CAS}$ Hold Time	100		120		ns	
$t_{CAS}$	$\overline{CAS}$ Pulse Width	35		45		ns	
$t_{RCD}$	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	65	25	75	ns	13
$t_{RAD}$	$\overline{RAS}$ to Column Address Delay Time	20	50	20	60	ns	14
$t_{CRP}$	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10		ns	
$t_{CP}$	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		15		ns	
$t_{ASR}$	Row Address Set-Up Time	0		0		ns	
$t_{RAH}$	Row Address Hold Time	15		15		ns	
$t_{ASC}$	Column Address Set-Up Time	0		0		ns	
$t_{CAH}$	Column Address Hold Time	20		25		ns	
$t_{AR}$	Column Address Hold Time referenced to $\overline{RAS}$	75		90		ns	
$t_{RAL}$	Column Address to $\overline{RAS}$ Lead Time	50		60		ns	
$t_{RCS}$	Read Command Set-Up Time	0		0		ns	
$t_{RCH}$	Read Command Hold Time	0		0		ns	10

# THM81000S/L-10/12

## ELECTRICAL CHARACTERISTIC AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM81000S/L-10		THM81000S/L-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
$t_{RRH}$	Read Command Hold Time referenced to $\overline{RAS}$	0		0		ns	10
$t_{WCH}$	Write Command Hold Time	20		25		ns	
$t_{WCR}$	Write Command Hold Time referenced to $\overline{RAS}$	75		90		ns	
$t_{WP}$	Write Command Pulse Width	20		25		ns	
$t_{RWL}$	Write Command to $\overline{RAS}$ Lead Time	25		30		ns	
$t_{CWL}$	Write Command to $\overline{CAS}$ Lead Time	25		30		ns	
$t_{DS}$	Data Set-Up Time	0		0		ns	11
$t_{DH}$	Data Hold Time	20		25		ns	11
$t_{DHR}$	Data Hold Time referenced to $\overline{RAS}$	75		90		ns	
$t_{REF}$	Refresh Period		8		8	ms	
$t_{WCS}$	Write Command Set-Up Time	0		0		ns	12
$t_{CSR}$	$\overline{CAS}$ Set-Up Time ( $\overline{CAS}$ before $\overline{RAS}$ Cycle)	10		10		ns	
$t_{CHR}$	$\overline{CAS}$ Hold Time ( $\overline{CAS}$ before $\overline{RAS}$ Cycle)	30		30		ns	
$t_{RPC}$	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		ns	
$t_{CPT}$	$\overline{CAS}$ Precharge Time ( $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50		60		ns	
$t_{CPN}$	$\overline{CAS}$ Precharge Time	15		20		ns	

### CAPACITANCE ( $V_{CC}=5V\pm 10\%$ , $f=1MHz$ , $T_a=0\sim 70^\circ C$ )

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$C_{I1}$	Input Capacitance ( $A0\sim A9, \overline{W}, \overline{CAS}, \overline{RAS}$ )		60	pF
$C_{DQ}$	I/O Capacitance ( $DQ0\sim DQ7$ )		15	pF

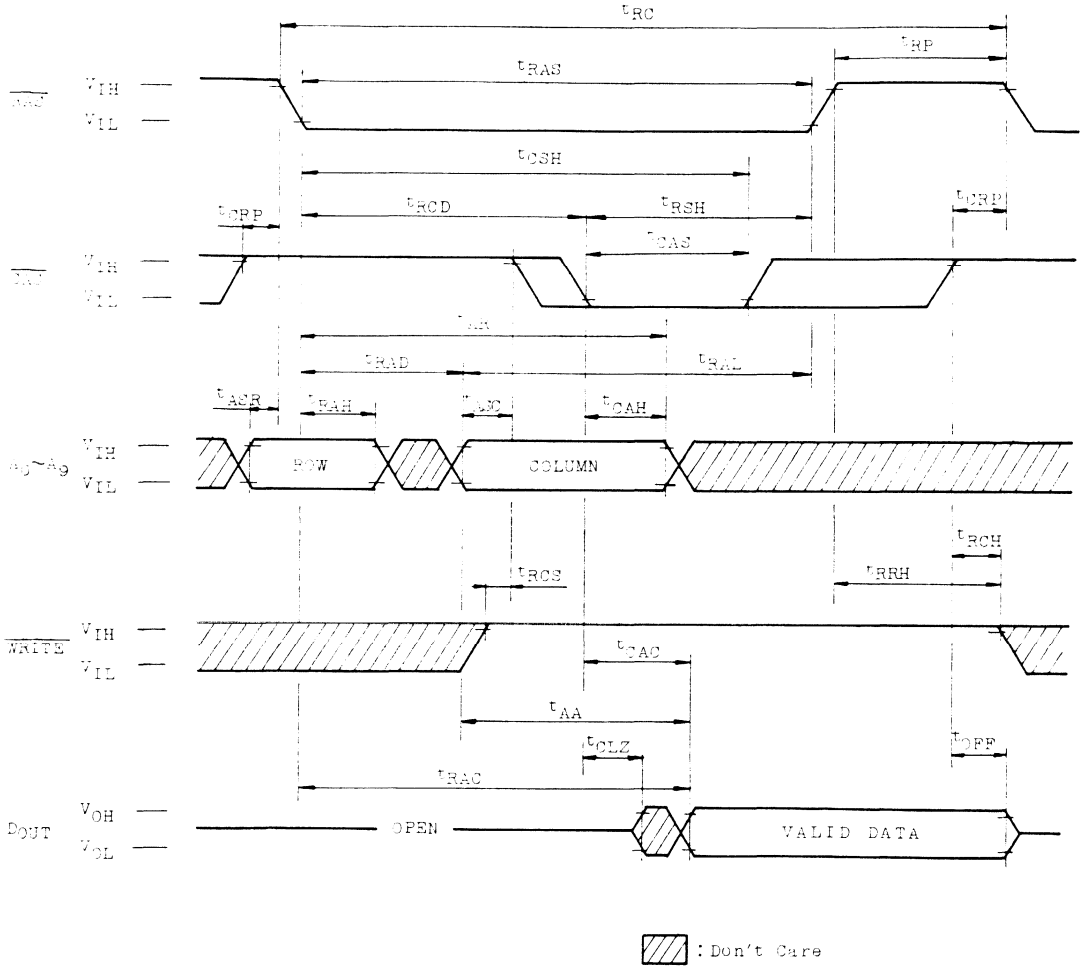
## THM81000S/L-10/12

### NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to  $V_{SS}$ .
3.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ ,  $I_{CC6}$  depend on cycle rate.
4.  $I_{CC1}$ ,  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200 $\mu$ s is required after power-up followed by 8  $\overline{RAS}$  cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{CAS}$  before  $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
6. AC measurements assume  $t_T=5$ ns.
7.  $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9.  $t_{OFF}(\text{max.})$  defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
11. These parameters are referenced to  $\overline{CAS}$  leading edge in early write cycles and to  $\overline{WRITE}$  leading edge in read-write cycles.
12.  $t_{WCS}$  is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the cycle is an early write cycle and data out pin will remain open circuit (high impedance).
13. Operation within the  $t_{RCD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled by  $t_{CAC}$ .
14. Operation within the  $t_{RAD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only: If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled by  $t_{AA}$ .

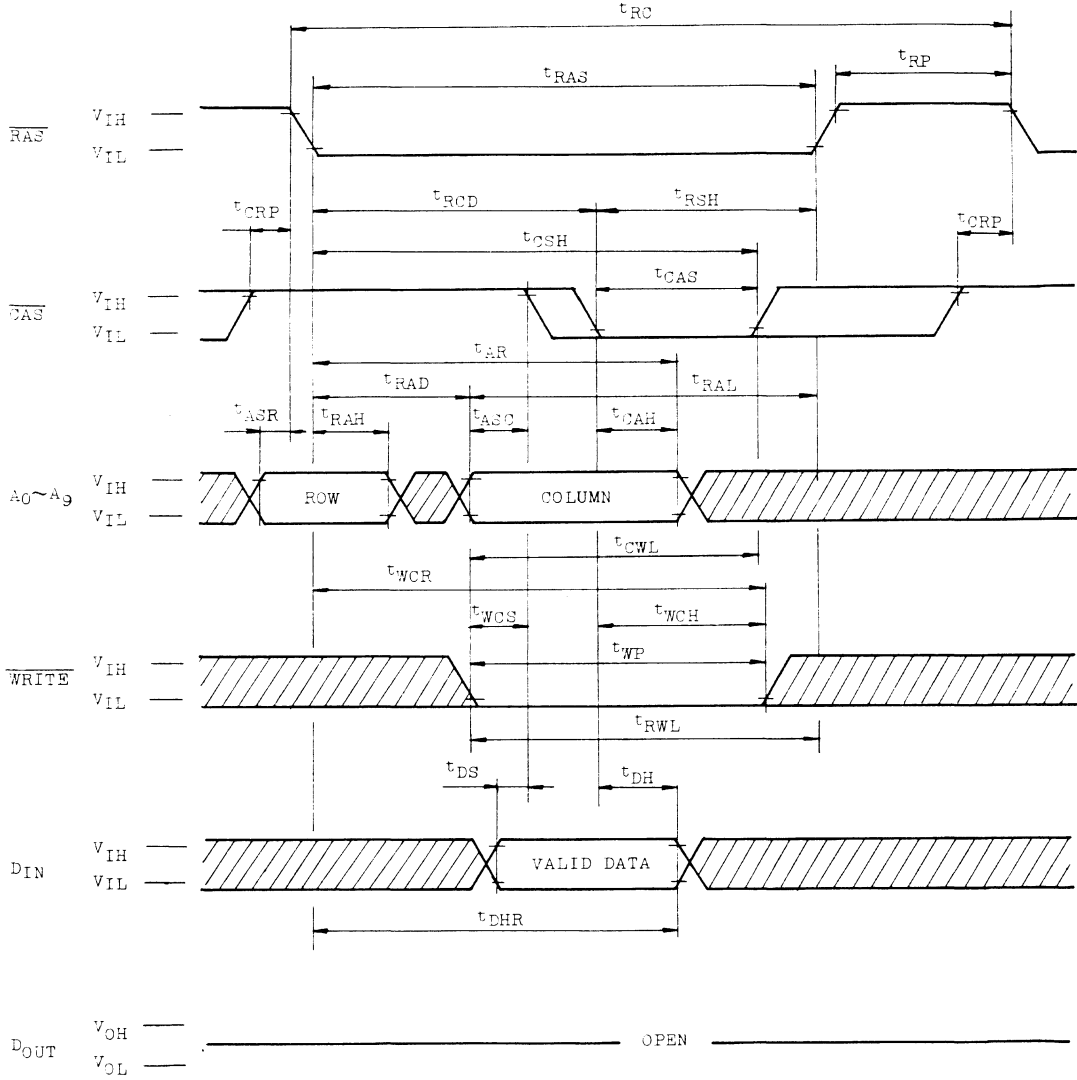



READ CYCLE



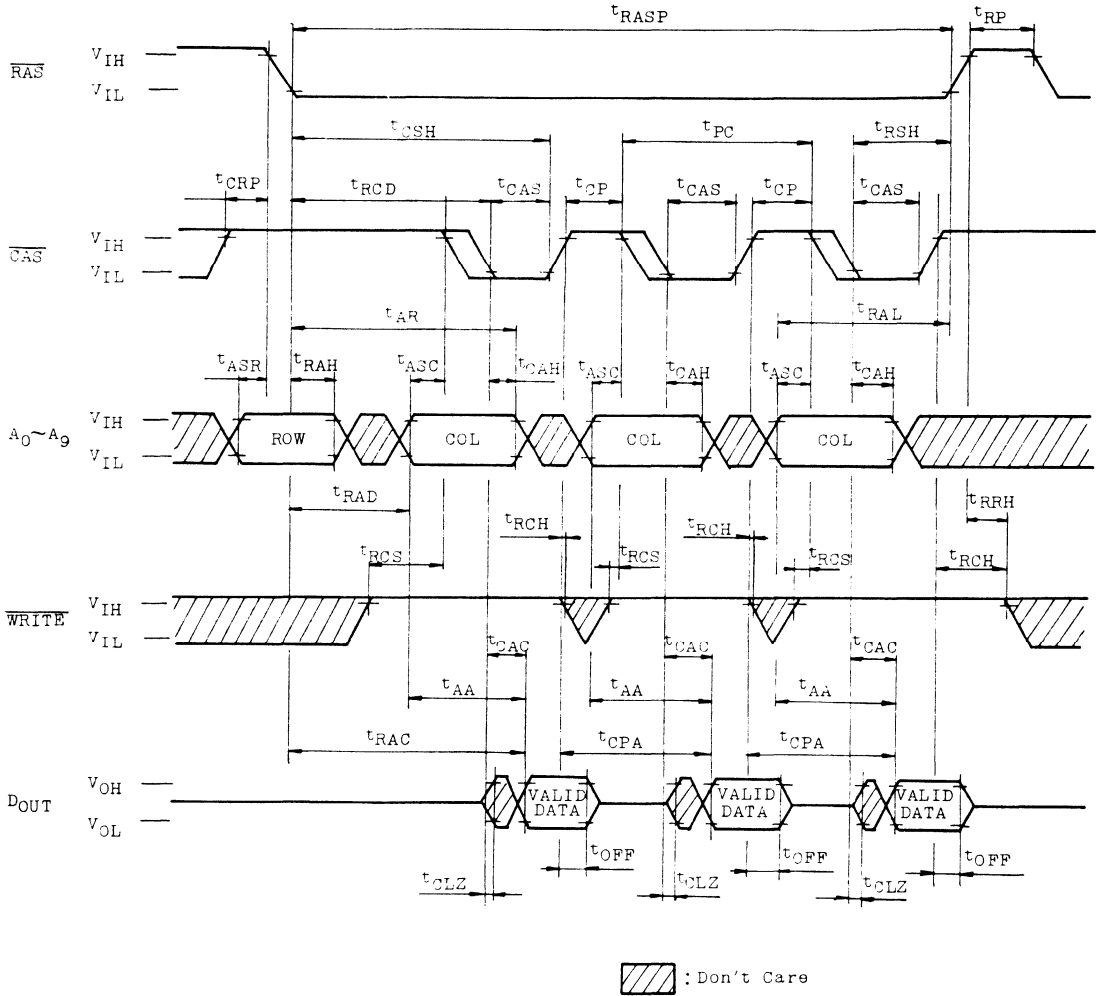
# THM81000S/L-10/12

## EARLY WRITE CYCLE



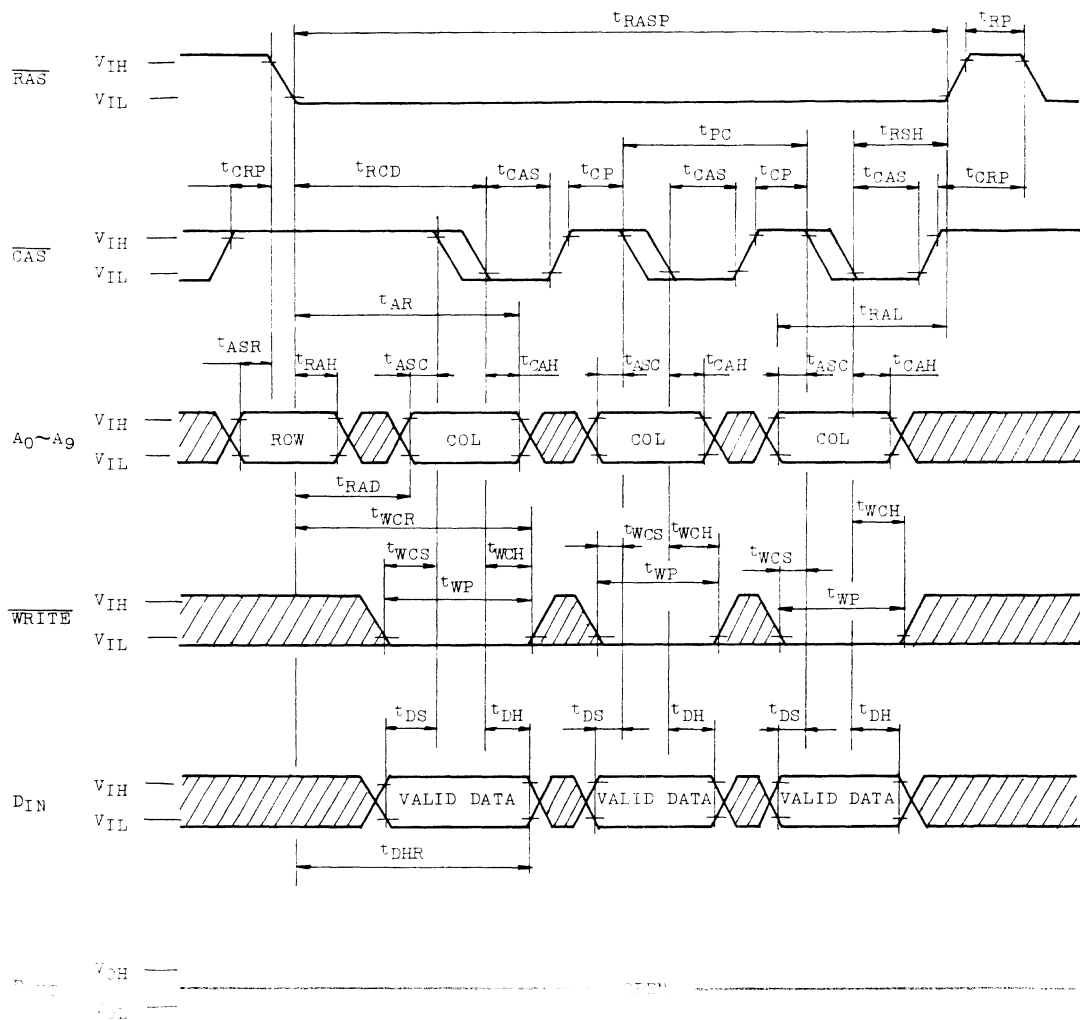
 : Don't Care

FAST PAGE MODE READ CYCLE

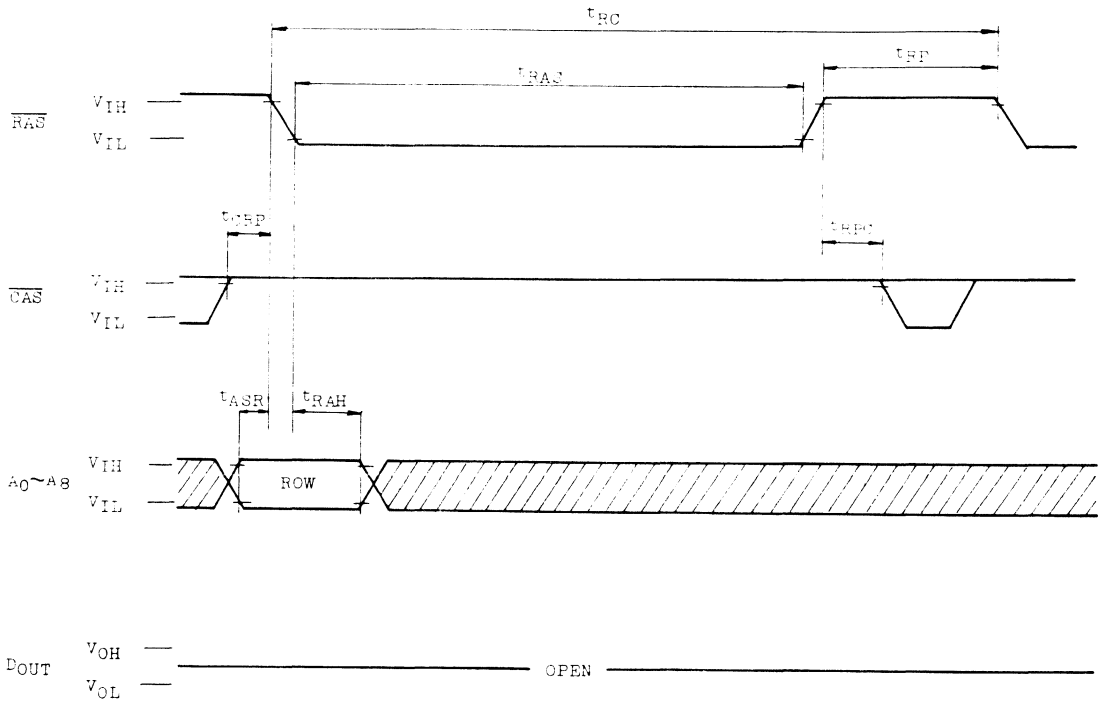



# THM81000S/L-10/12

## FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



RAS ONLY REFRESH CYCLE

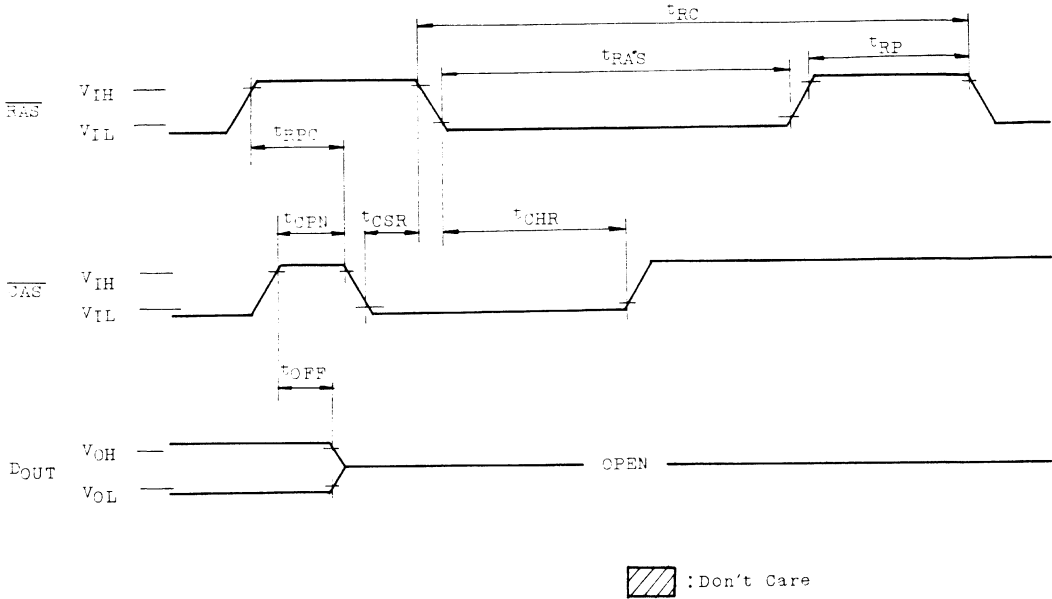


 : Don't Care

Note:  $\overline{\text{WRITE}}$ =Don't care,  $\text{A9}$ =Don't care

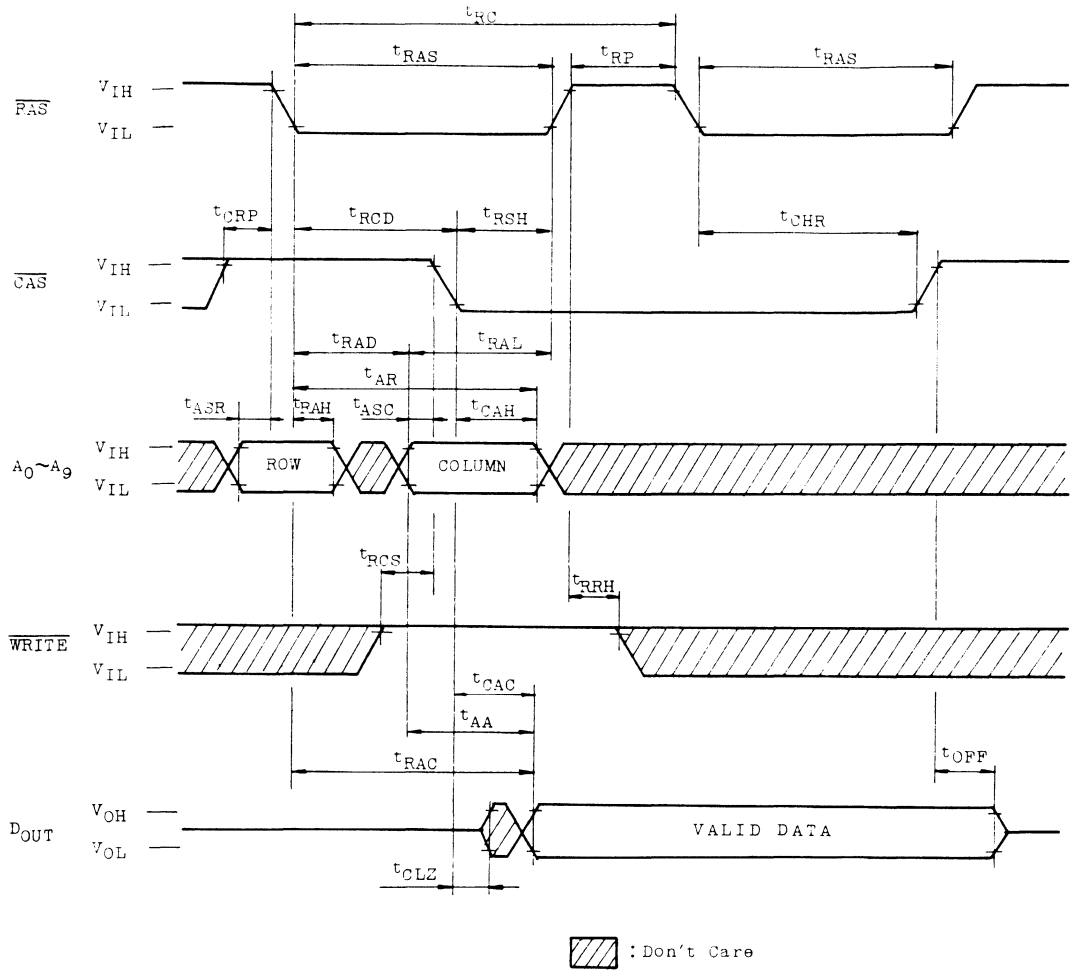
# THM81000S/L-10/12

## CAS BEFORE RAS REFRESH CYCLE



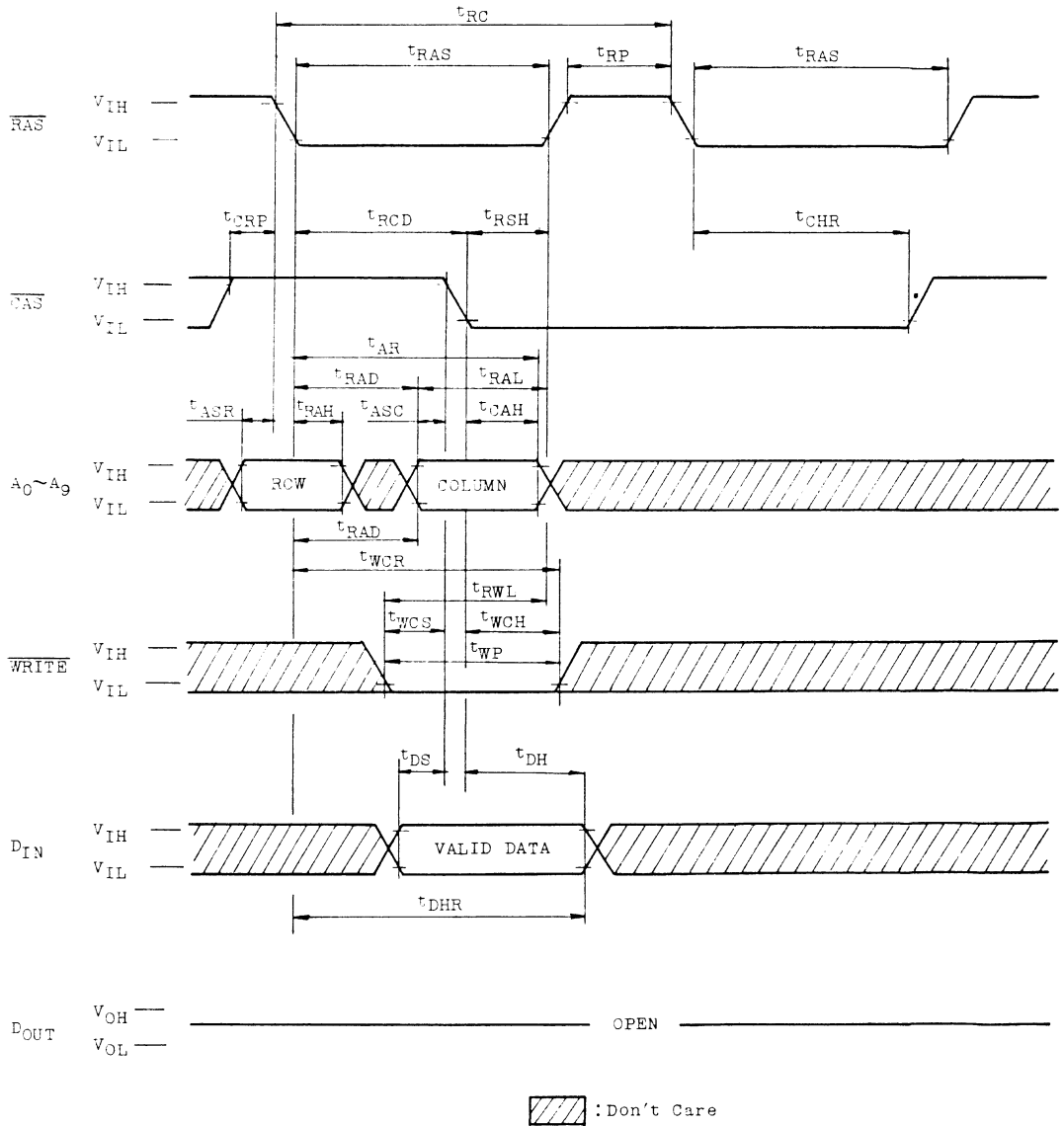
Note:  $\overline{\text{WRITE}}$ =Don't care, A0 ~ A9=Don't care

HIDDEN REFRESH CYCLE (READ)



# THM81000S/L-10/12

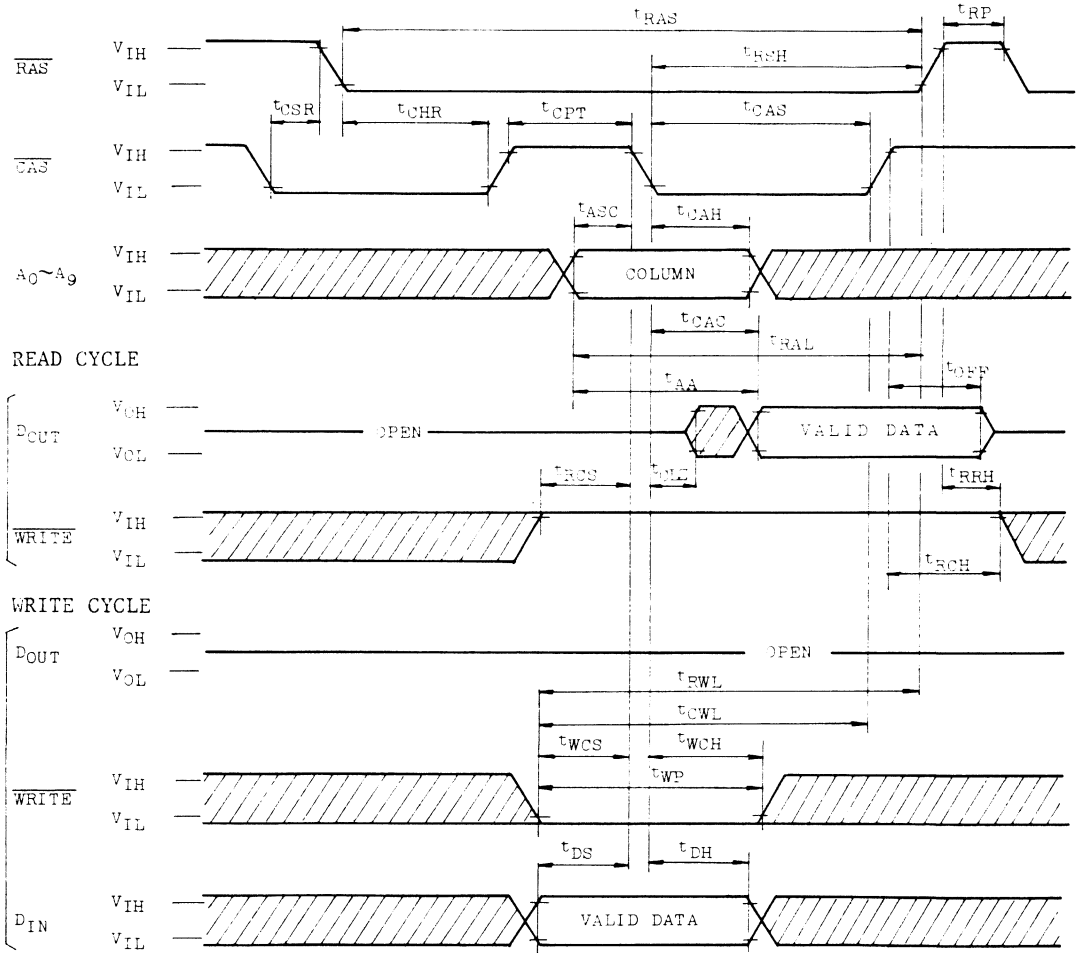
## HIDDEN REFRESH CYCLE (WRITE)





# THM81000S/L-10/12

## CAS BEFORE RAS REFRESH COUNTER TEST CYCLE

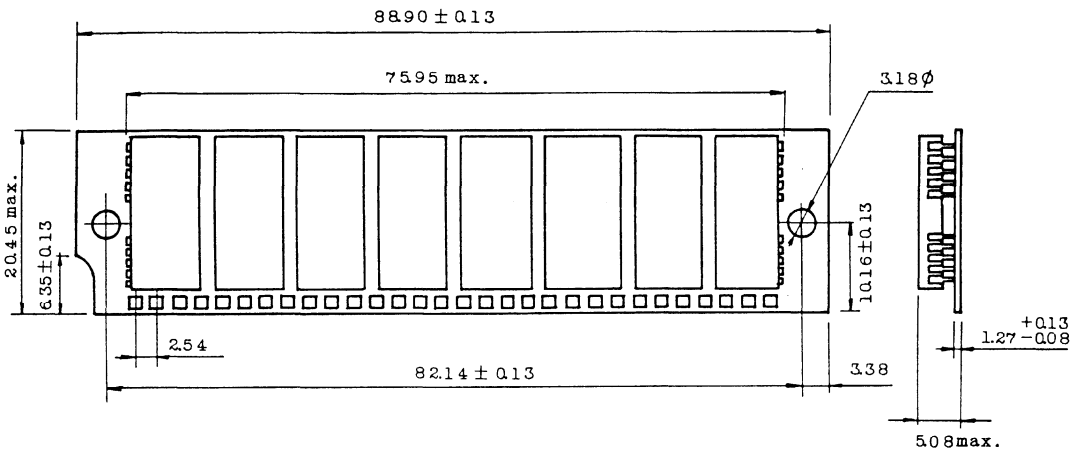


# THM81000S/L-10/12

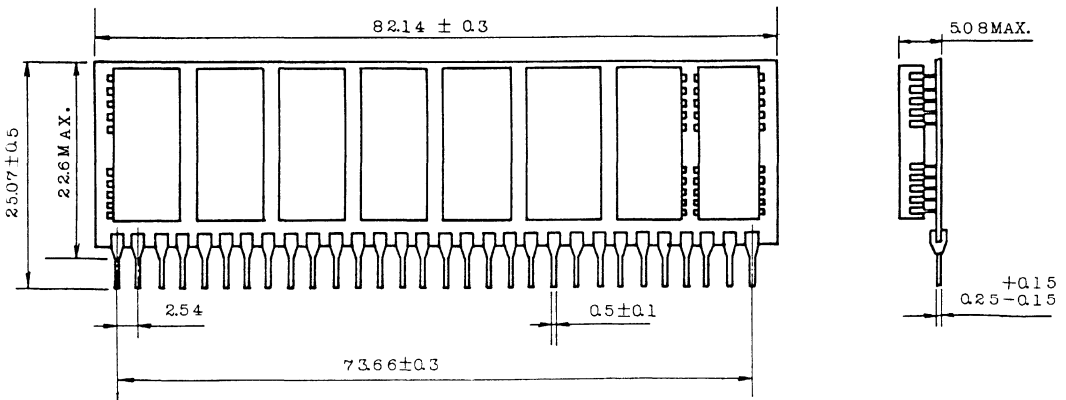
## OUTLINE DRAWINGS

• THM81000S

Unit in mm



• THM81000L



# TOSHIBA MOS MEMORY PRODUCT

1,048,576 WORDS × 9 BIT  
DYNAMIC RAM MODULE

THM91000S/L-10/12

## DESCRIPTION

The THM91000S/L is a 1,048,576 words by 9 bits dynamic RAM module which assembled 9 pcs of TC511000J on the printed circuit board.

The THM91000S/L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

## FEATURES

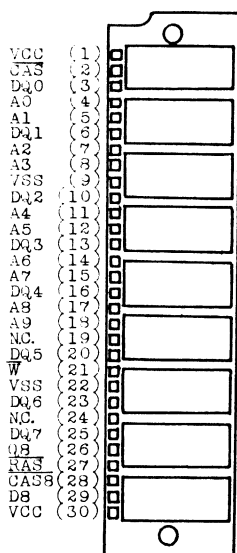
- 1,048,576 words by 9 bits organization
- Fast access time

	THM91000S/L-10	THM91000S/L-12
t <sub>RAC</sub> $\overline{\text{RAS}}$ Access Time	100ns	120ns
t <sub>AA</sub> Column Address Access Time	50ns	60ns
t <sub>CAC</sub> $\overline{\text{CAS}}$ Access Time	35ns	45ns
t <sub>RC</sub> Cycle Time	190ns	220ns
t <sub>PC</sub> Fast Page Mode Cycle Time	55ns	70ns

- Single power supply of 5V±10%
- Low power  
2,970 mW MAX. Operating (THM91000S/L-10)  
2,475 mW MAX. Operating (THM91000S/L-12)  
49.5 mW MAX. Standby
- $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh,  $\overline{\text{RAS}}$  only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms

## PIN CONNECTION

(TOP VIEW)

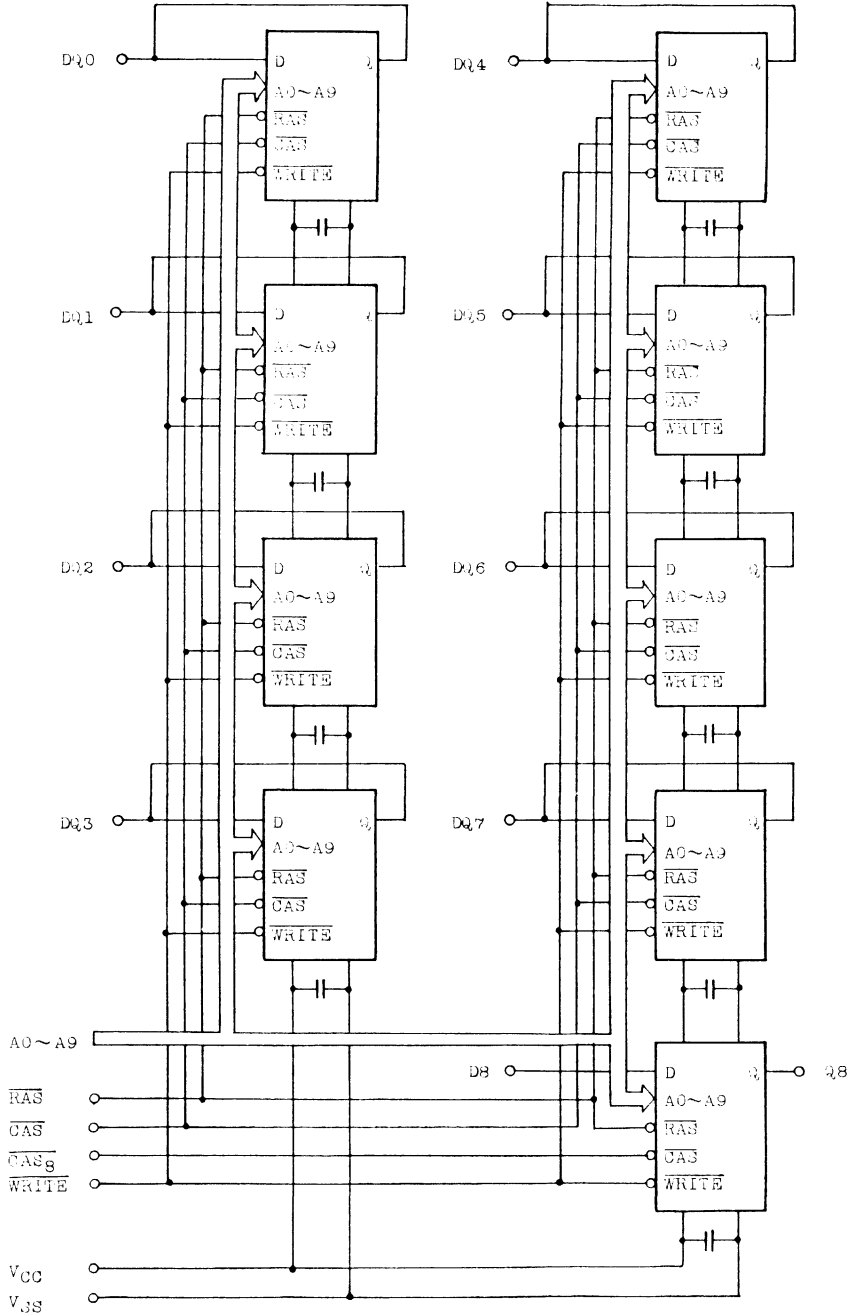


## PIN NAMES

A0 ~ 9	Address Inputs
DQ0 ~ 7	Data Input/Outputs
D8	Data Input
Q8	Data Output
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{CAS8}}$	Column Address Strobe
V <sub>CC</sub>	Power (+5V)
V <sub>SS</sub>	Ground
N.C.	No Connection

# THM91000S/L-10/12

## BLOCK DIAGRAM



# THM91000S/L-10/12

## ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V <sub>IN</sub>	-1 ~ 7	V	1
Output Voltage	V <sub>OUT</sub>	-1 ~ 7	V	1
Power Supply Voltage	V <sub>CC</sub>	-1 ~ 7	V	1
Operating Temperature	T <sub>OPR</sub>	0 ~ 70	°C	1
Storage Temperature	T <sub>STG</sub>	-55 ~ 125	°C	1
Soldering Temperature • Time	T <sub>SOLDER</sub>	260 • 10	°C • sec	1
Power Dissipation	P <sub>D</sub>	5.4	W	1
Short Circuit Output Current	I <sub>OUT</sub>	50	mA	1

## RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V	2
V <sub>IH</sub>	Input High Voltage	2.4		6.5	V	2
V <sub>IL</sub>	Input Low Voltage	-1.0		0.8	V	2

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10%, Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES	
I <sub>CC1</sub>	OPERATING CURRENT Average Power Supply Operating Current ( $\overline{RAS}$ , $\overline{CAS}$ , Address Cycling: $t_{RC}=t_{RC}$ MIN.)	THM91000S/L-10	-	540	mA	3, 4
		THM91000S/L-12	-	450		
I <sub>CC2</sub>	STANDBY CURRENT Power Supply Standby Current ( $\overline{RAS}=\overline{CAS}=V_{IH}$ )	-	18	mA		
I <sub>CC3</sub>	RAS ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ( $\overline{RAS}$ Cycling, $\overline{CAS}=V_{IH}$ : $t_{RC}=t_{RC}$ MIN.)	THM91000S/L-10	-	540	mA	3
		THM91000S/L-12	-	450		
I <sub>CC4</sub>	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ( $\overline{RAS}=V_{IL}$ , $\overline{CAS}$ Address Cycling: $t_{PC}=t_{PC}$ MIN.)	THM91000S/L-10	-	360	mA	3, 4
		THM91000S/L-12	-	270		
I <sub>CC5</sub>	STANDBY CURRENT Power Supply Standby Current ( $\overline{RAS}=\overline{CAS}=V_{CC}-0.2V$ )	-	9	mA		
I <sub>CC6</sub>	CAS BEFORE RAS REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ( $\overline{RAS}$ , $\overline{CAS}$ Cycling: $t_{RC}=t_{RC}$ MIN.)	THM91000S/L-10	-	540	mA	3
		THM91000S/L-12	-	450		
I <sub>I(L)</sub>	INPUT LEAKAGE CURRENT Input Leakage Current, any Input ( $0V \leq V_{IN} \leq 6.5V$ , All Other Pins not under Test=0V)	-90	90	µA		
I <sub>O(L)</sub>	OUTPUT LEAKAGE CURRENT (D <sub>OUT</sub> is disabled, $0V \leq V_{OUT} \leq 5.5V$ )	-20	20	µA		
V <sub>OH</sub>	OUTPUT LEVEL Output "H" Level Voltage (I <sub>OUT</sub> =-5mA)	2.4	-	V		
V <sub>OL</sub>	OUTPUT LEVEL Output "L" Level Voltage (I <sub>OUT</sub> =4.2mA)	-	0.4	V		

# THM91000S/L-10/12

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

( $V_{CC}=5V\pm 10\%$ ,  $T_a=0\sim 70^{\circ}C$ ) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM91000S/L-10		THM91000S/L-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
$t_{RC}$	Random Read or Write Cycle Time	190		220		ns	
$t_{PC}$	Fast Page Mode Cycle Time	55		70		ns	
$t_{RAC}$	Access Time from $\overline{RAS}$		100		120	ns	8, 13
$t_{CAC}$	Access Time from $\overline{CAS}$		35		45	ns	8, 13
$t_{AA}$	Access Time from Column Address		50		60	ns	8, 14
$t_{CPA}$	Access Time from $\overline{CAS}$ Precharge		50		65	ns	8
$t_{CLZ}$	$\overline{CAS}$ to Output in Low-Z	5		5		ns	8
$t_{OFF}$	Output Buffer Turn-off Delay	0	30	0	35	ns	9
$t_T$	Transition Time (Rise and Fall)	3	50	3	50	ns	7
$t_{RP}$	$\overline{RAS}$ Precharge Time	80		90		ns	
$t_{RAS}$	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000	ns	
$t_{RASp}$	$\overline{RAS}$ Pulse Width (Fast Page Mode)	100	100,000	120	100,000	ns	
$t_{RSH}$	$\overline{RAS}$ Hold Time	35		45		ns	
$t_{CSH}$	$\overline{CAS}$ Hold Time	100		120		ns	
$t_{CAS}$	$\overline{CAS}$ Pulse Width	35		45		ns	
$t_{RCD}$	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	65	25	75	ns	13
$t_{RAD}$	$\overline{RAS}$ to Column Address Delay Time	20	50	20	60	ns	14
$t_{CRP}$	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10		ns	
$t_{CP}$	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		15		ns	
$t_{ASR}$	Row Address Set-Up Time	0		0		ns	
$t_{RAH}$	Row Address Hold Time	15		15		ns	
$t_{ASC}$	Column Address Set-Up Time	0		0		ns	
$t_{CAH}$	Column Address Hold Time	20		25		ns	
$t_{AR}$	Column Address Hold Time referenced to $\overline{RAS}$	75		90		ns	
$t_{RAL}$	Column Address to $\overline{RAS}$ Lead Time	50		60		ns	
$t_{RCS}$	Read Command Set-Up Time	0		0		ns	
$t_{RCH}$	Read Command Hold Time	0		0		ns	10
$t_{RRH}$	Read Command Hold Time referenced to $\overline{RAS}$	0		0		ns	10

# THM91000S/L-10/12

## ELECTRICAL CHARACTERISTIC AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM91000S/L-10		THM91000S/L-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
$t_{WCH}$	Write Command Hold Time	20		25		ns	
$t_{WCR}$	Write Command Hold Time referenced to $\overline{RAS}$	75		90		ns	
$t_{WP}$	Write Command Pulse Width	20		25		ns	
$t_{RWL}$	Write Command to $\overline{RAS}$ Lead Time	25		30		ns	
$t_{CWL}$	Write Command to $\overline{CAS}$ Lead Time	25		30		ns	
$t_{DS}$	Data Set-Up Time	0		0		ns	11
$t_{DH}$	Data Hold Time	20		25		ns	11
$t_{DHR}$	Data Hold Time referenced to $\overline{RAS}$	75		90		ns	
$t_{REF}$	Refresh Period		3		8	ms	
$t_{WCS}$	Write Command Set-Up Time	0		0		ns	12
$t_{CSR}$	$\overline{CAS}$ Set-Up Time ( $\overline{CAS}$ before $\overline{RAS}$ Cycle)	10		10		ns	
$t_{CHR}$	$\overline{CAS}$ Hold Time ( $\overline{CAS}$ before $\overline{RAS}$ Cycle)	30		30		ns	
$t_{RPC}$	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		ns	
$t_{CPT}$	$\overline{CAS}$ Precharge Time ( $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50		60		ns	
$t_{CPV}$	$\overline{CAS}$ Precharge Time	15		20		ns	

## CAPACITANCE ( $V_{CC}=5V\pm 10\%$ , $f=1MHz$ , $T_a=0\sim 70^\circ C$ )

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$C_{I1}$	Input Capacitance ( $A0\sim A9$ , $\overline{U}$ , $\overline{CAS}$ , $\overline{RAS}$ )		60	pF
$C_{I2}$	Input Capacitance (D8, $\overline{CAS8}$ )		7	pF
$C_{DQ}$	I/O Capacitance (DQ0 $\sim$ DQ7)		15	pF
$C_Q$	Output Capacitance (Q8)		10	pF

## THM91000S/L-10/12

### NOTES:

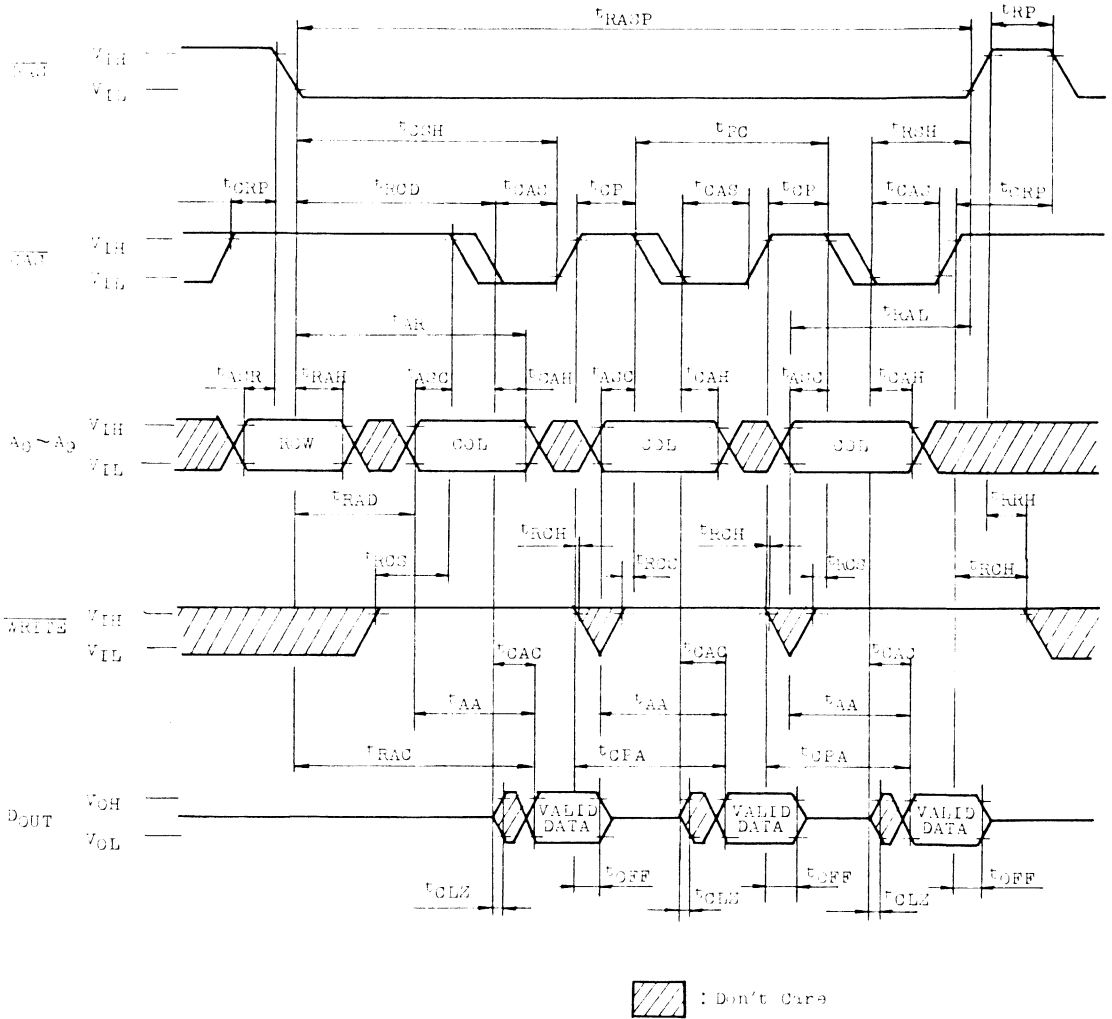
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to VSS.
3.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ ,  $I_{CC6}$  depend on cycle rate.
4.  $I_{CC1}$ ,  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200ns is required after power-up followed by 8  $\overline{RAS}$  cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{CAS}$  before  $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
6. AC measurements assume  $t_f=5ns$ .
7.  $V_{IH}(min.)$  and  $V_{IL}(max.)$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9.  $t_{OFF}(max.)$  defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
11. These parameters are referenced to  $\overline{CAS}$  leading edge in early write cycles and to  $\overline{WRITE}$  leading edge in read-write cycles.
12.  $t_{WCS}$  is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If  $t_{WCS} \neq t_{WCS}(min.)$ , the cycle is an early write cycle and data out pin will remain open circuit (high impedance).
13. Operation within the  $t_{RCD}(max.)$  limit insures that  $t_{RAC}(max.)$  can be met.  $t_{RCD}(max.)$  is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD}(max.)$  limit, then access time is controlled by  $t_{CAC}$ .
14. Operation within the  $t_{RAD}(max.)$  limit insures that  $t_{RAC}(max.)$  can be met.  $t_{RAD}(max.)$  is specified as a reference point only: If  $t_{RAD}$  is greater than the specified  $t_{RAD}(max.)$  limit, then access time is controlled by  $t_{AA}$ .





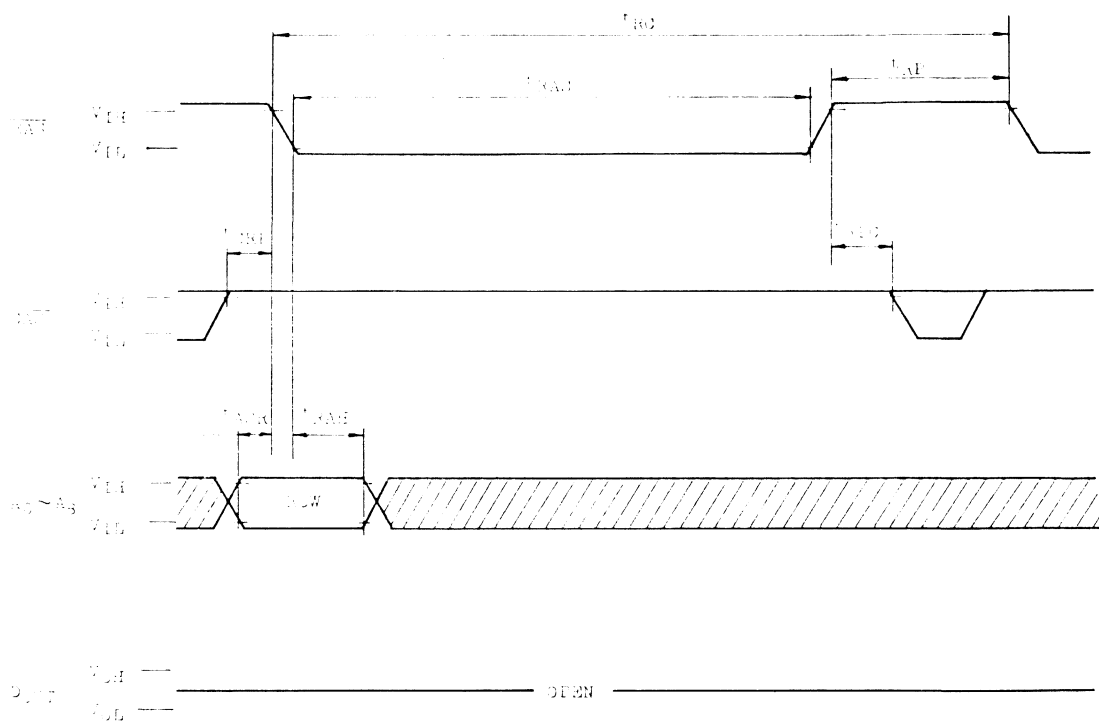



FAST PAGE MODE READ CYCLE





RAS ONLY REFRESH CYCLE

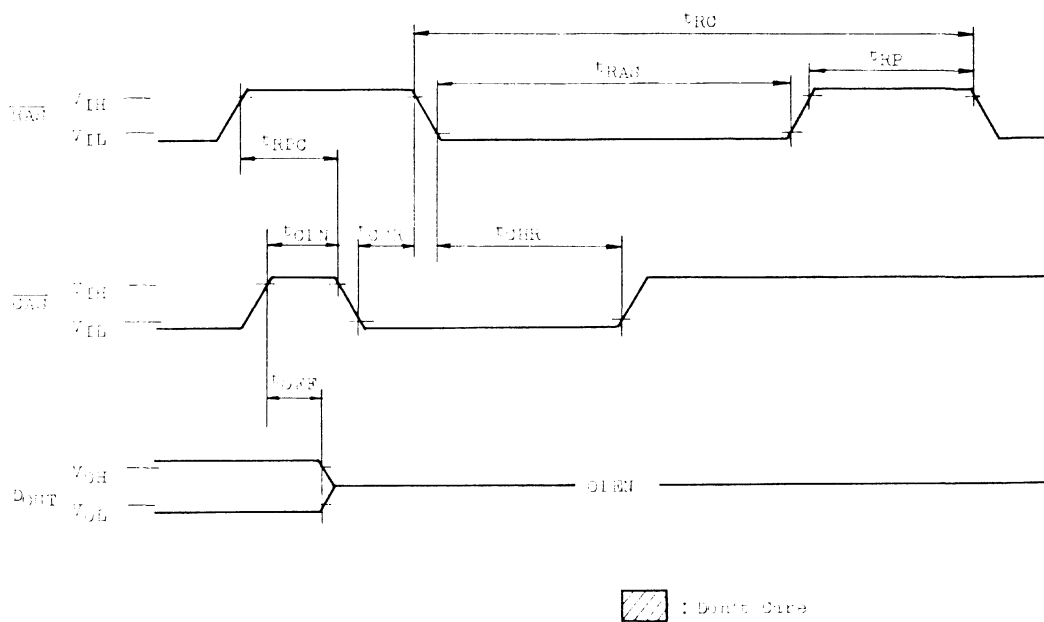


 : Don't Care

Note: WRITE=Don't care, A9=Don't care

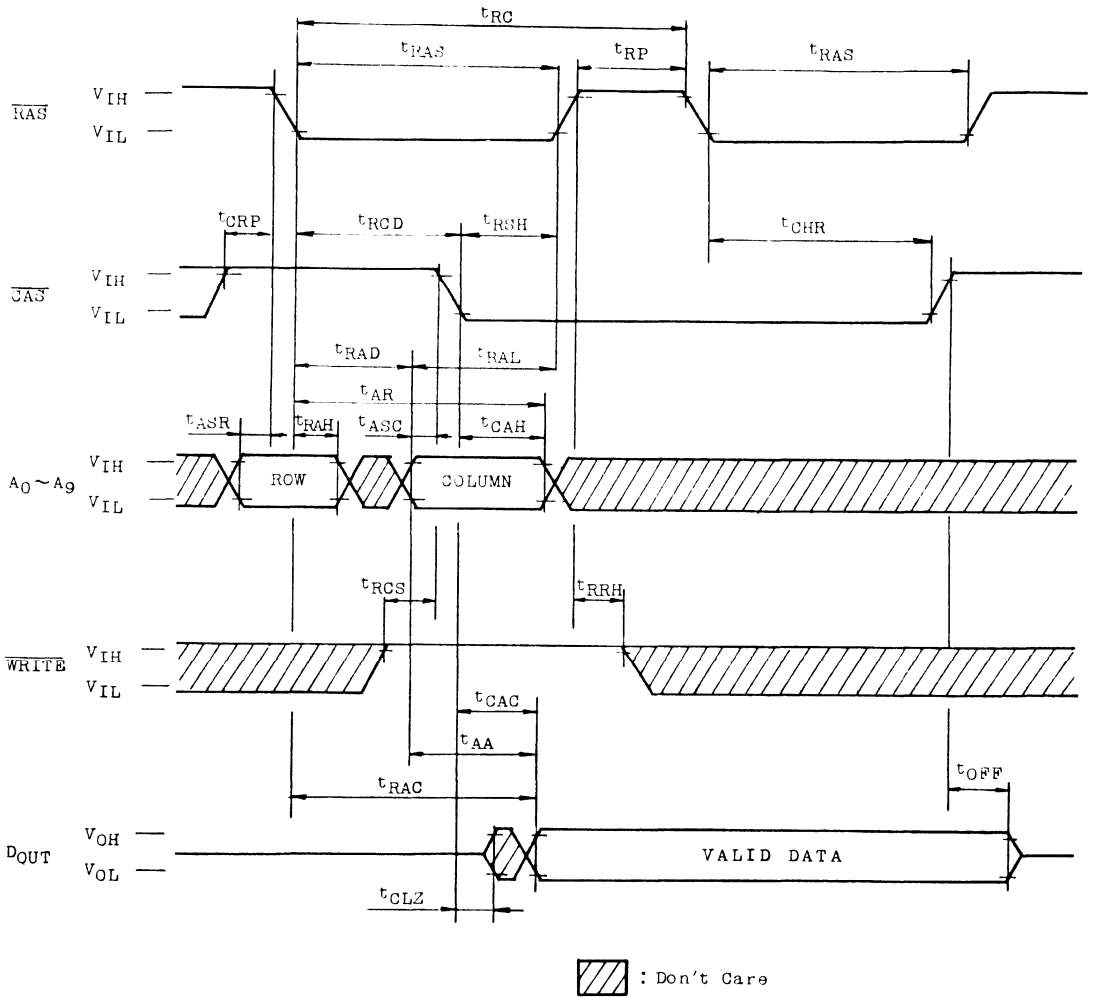
# THM91000S/L-10/12

## CAS BEFORE RAS REFRESH CYCLE



Note: WRITE=Don't care, A0~A9=Don't care

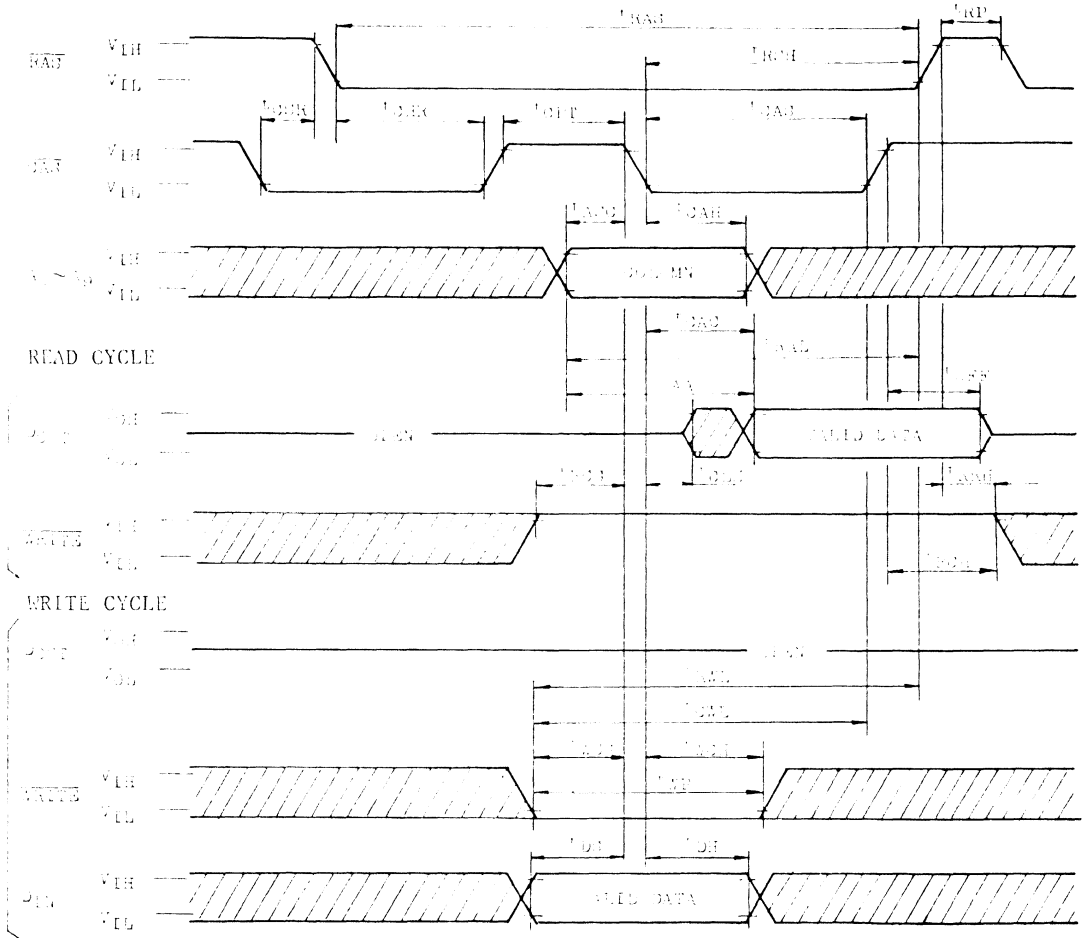
HIDDEN REFRESH CYCLE (READ)







CAS BEFORE RAS REFRESH COUNTER TEST CYCLE

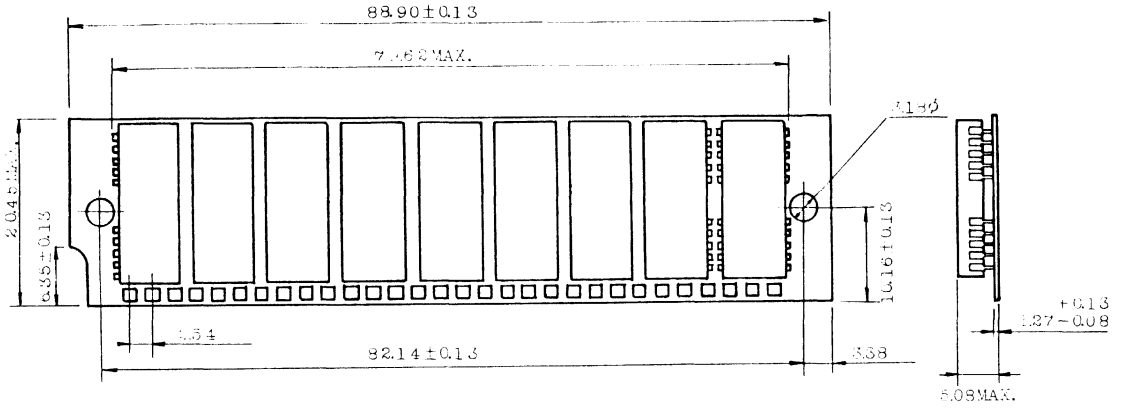


# THM91000S/L-10/12

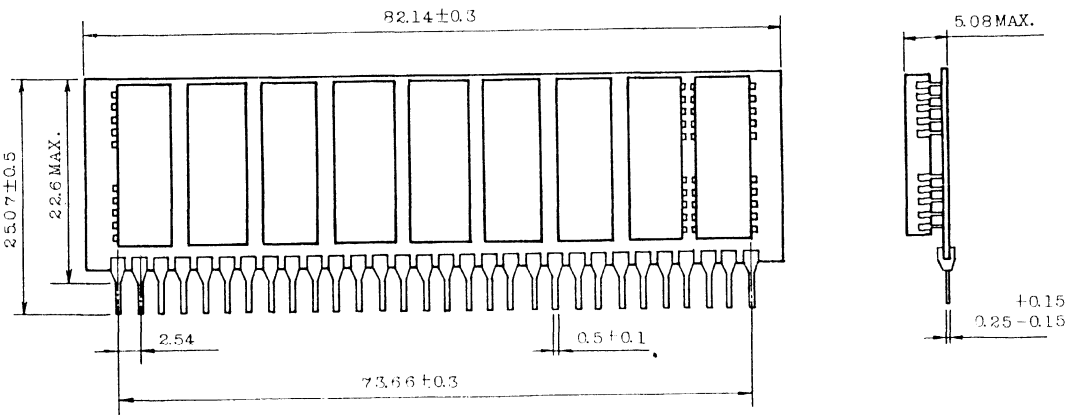
## OUTLINE DRAWINGS

• THM91000S

Unit in mm



• THM91000L







# TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD × 8 BIT STATIC RAM TMM2015BP-90, TMM2015BP-12  
 SILICON MONOLITHIC  
 N-CHANNEL SILICON GATE MOS PROCESS TMM2015BP-10, TMM2015BP-15

## DESCRIPTION

The TMM2015BP is a 16, 384 bits high speed and low power static random access memory organized as 2, 048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 90ns/100ns/120ns/150ns and maximum operating current of 50mA. When  $\overline{CS}$  is a logical high, the device

is placed in a low power standby mode in which maximum standby current is 5mA. Thus the TMM2015BP is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2015BP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability

## FEATURES

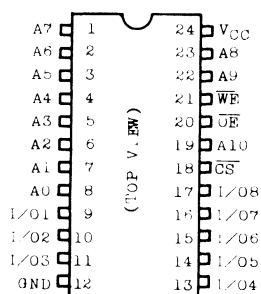
### ● Access Time and Current

Part Number	Parameter	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2015BP-90		90ns	50mA	5mA
TMM2015BP-10		100ns	50mA	5mA
TMM2015BP-12		120ns	50mA	5mA
TMM2015BP-15		150ns	50mA	5mA

- High Density Assembly Capability  
0.3 inch width package (24pin plastic DIP)

- Single 5V power Supply
- Fully Static Operation
- Power Down Feature:  $\overline{CS}$
- Output Buffer Control:  $\overline{OE}$
- Three State Outputs
- All Inputs and Outputs: Directly TTL Compatible
- Inputs Protected: All inputs have protection against static charge.

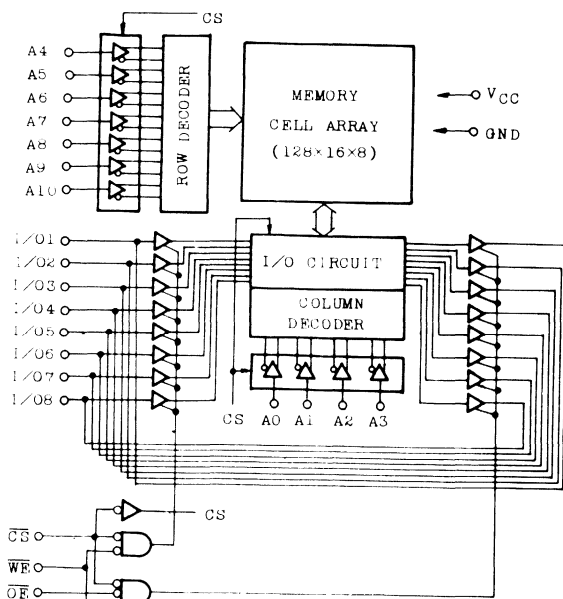
## PIN CONNENCTION



## PIN NAMES

A <sub>0</sub> ~A <sub>3</sub>	Column Address Inputs
A <sub>4</sub> ~A <sub>10</sub>	Row Address Inputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
I/O <sub>1</sub> ~I/O <sub>8</sub>	Data Input/Output
$\overline{OE}$	Output Enable Input
V <sub>CC</sub>	Power (5V)
GND	Ground

## BLOCK DIAGRAM



# TMM2015BP-90, TMM2015BP-12 TMM2015BP-10, TMM2015BP-15

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	Power Supply Voltage	-0.5~7.0	V
V <sub>IN</sub> , V <sub>OUT</sub>	Input/Output Voltage	-0.5*~7.0	V
T <sub>OPR</sub>	Operating Temperature	0~70	°C
T <sub>STG</sub>	Storage Temperature	-55~150	°C
T <sub>SOLDER</sub>	Soldering Temperature · Time	260 · 10	°C·sec
P <sub>D</sub>	Power Dissipation (Ta = 70°C)	0.7	W

\* -3.0V at Pulse width 50ns

## D. C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.0	—	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input Low Voltage	-0.5**	—	0.8	V
V <sub>CC</sub>	Power Supply Voltage	4.5	5.0	5.5	V

\*\* -3.0V at Pulse width 50ns

## D. C. CHARACTERISTICS (Ta=0~70°C, V<sub>CC</sub>=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> =0V~5.5V	-10	—	10	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OUT</sub> =-1.0mA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OUT</sub> =4.0mA	—	—	0.4	V
I <sub>LO</sub>	Output Leakage Current	$\overline{CS}=V_{IH}$ or $\overline{WE}=V_{IL}$ or $\overline{OE}=V_{IH}$ , V <sub>OUT</sub> =0V~5.5V	-10	—	10	μA
I <sub>SBP</sub>	Peak Power-on Current	$\overline{CS}=V_{CC}$ , I <sub>OUT</sub> =0mA	—	—	10	mA
I <sub>SB</sub>	Standby Current	$\overline{CS}=V_{IH}$ , I <sub>OUT</sub> =0mA	—	—	5	mA
I <sub>CC</sub>	Operating Current	$\overline{CS}=V_{IL}$ , I <sub>OUT</sub> =0mA	—	—	50	mA

## CAPACITANCE\*\*\* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =0V	5	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> =0V	10	pF

\*\*\* Note : This parameter is periodically sampled and is not 100% tested.

# TMM2015AP-90, TMM2015AP-12 TMM2015AP-10, TMM2015AP-15

## A. C. CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%)

### Read Cycle

SYMBOL	PARAMETER	TMM2015BP-90		TMM2015BP-10		TMM2015BP-12		TMM2015BP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	90	—	100	—	120	—	150	—	ns
t <sub>ACC</sub>	Address Access Time	—	90	—	100	—	120	—	150	
t <sub>CO</sub>	Chip Select Access Time	—	90	—	100	—	120	—	150	
t <sub>OE</sub>	Output Enable Time	—	35	—	35	—	50	—	55	
t <sub>OH</sub>	Output Data Hold Time from Address Change	10	—	10	—	10	—	10	—	
t <sub>CLZ</sub>	$\overline{CS}$ to Output in Low-Z	15	—	15	—	15	—	15	—	
t <sub>CHZ</sub>	$\overline{CS}$ to Output in High-Z	—	40	—	40	—	40	—	55	
t <sub>OLZ</sub>	$\overline{OE}$ to Output in Low-Z	5	—	5	—	5	—	5	—	
t <sub>OHZ</sub>	$\overline{OE}$ to Output in High-Z	—	35	—	35	—	35	—	50	
t <sub>PU</sub>	Chip Selection to power Up Time	0	—	0	—	0	—	0	—	
t <sub>PD</sub>	Chip Deselection to Power Down Time	—	50	—	50	—	60	—	60	

### Write Cycle

SYMBOL	PARAMETER	TMM2015BP-90		TMM2015BP-10		TMM2015BP-12		TMM2015BP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	90	—	100	—	120	—	150	—	ns
t <sub>CW</sub>	Chip Selection to End of Write	60	—	70	—	85	—	100	—	
t <sub>AS</sub>	Address Set Up Time	20	—	20	—	20	—	20	—	
t <sub>WP</sub>	Write Pulse Width	55	—	65	—	80	—	100	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	0	—	
t <sub>DS</sub>	Data Set Up Time	30	—	35	—	45	—	50	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	0	—	
t <sub>WLZ</sub>	$\overline{WE}$ to Output in Low-Z	5	—	5	—	5	—	5	—	
t <sub>WHZ</sub>	$\overline{WE}$ to Output in High-Z	—	25	—	30	—	35	—	50	

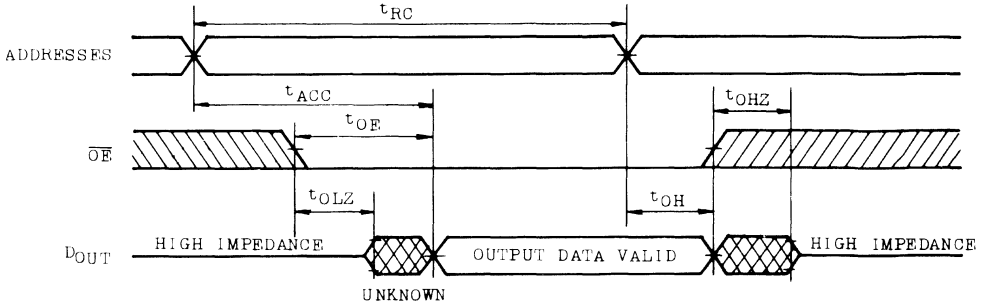
## A. C. TEST CONDITIONS

Input Pulse Levels	0~3.5V
Input Rise and Fall Time	10ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL Gate & C <sub>L</sub> =100pF

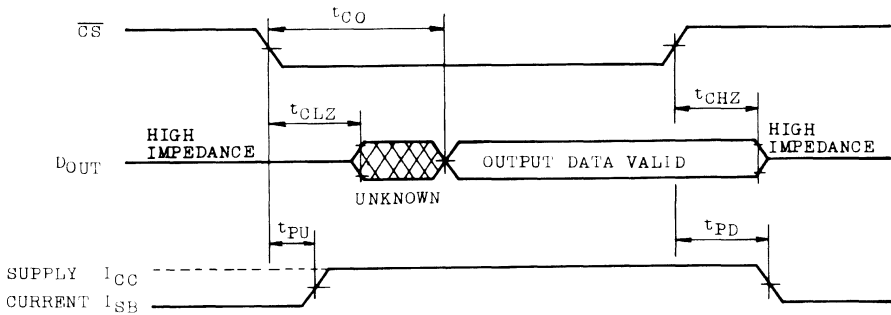
# TMM2015BP-90, TMM2015BP-12 TMM2015BP-10, TMM2015BP-15

## TIMING WAVEFORMS

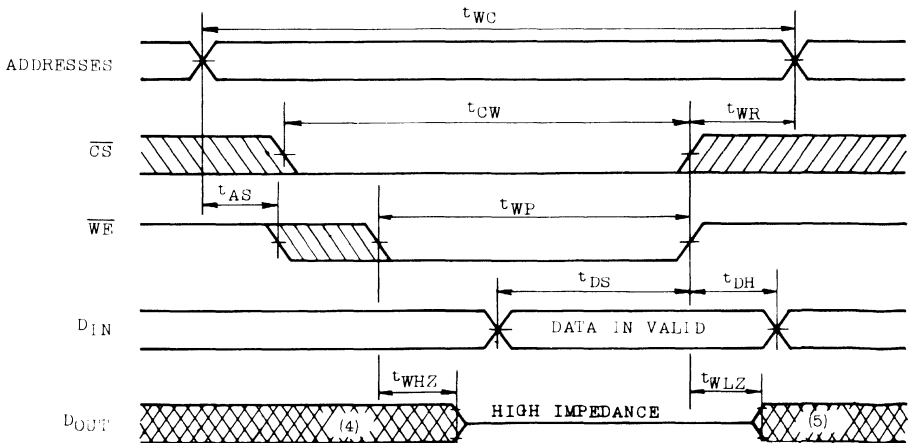
- (A) READ CYCLE (1) (1)



- (B) READ CYCLE (2) (1), (2)



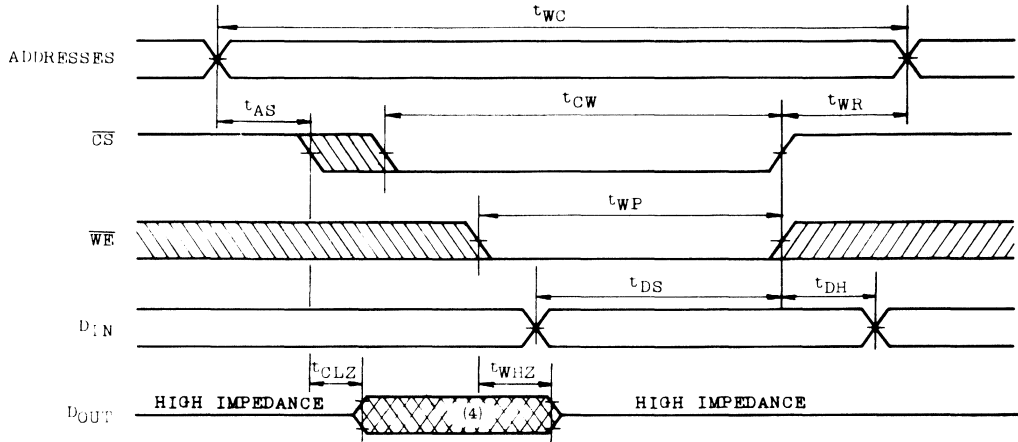
- (C) WRITE CYCLE (1) (3)





# TMM2015BP-90, TMM2015BP-12 TMM2015BP-10, TMM2015BP-15

● (D) WRITE CYCLE (2) (3)



NOTES:

- (1) The  $\overline{WE}$  is high for read cycle.  
Device is continuously selected,  $\overline{CS} = V_{IL}$  in read cycle (1)
- (2) All addresses are valid prior to or simultaneously with  $\overline{CS}$  transitions.
- (3) A write occurs during the overlap of low  $\overline{CS}$  and low  $\overline{WE}$ .  
The  $t_{WC}$  is specified as the time from the chip selection to end of write in write cycle, and the  $t_{WP}$  is specified as the overlap time of low  $\overline{CS}$  and low  $\overline{WE}$ .  
 $\overline{OE}$  is allowed to be low or high level in write cycle.  
If the  $\overline{OE}$  is high, the output buffers remain in a high impedance state in this period.
- (4) If the  $\overline{CS}$  low transition occurs simultaneously with or latter to the  $\overline{WE}$  low transition, the output buffers remain in a high impedance state in this period.
- (5) If the  $\overline{CS}$  high transition occurs simultaneously with  $\overline{WE}$  high transition, the output buffers remain in a high impedance state in this period.

These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A) t<sub>CLZ</sub>, t<sub>OLZ</sub>, t<sub>WLZ</sub> ..... Output Enable Time

(B) t<sub>CHZ</sub>, t<sub>OHZ</sub>, t<sub>WHZ</sub> ..... Output Disable Time

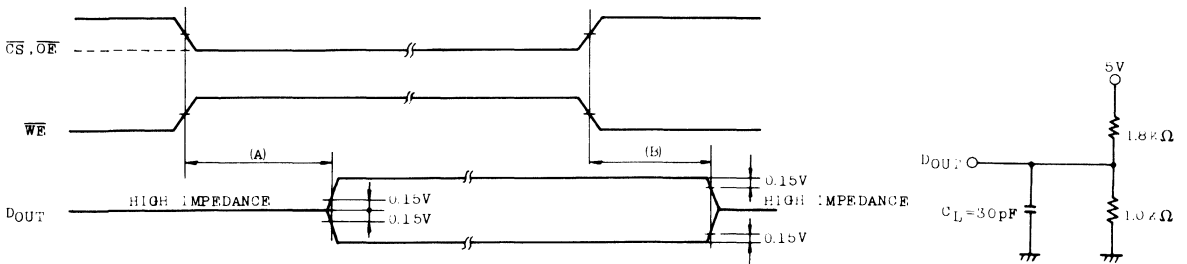
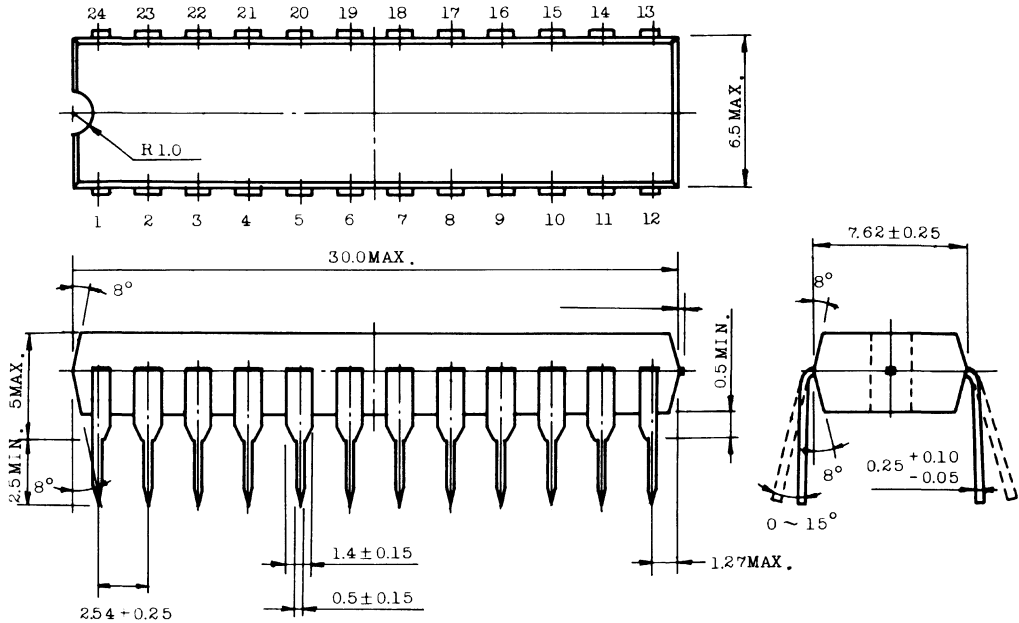


Fig. 1 Output load condition for enable disable time measurement.

# TMM2015BP-90, TMM2015BP-12 TMM2015BP-10, TMM2015BP-15

## OUTLINE DRAWINGS

Unit: mm



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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# TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD × 8 BIT STATIC RAM **TMM2016BP-90, TMM2016BP-12**  
 SILICON MONOLITHIC  
 N-CHANNEL SILICON GATE MOS PROCESS **TMM2016BP-10, TMM2016BP-15**

## DESCRIPTION

The TMM2016BP is a 16,384 bits high speed and low power static random access memory organized as 2,048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 90ns/100ns/120ns/150ns and maximum operating current of 50mA. When  $\overline{CS}$  is logical high, the device is

placed in a low power standby mode in which maximum standby current is 5mA. Thus the TMM2016BP is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2016BP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability

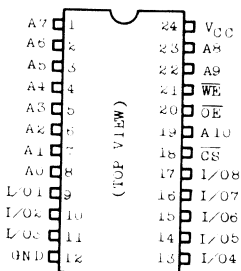
## FEATURES

### ● Access Time and Current

Part Number	Parameter	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2016BP-90		90ns	50mA	5mA
TMM2016BP-10		100ns	50mA	5mA
TMM2016BP-12		120ns	50mA	5mA
TMM2016BP-15		150ns	50mA	5mA

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature  $\overline{CS}$
- Output Buffer Control  $\overline{OE}$
- Three State Outputs
- All Inputs and Outputs: Directly TTL Compatible
- Inputs Protected: All inputs have protection against static charge

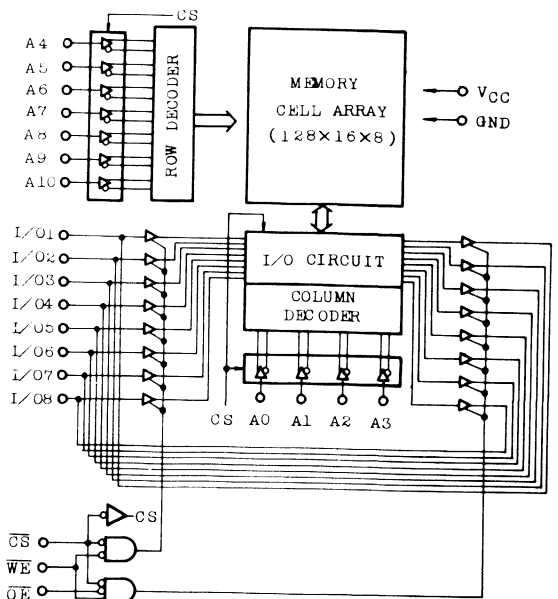
## PIN CONNECTION



## PIN NAMES

A <sub>0</sub> ~A <sub>3</sub>	Column Address Inputs
A <sub>4</sub> ~A <sub>10</sub>	Row Address Inputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
I/O <sub>1</sub> ~I/O <sub>8</sub>	Data Input/Output
$\overline{OE}$	Output Enable Input
V <sub>CC</sub>	Power (5V)
GND	Ground

## BLOCK DIAGRAM



# TMM2016BP-90, TMM2016BP-12 TMM2016BP-10, TMM2016BP-15

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	Power Supply Voltage	-0.5~7.0	V
V <sub>IN</sub> , V <sub>OUT</sub>	Input/Output Voltage	-0.5~7.0	V
T <sub>OPR</sub>	Operating Temperature	0~70	°C
T <sub>STG</sub>	Storage Temperature	-55~150	°C
T <sub>SOLDER</sub>	Soldering Temperature · Time	260 · 10	°C·sec
P <sub>D</sub>	Power Dissipation(Ta = 70°C)	1.0	W

\* -3.0V at Pulse width 50ns

## D. C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.0	—	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input Low Voltage	-0.5**	—	0.8	V
V <sub>CC</sub>	Power Supply Voltage	4.5	5.0	5.5	V

\*\* -3.0V at Pulse width 50ns

## D. C. CHARACTERISTICS (Ta=0~70°C, V<sub>CC</sub>=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX.	UNIT
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> =0V~5.5V	-10	—	10	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OUT</sub> =-1.0mA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OUT</sub> =4.0mA	—	—	0.4	V
I <sub>LO</sub>	Output Leakage Current	$\overline{CS}=V_{IH}$ or $\overline{WE}=V_{IL}$ or $\overline{OE}=V_{IH}$ , V <sub>OUT</sub> =0V~5.5V	-10	—	10	μA
I <sub>SBP</sub>	Peak Power-on Current	$\overline{CS}=V_{CC}$ I <sub>OUT</sub> =0mA	—	—	10	mA
I <sub>SB</sub>	Standby Current	$\overline{CS}=V_{IH}$ I <sub>OUT</sub> =0mA	—	—	5	mA
I <sub>CC</sub>	Operating Current	$\overline{CS}=V_{IL}$ I <sub>OUT</sub> =0mA	—	—	50	mA

## CAPACITANCE \*\*\* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =0V	5	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> =0V	10	pF

\*\*\* Note : This parameter is periodically sampled and is not 100% tested

# TMM2016BP-90, TMM2016BP-12 TMM2016BP-10, TMM2016BP-15

## A. C. CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%)

### Read Cycle

SYMBOL	PARAMETER	TMM2016BP-90		TMM2016BP-10		TMM2016BP-12		TMM2016BP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	90	—	100	—	120	—	150	—	ns
t <sub>ACC</sub>	Address Access Time	—	90	—	100	—	120	—	150	
t <sub>CO</sub>	Chip Select Access Time	—	90	—	100	—	120	—	150	
t <sub>OE</sub>	Output Enable Time	—	35	—	35	—	50	—	55	
t <sub>OH</sub>	Output Data Hold Time from Address Change	10	—	10	—	10	—	10	—	
t <sub>CLZ</sub>	$\overline{\text{CS}}$ to Output in Low-Z	15	—	15	—	15	—	15	—	
t <sub>CHZ</sub>	$\overline{\text{CS}}$ to Output in High-Z	—	40	—	40	—	40	—	55	
t <sub>OLZ</sub>	$\overline{\text{OE}}$ to Output in Low-Z	5	—	5	—	5	—	5	—	
t <sub>OHZ</sub>	$\overline{\text{OE}}$ to Output in High-Z	—	35	—	35	—	35	—	50	
t <sub>PU</sub>	Chip Selection to power Up Time	0	—	0	—	0	—	0	—	
t <sub>PD</sub>	Chip Deselection to Power Down Time	—	50	—	50	—	60	—	60	

### Write Cycle

SYMBOL	PARAMETER	TMM2016BP-90		TMM2016BP-10		TMM2016BP-12		TMM2016BP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	90	—	100	—	120	—	150	—	ns
t <sub>CW</sub>	Chip Selection to End of Write	60	—	70	—	85	—	100	—	
t <sub>AS</sub>	Address Set Up Time	20	—	20	—	20	—	20	—	
t <sub>WP</sub>	Write Pulse Width	55	—	65	—	80	—	100	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	0	—	
t <sub>DS</sub>	Data Set Up Time	30	—	35	—	45	—	50	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	0	—	
t <sub>WLZ</sub>	$\overline{\text{WE}}$ to Output in Low-Z	5	—	5	—	5	—	5	—	
t <sub>WHZ</sub>	$\overline{\text{WE}}$ to Output in High-Z	—	25	—	30	—	35	—	50	

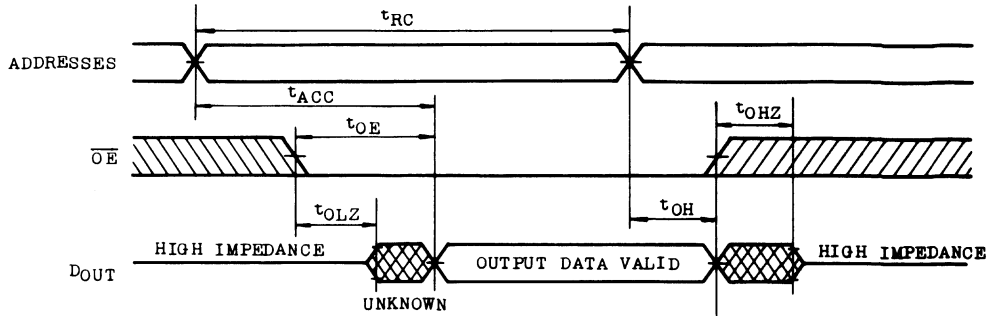
## A. C. TEST CONDITIONS

Input Pulse Levels	0~3.5V
Input Rise and Fall Time	10ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL Gate & C <sub>L</sub> =100pF

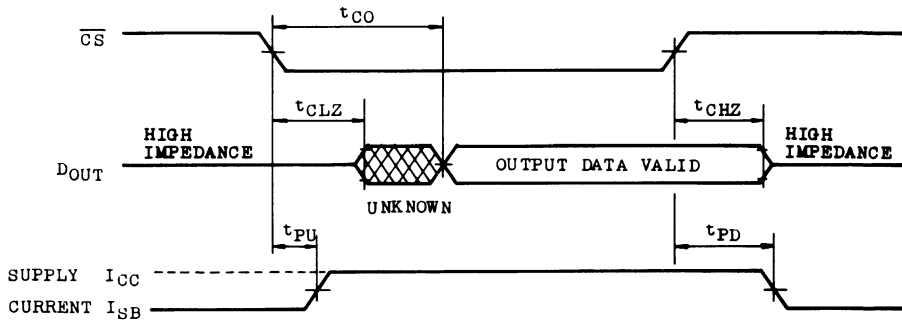
# TMM2016BP-90, TMM2016BP-12 TMM2016BP-10, TMM2016BP-15

## TIMING WAVEFORMS

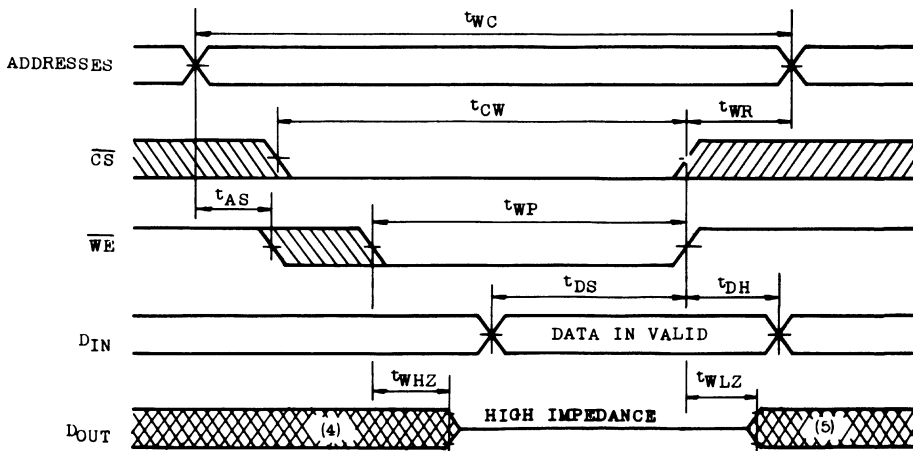
### ● (A) READ CYCLE (1) (1)



### ● (B) READ CYCLE (2) (1), (2)

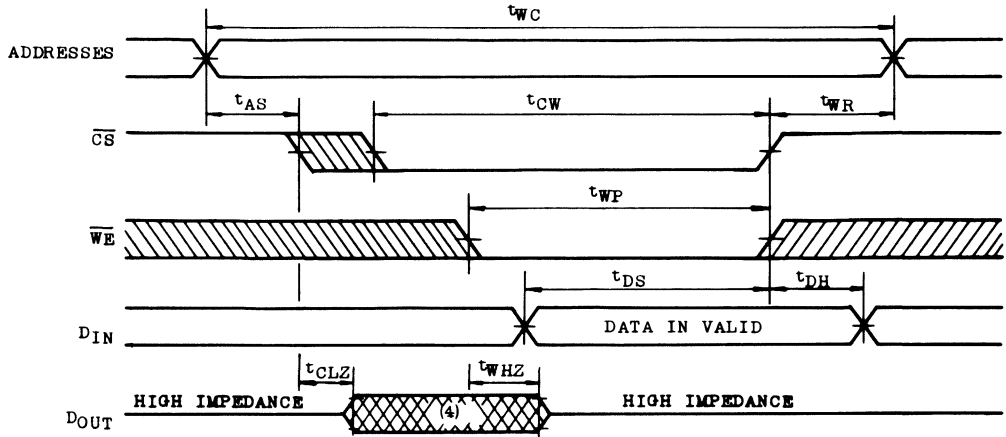


### ● (C) WRITE CYCLE (1) (3)



# TMM2016BP-90, TMM2016BP-12 TMM2016BP-10, TMM2016BP-15

## ● (D) WRITE CYCLE (2) (3)



### NOTES:

- (1) The  $\overline{WE}$  is high for read cycle.  
Device is continuously selected,  $\overline{CS}=V_{IL}$  in read cycle (1)
- (2) All addresses are valid prior to or simultaneously with  $\overline{CS}$  transitions.
- (3) A write occurs during the overlap of low  $\overline{CS}$  and low  $\overline{WE}$ .  
The  $t_{cw}$  is specified as the time from the chip selection to end of write in write cycle, and the  $t_{wp}$  is specified as the overlap time of low  $\overline{CS}$  and low  $\overline{WE}$ .  
 $\overline{OE}$  is allowed to be low or high level in write cycle.  
If the  $\overline{OE}$  is high, the output buffers remain in a high impedance state in this period.
- (4) If the  $\overline{CS}$  low transition occurs simultaneously with or later to the  $\overline{WE}$  low transition, the output buffers remain in a high impedance state in this period.
- (5) If the  $\overline{CS}$  high transition occurs simultaneously with  $\overline{WE}$  high transition, the output buffers remain in a high impedance state in this period.

These parameters are specified as follows and measured by using the load shown in Fig. 1

(A)  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{WLZ}$  ..... Output Enable Time

(B)  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$  ..... Output Disable Time

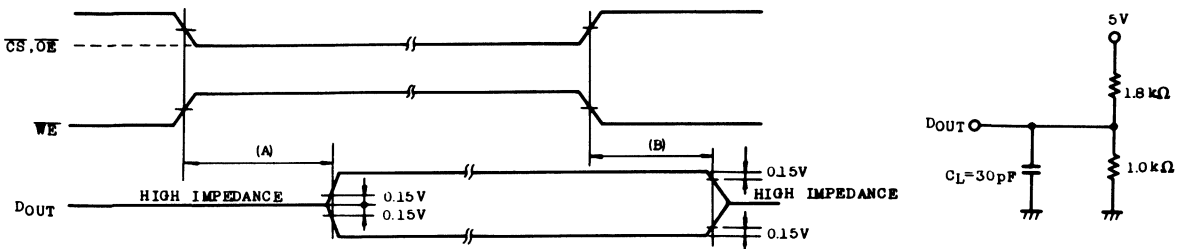
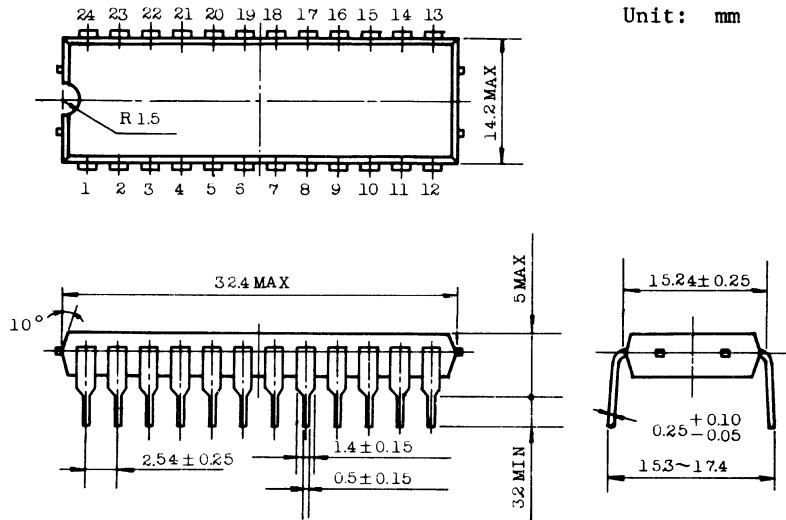


Fig. 1 Output load condition for enable disable time measurement.

# TMM2016BP-90, TMM2016BP-12 TMM2016BP-10. TMM2016BP-15

## OUTLINE DRAWINGS



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described. no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.  
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# TOSHIBA MOS MEMORY PRODUCT

2,048 WORD × 8 BIT CMOS STATIC RAM

TC5517CP-15/CPL-15/CP-20/CPL-20  
TC5517CF-15/CFL-15/CF-20/CFL-20

## DESCRIPTION

The TC5517CP/CF is a 16384-bit high speed and low power fully static random access memory organized as 2048 words by 8 bits using CMOS technology, and operates from a single 5 volt supply. The TC5517CP/CF has a output enable inputs,  $\overline{OE}$  for fast memory access and output control and chip enable enable input  $\overline{CE}$ , which is used for device selection and can be used in order to achieve minimum standby current mode easily for battery back up. Also the high speed and low power characteristics which maximum access time is 150ns, 200ns and maximum operating current is 5mA/MHz are

achieved. Thus the TC5517CP/CF is most suitable for use in low power applications where battery operation or battery back up for nonvolatility are required. Furthermore the TC5517CPL/CFL guaranteed a standby current equal to or less than 1μA at 60°C ambient temperature available. And the TC5517CP/CPL is pin compatible with 2716 type EPROM. This means that the TC5517CP/CPL and EPROM can be interchanged in the same socket, and the flexibility in the definition of the quantity of RAM versus EPROM allows the wide application in microcomputer system.

## FEATURES

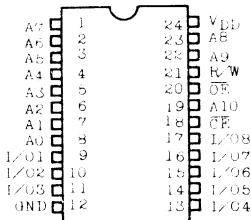
- Low Power Dissipation  
5mA/MHz (Max.)  
0.2μA(MAX.) at Ta=25°C  
1.0μA(MAX.) at Ta=60°C
  - 5V Single Power Supply
  - Low Voltage Operation : VDD=3V  
tCO=1μs(MAX.) Ta=60°C
  - Wide Temperature Operation  
Ta=-40~85°C
  - Fully Static Operation
  - Data Retention Voltage : 2.0V~5.5V
  - Output Buffer Control :  $\overline{OE}$
- Operating  
Standby  
Standby

- Access Time

	TC5517CP-15 CPL-15	TC5517CP-20 CPL-20
	TC5517CF-15 CFL-15	TC5517CF-20 CFL-20
Address Access Time (MAX.)	150ns	200ns
$\overline{CE}$ Access Time (MAX.)	150ns	200ns
$\overline{OE}$ Access Time (MAX.)	70ns	100ns

- Directly TTL Compatible : All Inputs and Outputs
- 24 Pin Standard Plastic Package : TC5517CP
- 24 Pin Flat Package : TC5517CF

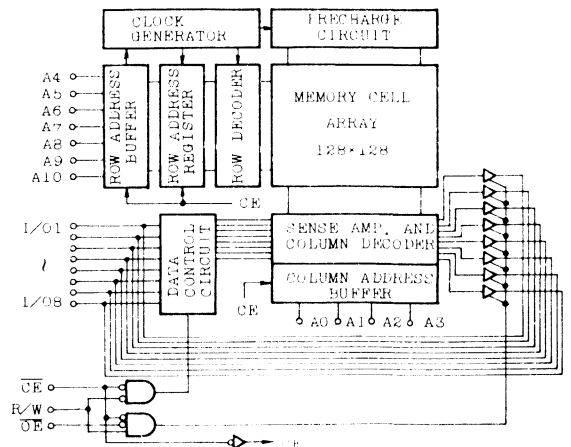
## PIN CONNECTION (TOP VIEW)



## PIN NAMES

A <sub>0</sub> ~A <sub>10</sub>	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O <sub>1</sub> ~I/O <sub>8</sub>	Data Input/Output
VDD	Power (+5V)
GND	Ground

## BLOCK DIAGRAM



# TC5517CP-15/CPL-15/CP-20/CPL-20

# TC5517CF-15/CFL-15/CF-20/CFL-20

## OPERATION MODE

MODE	$\overline{CE}$	$\overline{OE}$	R/W	$A_0 \sim A_{10}$	I/O <sub>1</sub> ~ I/O <sub>8</sub>	POWER
Read	L	L	H	Stable	Data Out	I <sub>DD0</sub>
Write	L	*	L	Stable	Data In	I <sub>DD0</sub>
Output Deselect	L	H	H	*	High Impedance	I <sub>DD0</sub>
** Standby	H	*	*	*	High Impedance	I <sub>DD5</sub>

Note : \* : H or L    \*\* : DataRetention Mode

## ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V <sub>DD</sub>	Power Supply Voltage	-0.3 ~ 7.0V
V <sub>IN</sub>	Input Voltage	-0.3V ~ V <sub>DD</sub> + 0.3V
V <sub>I/O</sub>	Input/Output Voltage	-0.3V ~ V <sub>DD</sub> + 0.3V
P <sub>D</sub>	Power Dissipation(Ta = 85°C)	0.8W(0.45W)*
T <sub>STG</sub>	Storage Temperature	-55°C ~ 150°C
T <sub>OPR</sub>	Operating Temperature	-40°C ~ 85°C
T <sub>SOLDER</sub>	Soldering Temperature·Time	260°C·10sec.

\*Plastic FP=0.45W

## RECOMMENDED D. C. OPERATING CONDITIONS (Ta = -40 ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	—	0.8	V
V <sub>DH</sub>	Data Retention Voltage	2.0	—	5.5	V

## D. C. CHARACTERISTICS

(Ta = -40 ~ 85°C, V<sub>DD</sub> = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	TC5517CP-15		TC5517CP-20		UNIT		
			CF-15	CF-20	MIN.	MAX.			
I <sub>IL</sub>	Input Leakage Current	0 ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	—	±1.0	—	±1.0	μA		
I <sub>I/O</sub>	I/O Leakage Current	$\overline{CE} = V_{IH}, 0V \leq V_{I/O} \leq V_{DD}$	—	±5.0	—	±5.0	μA		
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4V	-1.0	—	-1.0	—	mA		
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4V	2.0	—	2.0	—	mA		
I <sub>DD51</sub>	Standby Current	$\overline{CE} = 2.2V$	—	3.0	—	3.0	mA		
I <sub>DD52</sub>		$\overline{CE} \leq V_{DD} - 0.5V$	TC5517CPL/ CFL	Ta = 25°C	—	0.2	—	0.2	μA
				Ta = 60°C	—	1.0	—	1.0	
			TC5517CP/ CF	Ta = 25°C	—	1.0	—	1.0	
				Ta = 60°C	—	5.0	—	5.0	
I <sub>DD01</sub>	Operating Current	t <sub>cycle</sub> = Min. cycle, $\overline{CE} = 0V, I_{OUT} = 0mA$	V <sub>IN</sub> = V <sub>IH</sub> /V <sub>IL</sub>	—	45	—	30	mA	
			V <sub>IN</sub> = V <sub>DD</sub> /GND	—	40	—	25		
		t <sub>cycle</sub> = 1μs, $\overline{CE} = 0V, I_{OUT} = 0mA$	V <sub>IN</sub> = V <sub>IH</sub> /V <sub>IL</sub>	—	10	—	10		
			V <sub>IN</sub> = V <sub>DD</sub> /GND	—	5	—	5		

Note : Typical values are at Ta = 25°C, V<sub>DD</sub> = 5V.

# TC5517CP-15/CPL-15/CP-20/CPL-20 TC5517CF-15/CFL-15/CF-20/CFL-20

## CAPACITANCE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	—	5	10	pF
C <sub>I/O</sub>	Input/Output Capacitance	—	5	10	pF

Note : This parameter is periodically sampled and is not 100% tested.

## A. C. CHARACTERISTICS (T<sub>a</sub> = -40~85°C, V<sub>DD</sub> = 5V ± 10%)

### Read Cycle

SYMBOL	PARAMETER	TC5517CP-15/CPL-15 TC5517CF-15/CFL-15		TC5517CP-20/CPL-20 TC5517CF-20/CFL-20		UNITS
		MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	150	—	200	—	ns
t <sub>ACC</sub>	Address Time	—	150	—	200	
t <sub>OE</sub>	OE to Output Valid	—	70	—	100	
t <sub>CO</sub>	CE to Output Valid	—	150	—	200	
t <sub>LOF</sub>	CE or OE to Output Active	10	—	10	—	
t <sub>OD</sub>	Output High-Z from Deselection	—	50	—	60	
t <sub>OH</sub>	Output Hold from Address Change	15	—	20	—	

### Write Cycle

SYMBOL	PARAMETER	TC5517CP-15/CPL-15 TC5517CF-15/CFL-15		TC5517CP-20/CPL-20 TC5517CF-20/CFL-20		UNITS
		MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	100	—	200	—	ns
t <sub>WP</sub>	Write Pulse Width	120	—	150	—	
t <sub>AW</sub>	Address Set up Time	0	—	0	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	
t <sub>ODW</sub>	Output High-Z from R/W	—	50	—	60	
t <sub>ORW</sub>	Output Active from R/W	10	—	10	—	
t <sub>DS</sub>	Data Set up Time	60	—	80	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	

## A. C. TEST CONDITIONS

Output Load : 100pF + 1TTL Gate

Timing Measurement Reference Levels

Input Pulse Levels: 0.6V, 2.4V

Input : 0.8V and 2.2V

Output : 0.8V and 2.2V

Input Pulse Rise and Fall Times : 10ns

## 3V OPERATE SPECIFICATION

### D. C. RECOMMENDED OPERATING CONDITIONS (T<sub>a</sub> = -10~60°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	2.7	3.0	3.3	V
V <sub>IH</sub>	Input High Voltage	V <sub>DD</sub> - 0.2	—	V <sub>DD</sub>	V
V <sub>IL</sub>	Input Low Voltage	0	—	0.2	V

# TC5517CP-15/CPL-15/CP-20/CPL-20

# TC5517CF-15/CFL-15/CF-20/CFL-20

## D. C. CHARACTERISTICS

(Ta = -10 ~ 60 C)

SYMBOL	PARAMETER CONDIOIONS	MIN.	TYP.	MAX.	UNIT		
I <sub>IL</sub>	Input Leakage Current	0V ≦ V <sub>IN</sub> ≦ V <sub>DD</sub>	—	—	+1.0	μA	
I <sub>IO</sub>	Output Leakage Current	CE = V <sub>OH</sub> , 0V ≦ V <sub>I/O</sub> ≦ V <sub>DD</sub>	—	—	+5.0	μA	
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = V <sub>DD</sub> - 0.2V	100	—	—	μA	
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.2V	100	—	—	μA	
I <sub>DS</sub>	Standby Current	CE = V <sub>OH</sub>	TC5517CPL	Ta = 25 C	—	0.2	μA
			CFL	Ta = 60 C	—	1.0	
			TC5517CP	Ta = 25 C	—	1.0	
			CF	Ta = 60 C	—	5.0	
I <sub>DDO</sub>	Operating Current	CE = 0V, I <sub>OH</sub> = 0mA t <sub>r</sub> , t <sub>f</sub> ≦ 20nsec	t <sub>rise</sub> = 1μsec	—	2.0	3.0	mA
			t <sub>fall</sub> = 10μsec	—	0.3	0.5	

● All voltage is measured from GND.

## A. C. CHARACTERISTICS

(Ta = -10 ~ 60 C, V<sub>DD</sub> = 3V ± 10%)

### Read CYCLE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t <sub>RC</sub>	Read Cycle Time	1000	—	—	ns
t <sub>ACC</sub>	Address Access Time	—	250	1000	ns
t <sub>OE</sub>	OE to Output Valid	—	80	200	ns
t <sub>CO</sub>	CE to Output Valid	—	250	1000	ns
t <sub>COE</sub>	CE or OE Output Active	10	—	—	ns
t <sub>OD</sub>	Output High-Z Deselection	—	—	200	ns
t <sub>OH</sub>	Output Hold from Address Change	20	—	—	ns

### WRITE CYCLE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t <sub>WC</sub>	Write Cycle Time	1000	—	—	ns
t <sub>WP</sub>	Write Pulse Width	500	—	—	ns
t <sub>AW</sub>	Address Set up Time	100	—	—	ns
t <sub>WR</sub>	Write Recovery Time	100	—	—	ns
t <sub>ODW</sub>	Output High-Z from R/W	—	—	200	ns
t <sub>OEW</sub>	Output Active from R/W	10	—	—	ns
t <sub>DS</sub>	Data Set up Time	400	—	—	ns
t <sub>DH</sub>	Data Hold Time	50	—	—	ns

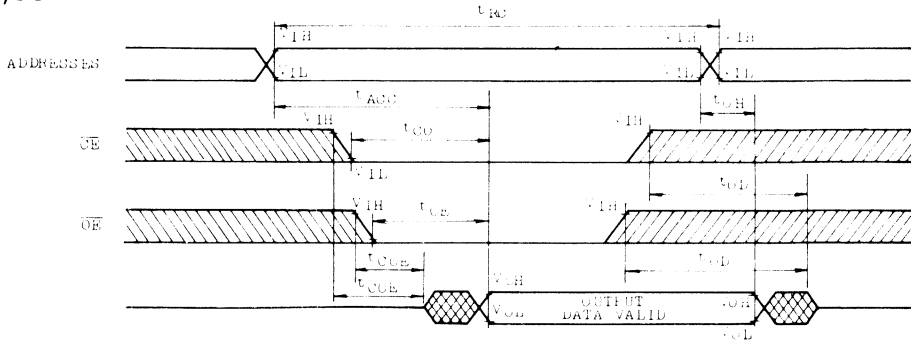
## A. C. TEST CONDITIONS

- Output Load : 100pF (Include Jig)
- Input Pulse Levels : 0.2V, V<sub>DD</sub> - 0.2V
- Timing Measurement Level : Input : 1.5V, 1.5V
- : Output : 1.5V, 1.5V
- Input Pulse Rise and Fall Times : ≦ 20ns

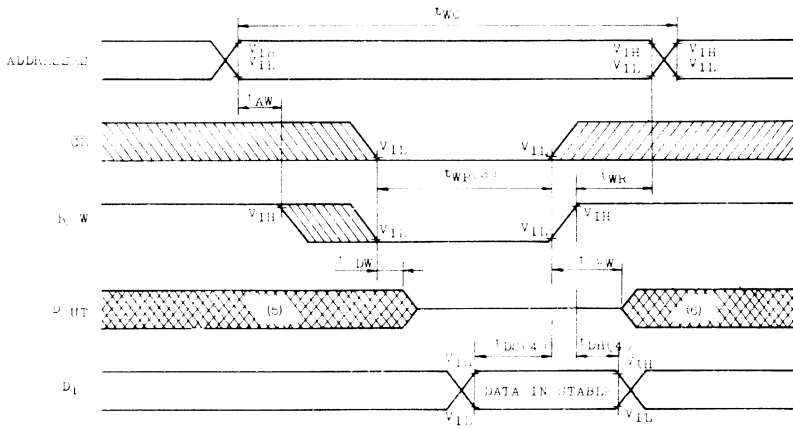
# TC5517CP-15/CPL-15/CP-20/CPL-20 TC5517CF-15/CFL-15/CF-20/CFL-20

## TIMING WAVEFORMS

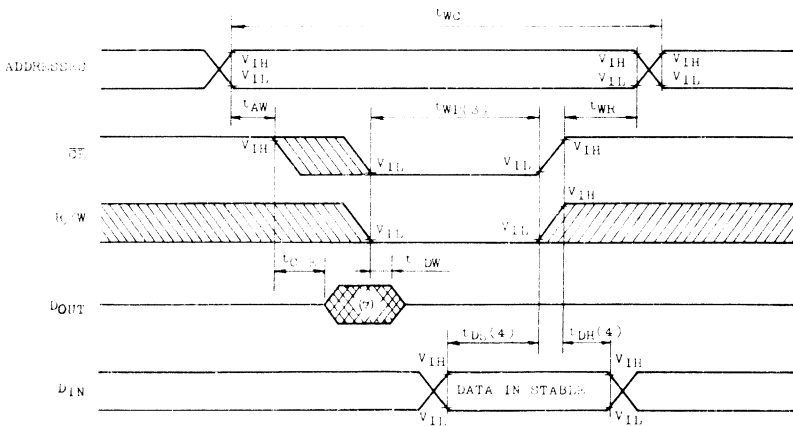
### ● Read Cycle




### ● Write Cycle 1 (2)



### ● Write Cycle 2 (2)



 : UNKNOWN

# TC5517CP-15/CPL-15/CP-20/CPL-20

# TC5517CF-15/CFL-15/CF-20/CFL-20

Note:

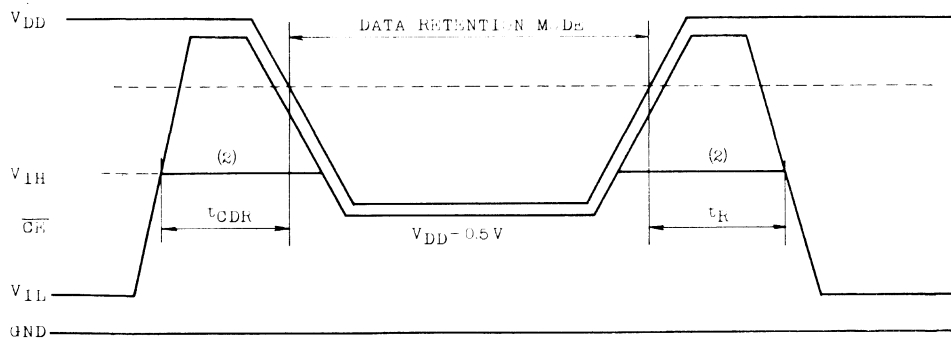
1. R/W is high for a Read Cycle.
2.  $\overline{OE} = V_{IH}$  or  $V_{IL}$ . If,  $\overline{OE} = V_{IH}$  during write cycle, the output buffers remain in a high impedance state.
3.  $t_{WP}$  is specified as the logical "AND" of  $\overline{CE}$  and R/W.
4.  $t_{DPH}$ ,  $t_{DS}$  are measured from the latter of  $\overline{CE}$  or R/W going low to the earlier of  $\overline{CE}$  or R/W going high.
5. If the  $\overline{CE}$  low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
6. If the  $\overline{CE}$  high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the R/W is low or the R/W low transition occurs prior to or simultaneously with the  $\overline{CE}$  low transition, the output buffers remain in high impedance state in this period.

## DATA RETENTION CHARACTERISTICS (Ta = -40~85 C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT	
$V_{DH}$	Data Retention Power Supply Voltage		2.0	—	5.5	V	
$I_{DDS2}$	Standby Current	TC5517CPL/CFL	Ta = 25°C	—	0.005	0.2	$\mu A$
			Ta = 60°C	—	—	1.0	
		TC5517CP/CF	Ta = 25°C	—	0.05	1.0	
			Ta = 60°C	—	—	5.0	
$t_{CDR}$	From Chip Deselection to Data Retention Mode		0	—	—	ns	
$t_R$	Recovery Time		$t_{RC}(1)$	—	—		

Note :

1.  $t_{RC}$  : Read Cycle Time



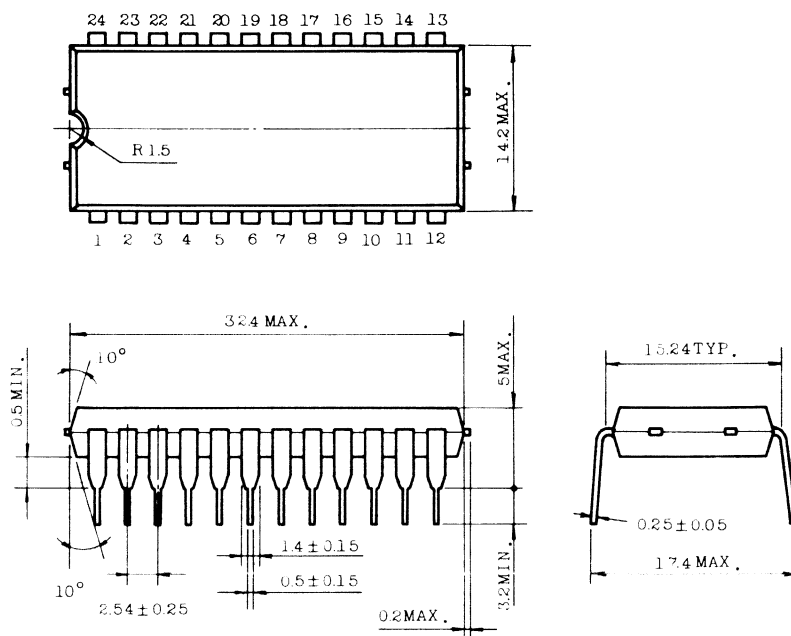
Note :

2. If the  $V_{IH}$  level of  $\overline{CE}$  is 2.2V, during the period that the  $V_{DD}$  voltage is going down from 4.5V to 2.7V  $I_{DDS1}$  current flows.

# TC5517CP-15/CPL-15/CP-20/CPL-20 TC5517CF-15/CFL-15/CF-20/CFL-20

## OUTLINE DRAWINGS

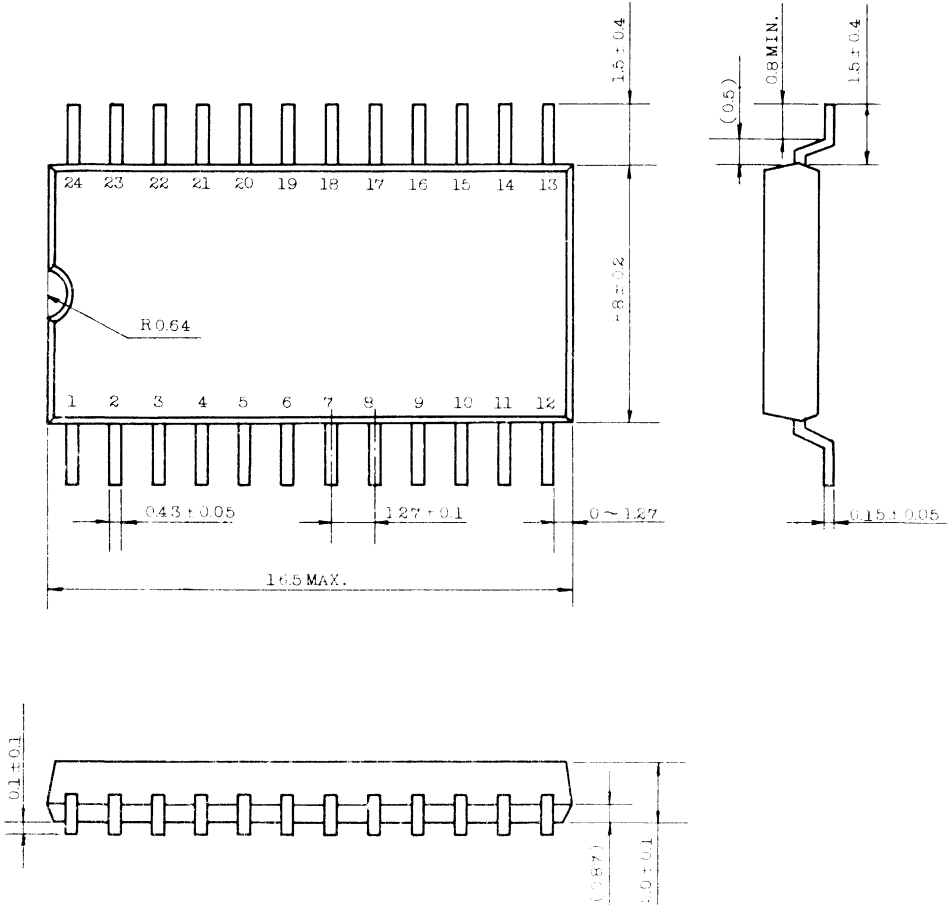
- Plastic DIP



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.24 leads.  
All dimensions are in millimeters.

**TC5517CP-15/CPL-15/CP-20/CPL-20**  
**TC5517CF-15/CFL-15/CF-20/CFL-20**

- Plastic FP



Note : Each lead pitch is 1.27mm.  
 All leads are located within 0.1mm of their true longitudinal position with respect to No.1 and No.24 leads.



# TC5517CP-15/CPL-15/CP-20/CPL-20 TC5517CF-15/CFL-15/CF-20/CFL-20

## PACKAGE INFORMATION FOR FLAT PACKAGE

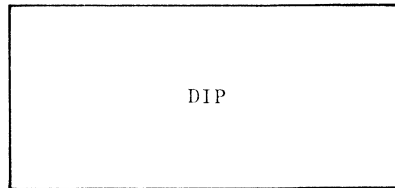
This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

1. Difference in dimension between flat and standard package.

Unit : mm

	Flat package	Standard package
Length	16.5	32.4
Width	9.0	14.2
Lead Pitch	1.27	2.54
Thickness	2.1	5

2. Comparison in occupied space.

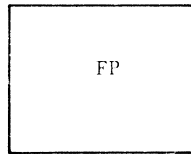


3. Advantage of this package

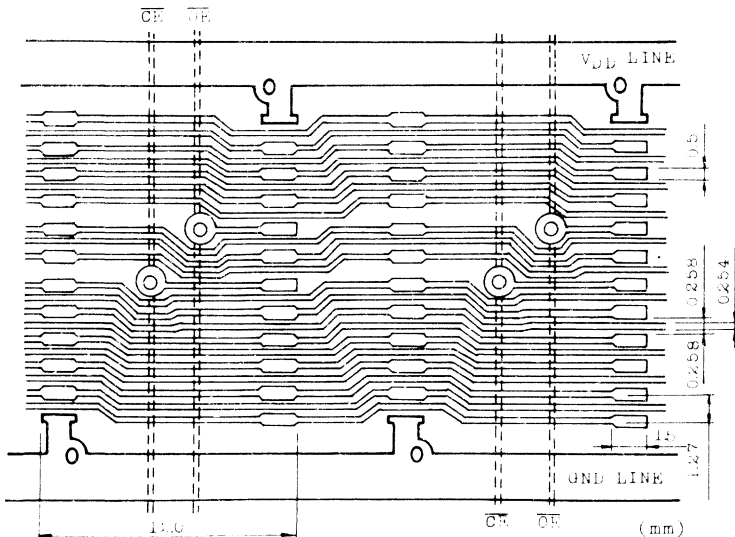
Small dimensions

Capability of High Density Assembly

Capability of thin Assembly — Capability of Assembly on both side of PC board.



4. PC pattern layout example.



**TC5517CP-15/CPL-15/CP-20/CPL-20**  
**TC5517CF-15/CFL-15/CF-20/CFL-20**

Note: Toshiba does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.  
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# TOSHIBA MOS MEMORY PRODUCT

2,048 WORD × 8 BIT CMOS STATIC RAM

TC5518CP-15/CPL-15/CP-20/CPL-20  
TC5518CF-15/CFL-15/CF-20/CFL-20

## DESCRIPTION

The TC5518CP/CF is a 16384-bit high speed and low power sully static random access memory organized as 2048 words by a 8 bits using CMOS technology, and operates from a single 5 volt supply. The TC5518CP/CF has two chip enable inputs, CE1 and CE2, which are used for device selection and can be used in order to achieve minimum standby current mode easily for battery back up. Also the high speed and low power characteristics which maximum access time is 150ns, 200ns and maximum operating current is 5mA/MHz are achieved.

Thus the TC5518CP/CF is most suitable for use in low power applications where battery operation or battery back up for nonvolatility are required. Furthermore the TC5518CPL/CFL guaranteed a standby current equal to or less than 1μA at 60°C ambient temperature available. And the TC5518CP/CPL is pin compatible with 2716 type EPROM. This means that the TC5518CP/CPL and EPROM can be interchanged in the same socket, and the flexibility in the definition of the quantity of RAM versus EPROM allows the wide application in microcomputer system.

## FEATURES

- Low Power Dissipation  
5mA/Max.  
0.2μA(MAX.) at Ta=25°C  
1.0μA(MAX.) at Ta=60°C
- 5V Single PowerSupply
- Low Voltage Operation : V<sub>DD</sub>=3V  
t<sub>CO1,2</sub>=1μs(MAX.) Ta=60°C
- Wide Temperature Operation  
Ta=-40~85°C
- Fully Static Operation
- Data Retention Voltage : 2.0V~5.5V
- Two Chip Enables (CE1, CE2)  
Simple Memory Expansion and Battery Back Up

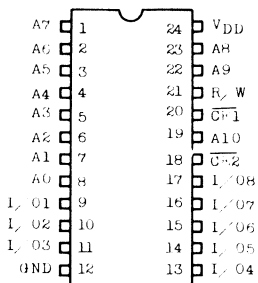
Operating  
Standby  
Standby

## ● Access Time

	TC5518CP-15, CPL-15	TC5518CP-20/CPL-20
	TC5518CF-15 CFL-15	TC5518CF-20/CFL-20
Address Access Time (MAX.)	150ns	200ns
CE1 Access Time (MAX.)	150ns	200ns
CE2 Access Time (MAX.)	150ns	200ns

- Directly TTL Compatible : All Inputs and Outputs
- 24 Pin Standard Plastic Package : TC5518CP
- 24 Pin Flat Package : TC5518CF

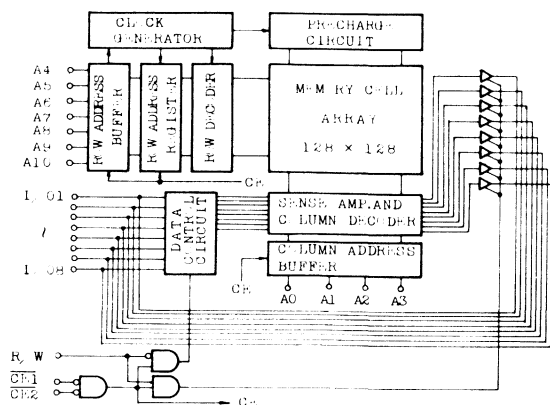
## PIN CONNECTION (TOP VIEW)



## PIN NAMES

A <sub>0</sub> ~A <sub>10</sub>	Address Inputs
R/W	Read/Write Control Input
CE <sub>1</sub> , CE <sub>2</sub>	Chip Enable Inputs
I/O <sub>1</sub> ~I/O <sub>8</sub>	Data Input/Output
V <sub>DD</sub>	Power (+5V)
GND	Ground

## BLOCK DIAGRAM



# TC5518CP-15/CPL-15/CP-20/CPL-20

# TC5518CF-15/CFL-15/CF-20/CFL-20

## OPERATION MODE

MODE	CE <sub>1</sub>	CE <sub>2</sub>	R/W	A <sub>0</sub> ~A <sub>10</sub>	I/O <sub>1</sub> ~I/O <sub>8</sub>	POWER
Read	L	L	H	Stable	Data Out	I <sub>DD0</sub>
Write	L	L	L	Stable	Data In	I <sub>DD0</sub>
** Standby 1	*	H	*	*	High Impedance	I <sub>DD5</sub>
** Standby 2	H	*	*	*	High Impedance	I <sub>DD5</sub>

Note : \* : H or L    \*\* : Data Retention Mode

## ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V <sub>DD</sub>	Power Supply Voltage	-0.3~7.0V
V <sub>IN</sub>	Input Voltage	-0.3V~V <sub>DD</sub> +0.3V
V <sub>I/O</sub>	Input Output Voltage	-0.3V~V <sub>DD</sub> +0.3V
P <sub>D</sub>	Power Dissipation(Ta=85°C)	0.8W(0.45W)*
T <sub>STG</sub>	Storage Temperature	-55°C~150°C
T <sub>OPR</sub>	Operating Temperature	-40°C~85°C
T <sub>SOLDER</sub>	Soldering Temperature·Time	260°C·10sec.

\*Plastic FP=0.45W

## RECOMMENDED D. C. OPERATING CONDITIONS (Ta = -40~85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	--	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	--	0.8	V
V <sub>DH</sub>	Data Retention Voltage	2.0	--	5.5	V

## D. C. CHARACTERISTICS

(Ta = -40~85°C, V<sub>DD</sub> = 5V±10%)

SYMBOL	PARAMETER	CONDITIONS	TC5518CP-15		TC5518CP-20		UNIT		
			CF-15		CF-20				
I <sub>II</sub>	Input Leakage Current	0 ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	--	±1.0	--	±1.0	μA		
I <sub>I/O</sub>	I/O Leakage Current	CE <sub>1</sub> = V <sub>IH</sub> , 0V ≤ V <sub>i</sub> ≤ V <sub>DD</sub>	--	±5.0	--	±5.0	μA		
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4V	-1.0	--	-1.0	--	mA		
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4V	2.0	--	2.0	--	mA		
I <sub>DD51</sub>		CE <sub>1</sub> = 2.2V or CE <sub>2</sub> = 2.2V	--	3.0	--	3.0	mA		
I <sub>DD52</sub>	Standby Current	CE <sub>1</sub> = V <sub>DD</sub> -0.5V or CE <sub>2</sub> = V <sub>DD</sub> -0.5V	TC5518CPL/ CFL	Ta = 25°C	--	0.2	--	0.2	μA
				Ta = 60°C	--	1.0	--	1.0	
		V <sub>DD</sub> = 2~ 5.5V	TC5518CP/ CF	Ta = 25°C	--	1.0	--	1.0	
				Ta = 60°C	--	5.0	--	5.0	
				Ta = 85°C	--	30	--	30	
I <sub>DD01</sub>	Operating Current	t <sub>LOW</sub> = Min cycle, CE <sub>1</sub> = CE <sub>2</sub> = 0V, I <sub>IN</sub> = 0mA	V <sub>IN</sub> = V <sub>IH</sub> , V <sub>i</sub>	--	45	--	30	mA	
V <sub>IN</sub> = V <sub>DD</sub> , GND				--	40	--	25		
I <sub>DD03</sub>		t <sub>LOW</sub> = 1μs, CE <sub>1</sub> = --	V <sub>IN</sub> = V <sub>IH</sub> , V <sub>i</sub>	--	10	--	10		
I <sub>DD02</sub>				CE <sub>1</sub> = 0V, I <sub>IN</sub> = 0mA	V <sub>i</sub> = V <sub>DD</sub> , GND	--	5		--

Note : Typical values are at Ta = 25°C, V<sub>DD</sub> = 5V.

# TC5518CP-15/CPL-15/CP-20/CPL-20 TC5518CF-15/CFL-15/CF-20/CFL-20

## CAPACITANCE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	—	5	10	pF
C <sub>OUT</sub>	Input/Output Capacitance	—	5	10	pF

Note : This parameter is periodically sampled and is not 100% tested.

### A. C. CHARACTERISTICS (Ta = -40~85°C, V<sub>DD</sub> = 5V ± 10%)

#### Read Cycle

SYMBOL	PARAMETER	TC5518CP-15/CPL-15 TC5518CF-15/CFL-15		TC5518CP-20/CPL-20 TC5518CF-20/CFL-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	150	—	200	—	ns
t <sub>ACC</sub>	Address Access Time	—	150	—	200	
t <sub>CO1</sub>	CE <sub>1</sub> to Output Valid	—	150	—	200	
t <sub>CO2</sub>	CE <sub>2</sub> to Output Valid	—	150	—	200	
t <sub>COF</sub>	CE <sub>1</sub> or CE <sub>2</sub> to Output Active	10	—	10	—	
t <sub>OD</sub>	Output High-Z Deselection	—	50	—	60	
t <sub>OH</sub>	Output Hold from Address Change	15	—	20	—	

SYMBOL	PARAMETER	TC5518CP-15/CPL-15 TC5518CF-15/CFL-15		TC5518CP-20/CPL-20 TC5518CF-20/CFL-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	150	—	200	—	ns
t <sub>WP</sub>	Write Pulse Width	120	—	150	—	
t <sub>AW</sub>	Address Set up Time	0	—	0	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	
t <sub>ODW</sub>	Output High-Z from R/W	—	50	—	60	
t <sub>OFW</sub>	Output Active from R/W	10	—	10	—	
t <sub>DS</sub>	Data Set up Time	60	—	80	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	

### A. C. TEST CONDITIONS

Output Load : 100pF + 1TTL Gate

Input Pulse Levels : 0.6V, 2.4V

Timing Measurement Reference Levels

Input : 0.8V and 2.2V

Output : 0.8V and 2.2V

Input Pulse Rise and Fall Times : 10ns

## 3V OPERATE SPECIFICATION

### D. C. RECOMMENDED OPERATING CONDITIONS (Ta = -10~60°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	2.7	3.0	3.3	V
V <sub>IH</sub>	Input High Voltage	V <sub>DD</sub> - 0.2	—	V <sub>DD</sub>	V
V <sub>IL</sub>	Input Low Voltage	0	—	0.2	V

# TC5518CP-15/CPL-15/CP-20/CPL-20

# TC5518CF-15/CFL-15/CF-20/CFL-20

## D. C. CHARACTERISTICS (Ta = -10~60°C)

SYMBOL	PARAMETER CONDIIONS	MIN.		TYP.	MAX.	UNIT		
I <sub>IL</sub>	Input Leakage Current	0V ≤ V <sub>IH</sub> ≤ V <sub>DD</sub>		—	—	±1.0	μA	
I <sub>LO</sub>	Output Leakage Current	$\overline{CE1}$ , 2 = V <sub>IH</sub> , 0V ≤ V <sub>IO</sub> ≤ V <sub>DD</sub>		—	—	±5.0	μA	
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = V <sub>DD</sub> - 0.2V		-100	—	—	μA	
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.2V		100	—	—	μA	
I <sub>DD5</sub>	Standby Current	$\overline{CE1} = \overline{CE2} = V_{IH}$	TC5518CPL/ CFL	Ta = 25°C	—	—	0.2	μA
				Ta = 60°C	—	—	1.0	
			TC5518CP/ CF	Ta = 25°C	—	—	1.0	
				Ta = 60°C	—	—	5.0	
I <sub>DD0</sub>	Operating Current	$\overline{CE1}$ , 2 = 0V, I <sub>OUT</sub> = 0mA t <sub>r</sub> , t <sub>f</sub> ≤ 20nsec		t <sub>cycle</sub> = 1μsec	—	2.0	3.0	mA
				t <sub>cycle</sub> = 10μsec	—	0.3	0.5	

● All voltage is measured from GND.

## A. C. CHARACTERISTICS (Ta = -10~60°C, V<sub>DD</sub> = 3V ± 10%)

### Read CYCLE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t <sub>RC</sub>	Read Cycle Time	1000	—	—	ns
t <sub>ACC</sub>	Address Access Time	—	250	1000	ns
t <sub>CO1</sub>	$\overline{CE1}$ to Output Valid	—	250	1000	ns
t <sub>CO2</sub>	$\overline{CE2}$ to Output Valid	—	250	1000	ns
t <sub>COE</sub>	$\overline{CE1}$ or $\overline{CE2}$ Output Active	10	—	—	ns
t <sub>OD</sub>	Output High-Z Deselection	—	—	200	ns
t <sub>OH</sub>	Output Hold from Address Change	20	—	—	ns

### WRITE CYCLE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t <sub>WC</sub>	Write Cycle Time	1000	—	—	ns
t <sub>WP</sub>	Write Pulse Width	500	—	—	ns
t <sub>AW</sub>	Address Set up Time	100	—	—	ns
t <sub>WR</sub>	Write Recovery Time	100	—	—	ns
t <sub>ODW</sub>	Output High-Z from R/W	—	—	200	ns
t <sub>OEW</sub>	Output Active from R/W	10	—	—	ns
t <sub>DS</sub>	Data Set up Time	400	—	—	ns
t <sub>DH</sub>	Data Hold Time	50	—	—	ns

## A. C. TEST CONDITIONS

Output Load : 100pF (Include Jig)

Input Pulse Levels : 0.2V, V<sub>DD</sub> - 0.2V

Timing Measurement Level Input : 1.5V, 1.5V

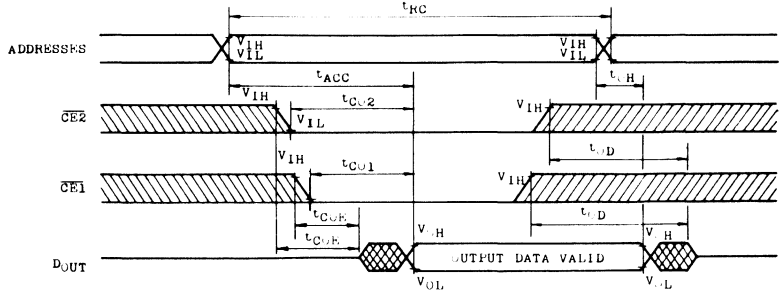
Output : 1.5V, 1.5V

Input Pulse Rise and Fall Times : ≤ 20ns

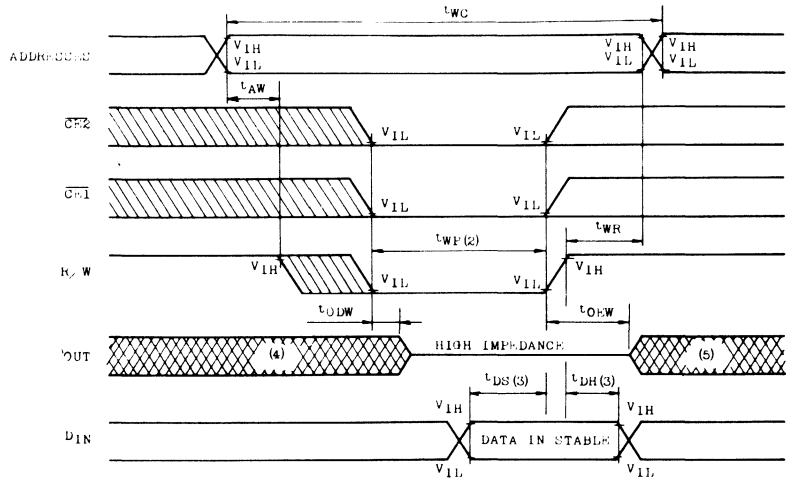
# TC5518CP-15/CPL-15/CP-20/CPL-20 TC5518CF-15/CFL-15/CF-20/CFL-20

## TIMING WAVEFORMS

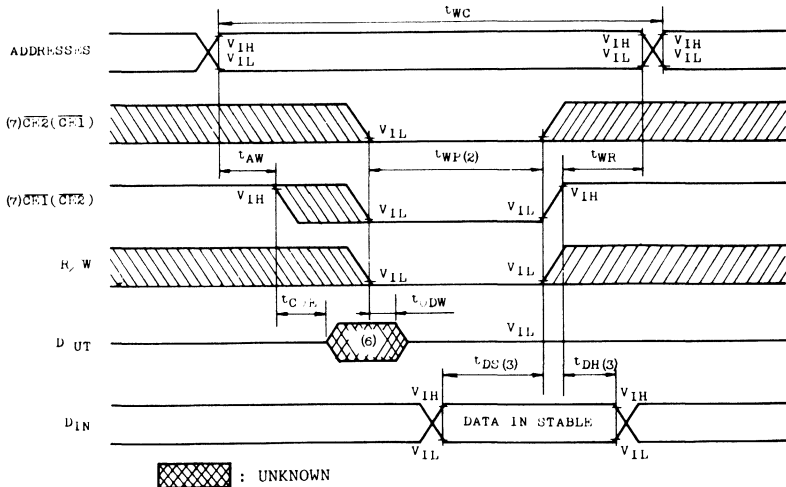
- Read Cycle



- Write Cycle 1 (2)



- Write Cycle 2 (2)



# TC5518CP-15/CPL-15/CP-20/CPL-20

# TC5518CF-15/CFL-15/CF-20/CFL-20

Note :

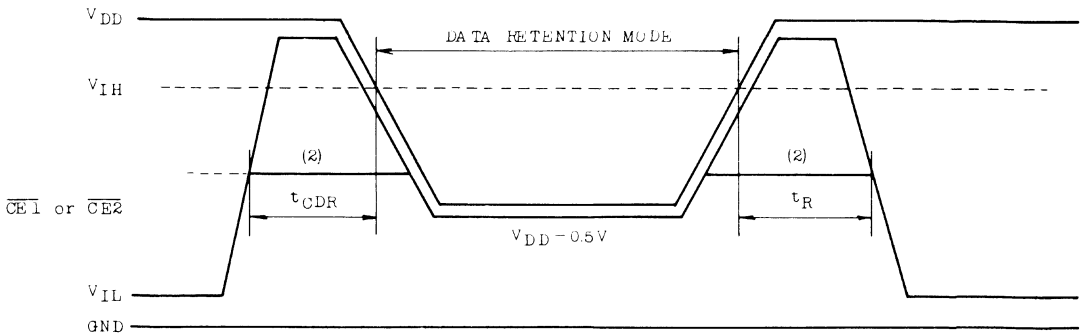
1. R/W is high for a read Cycle.
2.  $t_{WP}$  is specified as logical "AND" of  $\overline{CE_1}$ ,  $\overline{CE_2}$  and R/W.  
 $t_{WP}$  is measured from the latter of  $\overline{CE_1}$ ,  $\overline{CE_2}$  or R/W going low to the earlier of  $\overline{CE_1}$ ,  $\overline{CE_2}$  or R/W going high.
3.  $t_{DH}$ ,  $t_{DS}$  are measured from the earlier of  $\overline{CE_1}$ ,  $\overline{CE_2}$  or R/W going high.
4. If the  $\overline{CE_1}$  or  $\overline{CE_2}$  low transition occurs simultaneously or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
5. If the  $\overline{CE_1}$  or  $\overline{CE_2}$  high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
6. If the R/W is low or the R/W low transition occurs prior to or simultaneously with the  $\overline{CE_1}$  or  $\overline{CE_2}$  low transition, the output buffers remain in a high impedance state in this period.
7. A write occurs during the overlap of a low  $\overline{CE_1}$ , low  $\overline{CE_2}$  and low R/W.  
 In write cycle 2, write is controlled by either  $\overline{CE_1}$  or  $\overline{CE_2}$ .

## DATA RETENTION CHARACTERISTICS (Ta = 40~85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT		
$V_{DH}$	Data Retention Power Supply Voltage	2.0	---	5.5	V		
$I_{DDS2}$	Standby Current	TC5518CPL/CFL	Ta = 25°C	---	0.005	$\mu A$	
			Ta = 60°C	---	1.0		
		TC5518CP/CF	Ta = 25°C	---	0.05		1.0
			Ta = 60°C	---	---		5.0
		Ta = 85°C	---	---	30		
$t_{CDR}$	From Chip Deselection to Data Retention Mode	0	---	---	$\mu S$		
$t_R$	Recovery Time	$t_{rc}(1)$	---	---	ns		

Note :

1.  $t_{RC}$  : Read Cycle Time



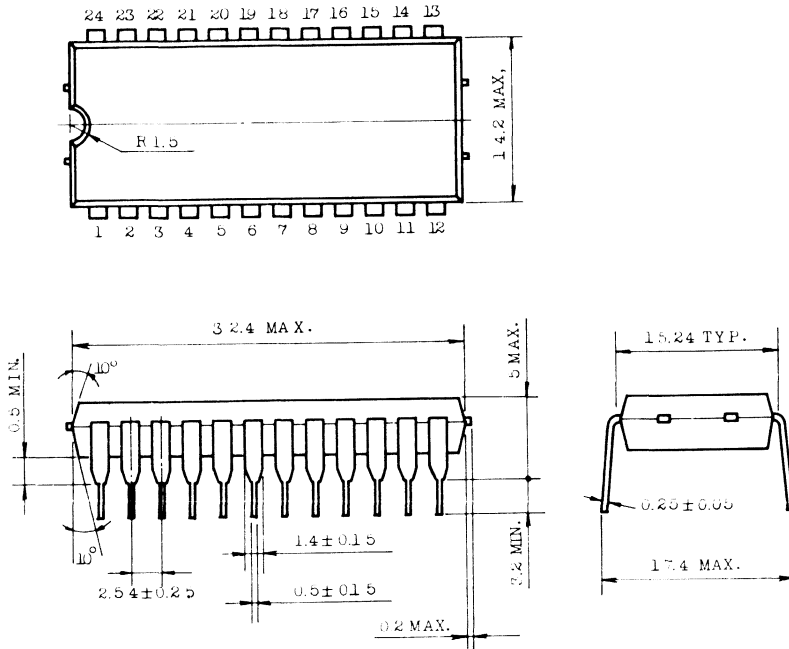
2. If the  $V_{IH}$  level of  $\overline{CE_2}$  ( $\overline{CE_1}$ ) is 2.2V, during the period that the  $V_{DD}$  voltage is going down from 4.5V to 2.7V,  $I_{DDS1}$  current flows.



# TC5518CP-15/CPL-15/CP-20/CPL-20 TC5518CF-15/CFL-15/CF-20/CFL-20

## OUTLINE DRAWINGS

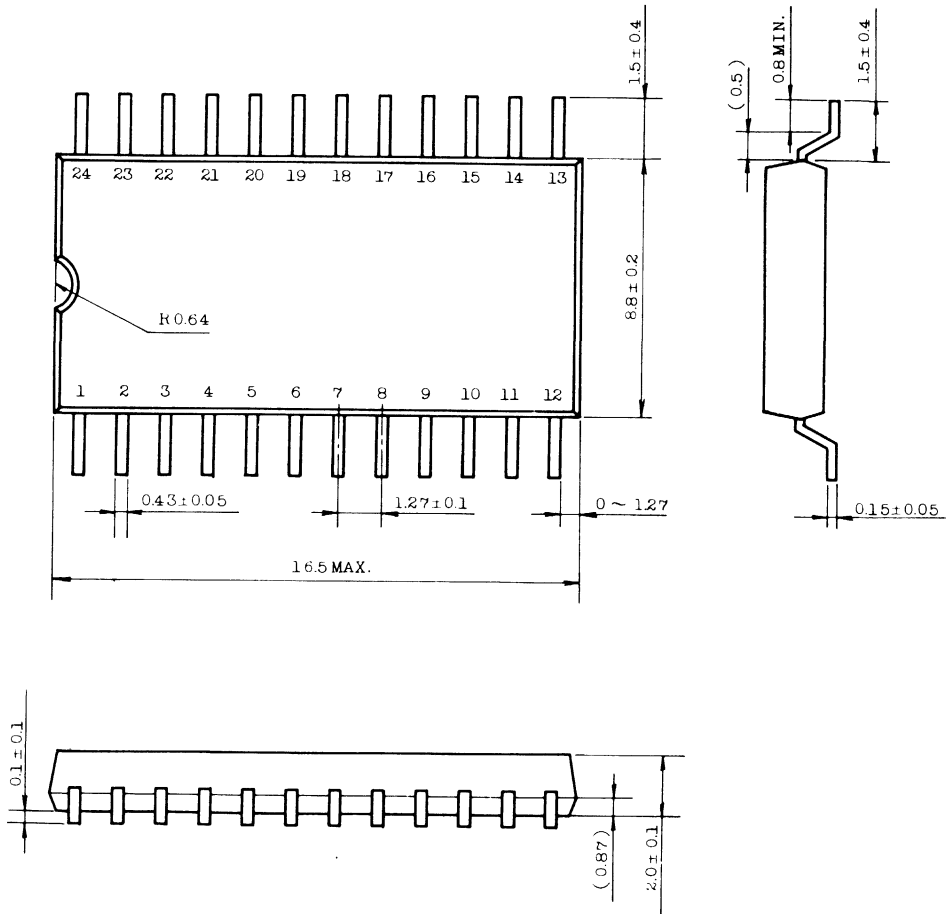
- Plastic DIP



Note : Each lead pitch is 2.54mm.  
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.  
All dimensions are in millimeters.

# TC5518CP-15/CPL-15/CP-20/CPL-20 TC5518CF-15/CFL-15/CF-20/CFL-20

- Plastic FP



Note : Each lead pitch is 1.27mm.  
All leads are located within 0.1mm of their true longitudinal position with respect to No.1 and No.24 leads.

# TC5518CP-15/CPL-15/CP-20/CPL-20 TC5518CF-15/CFL-15/CF-20/CFL-20

## PACKAGE INFORMATION FOR FLAT PACKAGE

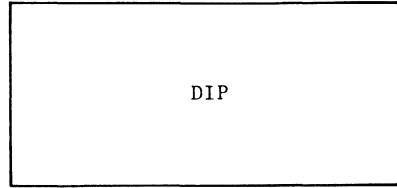
This new flat package is a very small and this compared with conventional standard dual-in-line package. Differences as follows.

1. Difference in dimension between flat and standard package.

Unit : mm

	Flat package	Standard package
Length	16.5	32.4
Width	9.0	14.2
Lead Pitch	1.27	2.54
Thickness	2.1	5

2, Comparison in occupied space



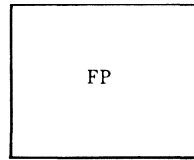
3. Advantage of this package

Small dimensions

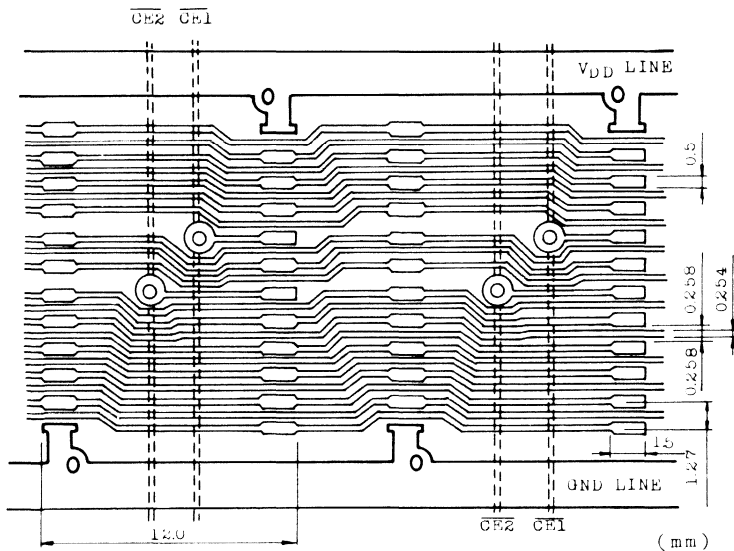
Capability of High Density Assembly

Capability of thin Assembly —

Capability of Assembly on both side of PC board



4. PC pattern layout example



**TC5518CP-15/CPL-15/CP-20/CPL-20**  
**TC5518CF-15/CFL-15/CF-20/CFL-20**

Note: Toshiba does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied, and Toshiba reserves the right at any time without notice, to change said circuitry.  
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# TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD × 8 BIT STATIC RAM  
N-CHANNEL SILICON GATE MOS

## TMM2063P-10, TMM2063P-12 TMM2063P-15

### DESCRIPTION

The TMM2063P is a 65,536 bits high speed and low power static random access memory organized as 8,192 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 100ns/120ns/150ns and maximum operating current of 80mA. When  $\overline{CS}_1$  is a logical high or  $\overline{CS}_2$  is a logical low, the device is placed in a low power standby

mode in which maximum standby current is 10mA. Thus the TMM2063P is most suitable for use in microcomputer peripheral memory where the low power applications are required, moreover, suitable for use in high density assembly as 0.3 inch width package is use for. The TMM2063P is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

### FEATURES

#### ● Access Time and Current

Part Number	Parameter	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2063P-10		100ns	80mA	10mA
TMM2063P-12		120ns	80mA	10mA
TMM2063P-15		150ns	80mA	10mA

#### ● High Density Assembly Capability : 0.3 inch width package (28 pin plastic DIP)

#### ● Single 5V Power Supply

#### ● Fully Static Operation

#### ● Power Down Feature : $\overline{CS}_1$ , $\overline{CS}_2$

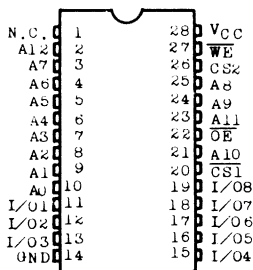
#### ● Output Buffer Control : $\overline{OE}$

#### ● Three State Outputs

#### ● All Inputs and Outputs : Directly TTL Compatible

#### ● Inputs Protected : All inputs have protection against static charge

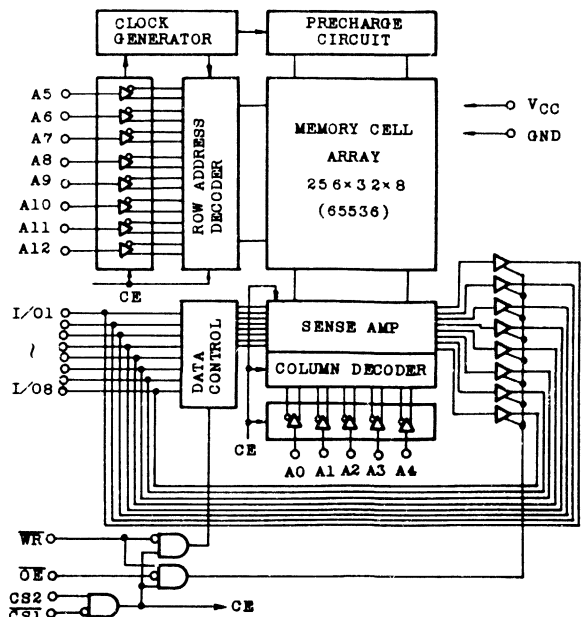
### PIN CONNECTION



### PIN NAMES

SYMBOL	NAME
A <sub>0</sub> ~A <sub>4</sub>	Column Address Inputs
A <sub>5</sub> ~A <sub>12</sub>	Row Address Inputs
$\overline{CS}_1$ , $\overline{CS}_2$	Chip Select Inputs
$\overline{WE}$	Write Enable Input
I/O <sub>1</sub> ~I/O <sub>8</sub>	Data Input/Output
$\overline{OE}$	Output Enable Input
V <sub>CC</sub>	Power (+5V)
GND	Ground
N. C.	No Connection

### BLOCK DIAGRAM



# TMM2063P-10, TMM2063P-12 TMM2063P-15

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	Power Supply Voltage	-0.5~7.0	V
V <sub>IN</sub> , V <sub>OUT</sub>	Input/Output Voltage	-0.5*~7.0	V
T <sub>OPR</sub>	Operating Temperature	0~70	°C
T <sub>STG</sub>	Storage Temperature	-55~150	°C
T <sub>SOLDER</sub>	Soldering Temperature · Time	260 · 10	°C·sec
P <sub>D</sub>	Power Dissipation (Ta = 70°C)	0.8	W

\* -3.0V at Pulse width 50ns

## D. C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.0	—	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input Low Voltage	-0.5**	—	0.8	V
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V

\*\* -3.0V at Pulse width 50ns

## D. C. CHARACTERISTICS (Ta=0~70°C, V<sub>CC</sub>=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> =0V~5.5V	-10	—	10	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OUT</sub> =-1.0mA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OUT</sub> =2.1mA	—	—	0.4	V
I <sub>LO</sub>	Output Leakage Current	CS <sub>1</sub> =V <sub>IH</sub> or CS <sub>2</sub> =V <sub>IL</sub> or WE=V <sub>IL</sub> or OE=V <sub>IH</sub> , V <sub>OUT</sub> =0V~5.5V	-10	—	10	μA
I <sub>SBP</sub>	Peak Power-on Current	CS <sub>1</sub> =V <sub>CC</sub> , CS <sub>2</sub> =0V I <sub>OUT</sub> =0mA	—	—	20	mA
I <sub>SB</sub>	Standby Current	CS <sub>1</sub> =V <sub>IH</sub> or CS <sub>2</sub> =V <sub>IL</sub> , I <sub>OUT</sub> =0mA	—	—	10	mA
I <sub>CC</sub>	Operating Current	CS <sub>1</sub> =V <sub>IL</sub> , CS <sub>2</sub> =V <sub>IH</sub> , I <sub>OUT</sub> =0mA	—	—	80	mA

## CAPACITANCE\*\*\* (Ta=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =0V	5	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>IN</sub> =0V	10	pF

\*\*\* Note : This parameter is periodically sampled and is not 100% tested.

# TMM2063P-10, TMM2063P-12 TMM2063P-15

## A. C. CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V ± 10%)

### Read Cycle

SYMBOL	PARAMETER	TMM2063P-10		TMM2063P-12		TMM2063P-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	100	—	120	—	150	—	ns
t <sub>ACC</sub>	Address Access Time	—	100	—	120	—	150	
t <sub>CO1</sub>	CS <sub>1</sub> Access Time	—	100	—	120	—	150	
t <sub>CO2</sub>	CS <sub>2</sub> Access Time	—	100	—	120	—	150	
t <sub>OE</sub>	OE Access Time	—	40	—	50	—	60	
t <sub>OH</sub>	Output Data Hold Time from Address Change	10	—	10	—	10	—	
t <sub>CLZ</sub>	CS <sub>1</sub> or CS <sub>2</sub> to Output in Low-Z	10	—	10	—	10	—	
t <sub>CHZ</sub>	CS <sub>1</sub> or CS <sub>2</sub> to Output in High-Z	—	40	—	40	—	55	
t <sub>OLZ</sub>	OE to Output in Low-Z	5	—	5	—	5	—	
t <sub>OHZ</sub>	OE to Output in High-Z	—	35	—	35	—	50	
t <sub>PU</sub>	Chip Selection to Power Up Time	0	—	0	—	0	—	
t <sub>PD</sub>	Chip Deselection to Power Down Time	—	50	—	60	—	60	

### Write Cycle

SYMBOL	PARAMETER	TMM2063P-10		TMM2063P-12		TMM2063P-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	100	—	120	—	150	—	ns
t <sub>CW</sub>	Chip Selection to End of Write	80	—	100	—	120	—	
t <sub>AS</sub>	Address Set Up Time	10	—	10	—	10	—	
t <sub>WP</sub>	Write Pulse Width	70	—	85	—	100	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	
t <sub>DS</sub>	Data Set Up Time	40	—	50	—	60	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	
t <sub>WLZ</sub>	$\overline{WE}$ to Output in Low-Z	5	—	5	—	5	—	
t <sub>WHZ</sub>	$\overline{WE}$ to Output in High-Z	—	30	—	35	—	40	

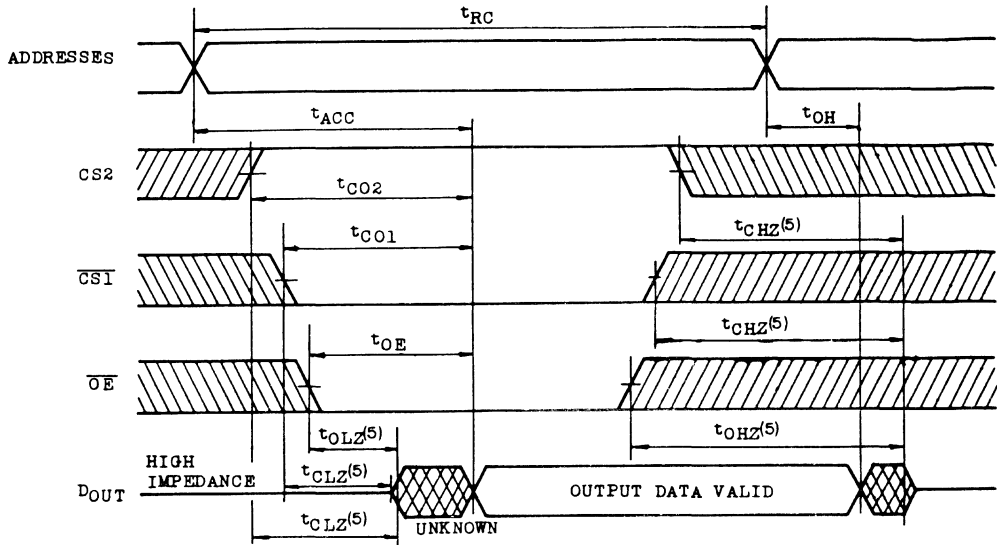
## A. C. TEST CONDITIONS

Input Pulse Levels	V <sub>IH</sub> = 2.2V, V <sub>IL</sub> = 0.6V
Input Rise and Fall Time	10ns
Input and Output Reference Levels	1.5V
Output Load	1 TTL Gate & C <sub>L</sub> = 100pF

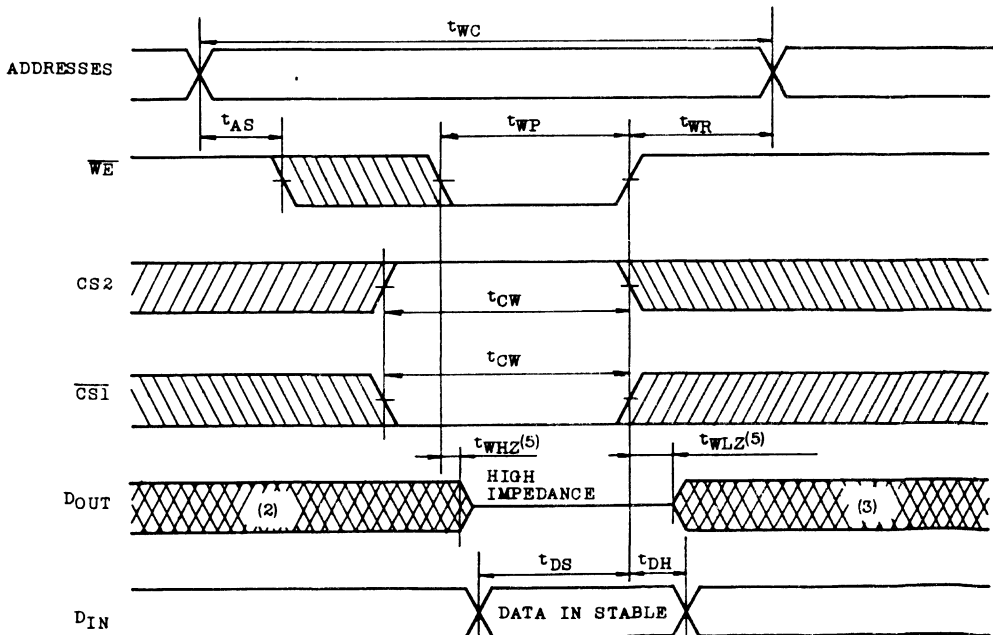
# TMM2063P-10, TMM2063P-12 TMM2063P-15

## TIMING WAVEFORMS

### ● READ CYCLE (1)



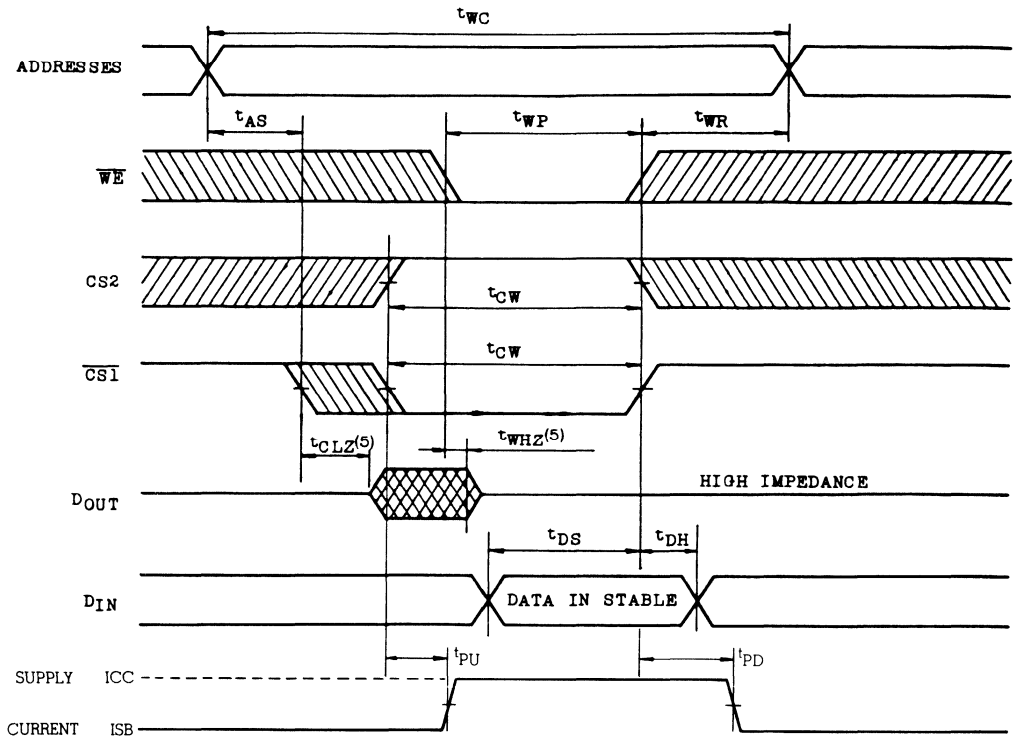
### ● WRITE CYCLE 1 (4) ( $\overline{WE}$ Controlled Write)



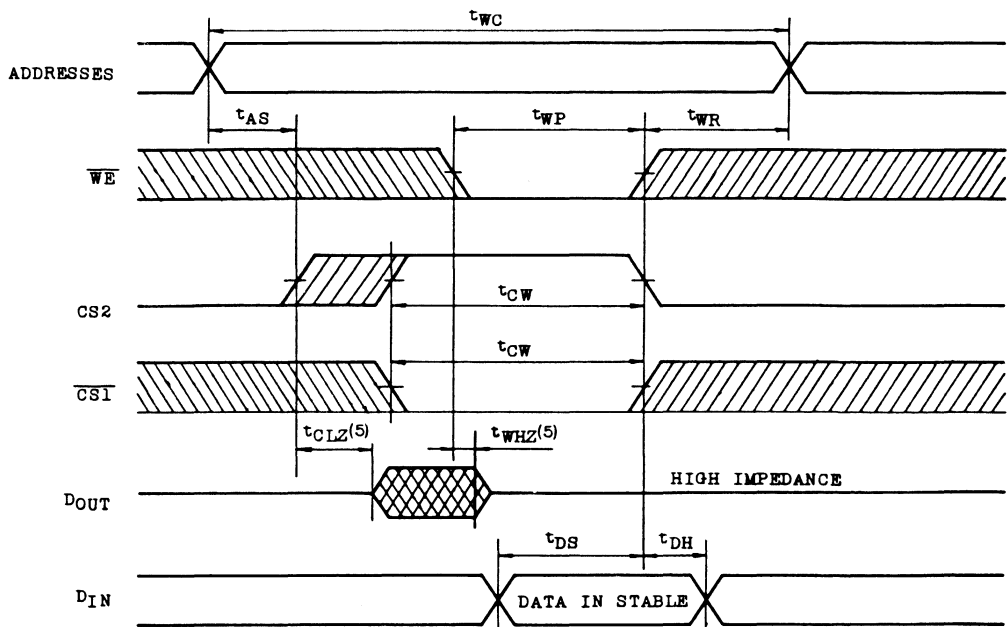


# TMM2063P-10, TMM2063P-12 TMM2063P-15

● WRITE CYCLE 2 (4) ( $\overline{CS1}$  Controlled Write)



● WRITE CYCLE 3 (4) ( $\overline{CS2}$  Controlled Write)



# TMM2063P-10, TMM2063P-12 TMM2063P-15

Note :

1.  $\overline{WE}$  is High for Read Cycle.
2. Assuming that  $\overline{CS}_1$  Low transition or  $CS_2$  High transition occurs coincident with or after  $\overline{WE}$  Low transition, Outputs remain in a high impedance state.
3. Assuming that  $\overline{CS}_1$  High transition or  $CS_2$  Low transition occurs coincident with or prior to  $\overline{WE}$  High transition, Outputs remain in a high impedance state.
4. Assuming that  $\overline{OE}$  is High for Write Cycle, Outputs are in high impedance state during this period.
5. These parameters are specified as follows and measured by using the load shown in Fig. 1.
  - (A)  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{WLZ}$ .....Output Enable Time
  - (B)  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$ .....Output Disable Time

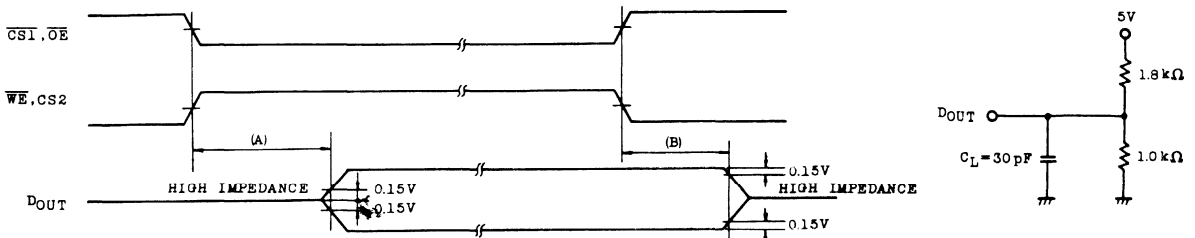
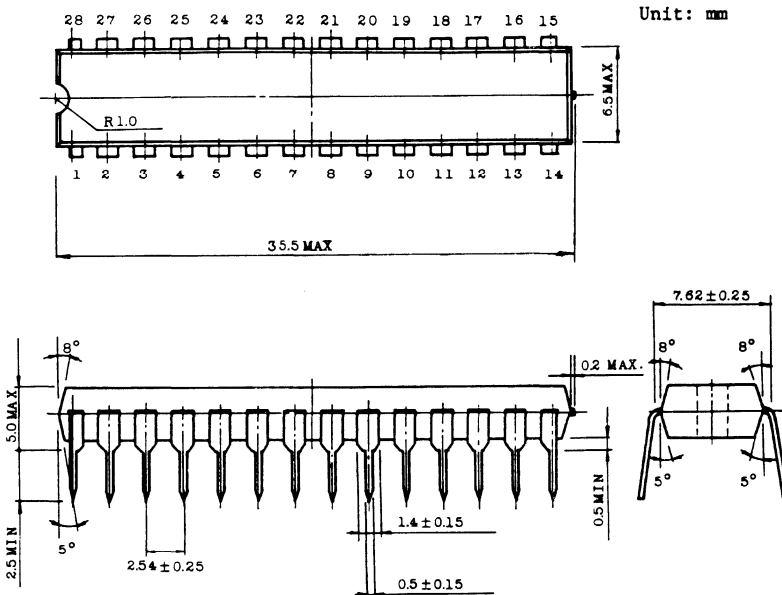


Fig. 1 Output load condition for enable disable time measurement

## OUTLINE DRAWINGS



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No.28 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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# TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD × 8 BIT STATIC RAM TMM2064P-10, TMM2064P-12  
N-CHANNEL SILICON GATE MOS TMM2064P-15

## DESCRIPTION

The TMM2064P is a 65,536 bits high speed and low power static random access memory organized as 8,192 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 100ns/120ns/150ns and maximum operating current of 80mA. When  $\overline{CS}_1$  is a logical high or  $\overline{CS}_2$  is a logical

low, the device is placed in a low power standby mode in which maximum standby current is 10mA. Thus the TMM2064P is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2064P is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

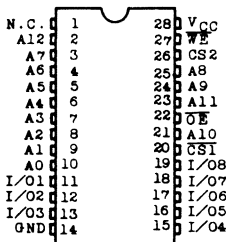
## FEATURES

### ● Access Time and Current

Part Number	Parameter	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2064P-10		100ns	80mA	10mA
TMM2064P-12		120ns	80mA	10mA
TMM2064P-15		150ns	80mA	10mA

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature :  $\overline{CS}_1$   $\overline{CS}_2$
- Output Buffer Control :  $\overline{OE}$
- Three State Outputs
- All Inputs and Outputs : Directly TTL Compatible
- Inputs Protected : All inputs have protection against static charge.

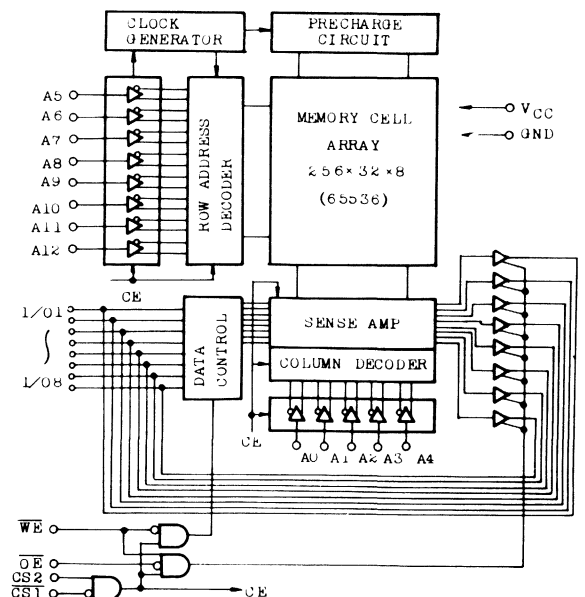
## PIN CONNECTION



## PIN NAMES

SYMBOL	NAME
$A_0 \sim A_4$	Column Address Inputs
$A_5 \sim A_{12}$	Row Address Inputs
$\overline{CS}_1, \overline{CS}_2$	Chip Select Inputs
$\overline{WE}$	Write Enable Input
$I/O_1 \sim I/O_8$	Data Input/Output
$\overline{OE}$	Output Enable Input
$V_{CC}$	Power (5V)
GND	Ground
N. C.	No Connection

## BLOCK DIAGRAM



# TMM2064P-10, TMM2064P-12 TMM2064P-15

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	Power Supply Voltage	-0.5~7.0	V
V <sub>IN</sub> , V <sub>OUT</sub>	Input/Output Voltage	-0.5*~7.0	V
T <sub>OPR</sub>	Operating Temperature	0~70	°C
T <sub>STG</sub>	Storage Temperature	-55~150	°C
T <sub>SOLDER</sub>	Soldering Temperature · Time	260 · 10	°C·sec
P <sub>D</sub>	Power Dissipation (Ta=70°C)	1.0	W

\* -3.0V at Pulse width 50ns

## D. C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.0	—	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input Low Voltage	-0.5**	—	0.8	V
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V

\*\* -3.0V at Pulse width 50ns

## D. C. CHARACTERISTICS (Ta=0~70°C, V<sub>CC</sub>=5.0V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> =0V~5.5V	-10	—	10	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OUT</sub> =-1.0mA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OUT</sub> =2.1mA	—	—	0.4	V
I <sub>LO</sub>	Output Leakage Current	CS <sub>1</sub> =V <sub>IH</sub> or CS <sub>2</sub> =V <sub>IL</sub> or WE=V <sub>IL</sub> or OE=V <sub>IH</sub> , V <sub>OUT</sub> =0V~5.5V	-10	—	10	μA
I <sub>SBP</sub>	Peak Power-on Current	CS <sub>1</sub> =V <sub>CC</sub> , CS <sub>2</sub> =0V I <sub>OUT</sub> =0mA	—	—	20	mA
I <sub>SB</sub>	Standby Current	CS <sub>1</sub> =V <sub>IH</sub> or CS <sub>2</sub> =V <sub>IL</sub> , I <sub>OUT</sub> =0mA	—	—	10	mA
I <sub>CC</sub>	Operating Current	CS <sub>1</sub> =V <sub>IL</sub> , CS <sub>2</sub> =V <sub>IH</sub> , I <sub>OUT</sub> =0mA	—	—	80	mA

## CAPACITANCE\*\*\* (Ta=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =0V	5	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>IN</sub> =0V	10	pF

\*\*\* Note : This parameter is periodically sampled and is not 100% tested.

# TMM2064P-10, TMM2064P-12 TMM2064P-15

## A. C. CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%)

### Read Cycle

SYMBOL	PARAMETER	TMM2064P-10		TMM2064P-12		TMM2064P-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	100	—	120	—	150	—	ns
t <sub>ACC</sub>	Address Access Time	—	100	—	120	—	150	
t <sub>CO1</sub>	CS <sub>1</sub> Access Time	—	100	—	120	—	150	
t <sub>CO2</sub>	CS <sub>2</sub> Access Time	—	100	—	120	—	150	
t <sub>OE</sub>	OE Access Time	—	40	—	50	—	60	
t <sub>OH</sub>	Output Data Hold Time from Address Change	10	—	10	—	10	—	
t <sub>CLZ</sub>	CS <sub>1</sub> or CS <sub>2</sub> to Output in Low-Z	10	—	10	—	10	—	
t <sub>CHZ</sub>	CS <sub>1</sub> or CS <sub>2</sub> to Output in High-Z	—	40	—	40	—	55	
t <sub>OLZ</sub>	OE to Output in Low-Z	5	—	5	—	5	—	
t <sub>OHZ</sub>	OE to Output in High-Z	—	35	—	35	—	50	
t <sub>PU</sub>	Chip Selection to Power Up Time	0	—	0	—	0	—	
t <sub>PD</sub>	Chip Deselection to Power Down Time	—	50	—	60	—	60	

### Write Cycle

SYMBOL	PARAMETER	TMM2064P-10		TMM2064P-12		TMM2064P-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	100	—	120	—	150	—	ns
t <sub>CW</sub>	Chip Selection to End of Write	80	—	100	—	120	—	
t <sub>AS</sub>	Address Set Up Time	10	—	10	—	10	—	
t <sub>WP</sub>	Write Pulse Width	70	—	85	—	100	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	
t <sub>DS</sub>	Data Set Up Time	40	—	50	—	60	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	
t <sub>WLZ</sub>	WE to Output in Low-Z	5	—	5	—	5	—	
t <sub>WHZ</sub>	WE to Output in High-Z	—	30	—	35	—	40	

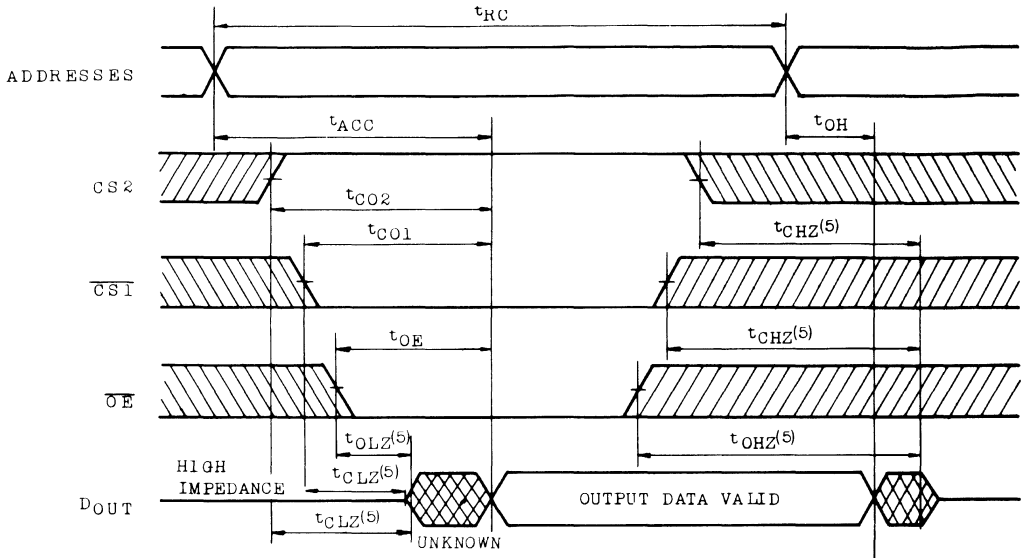
## A. C. TEST CONDITIONS

Input Pulse Levels	V <sub>IH</sub> =2.2V, V <sub>IL</sub> =0.6V
Input Rise and Fall Time	10ns
Input and Output Reference Levels	1.5V
Output Load	1 TTL Gate & C <sub>L</sub> =100pF

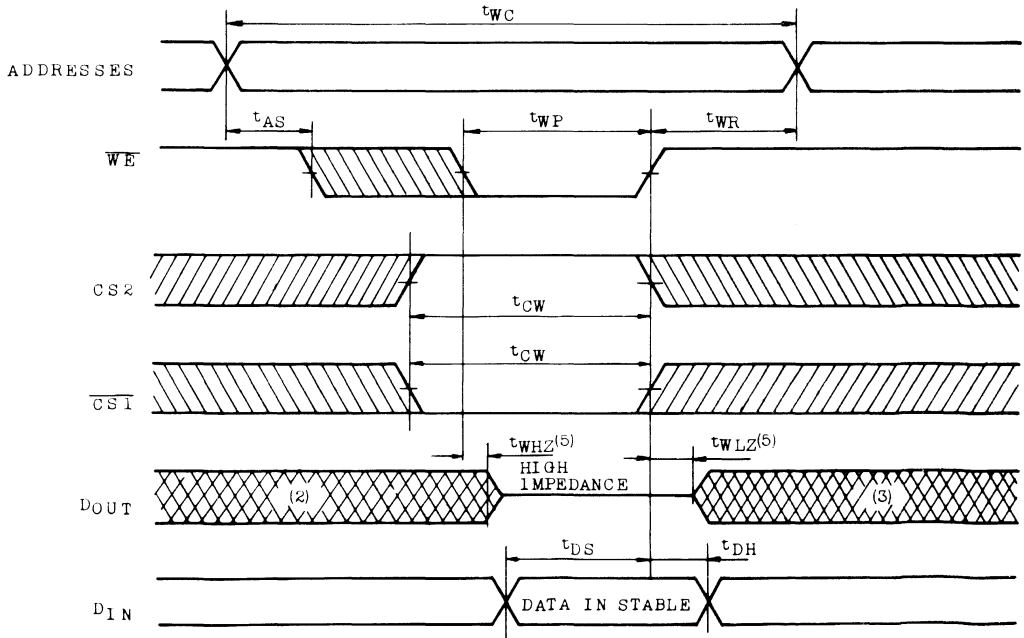
# TMM2064P-10, TMM2064P-12 TMM2064P-15

## TIMING WAVEFORMS

### ● READ CYCLE (1)

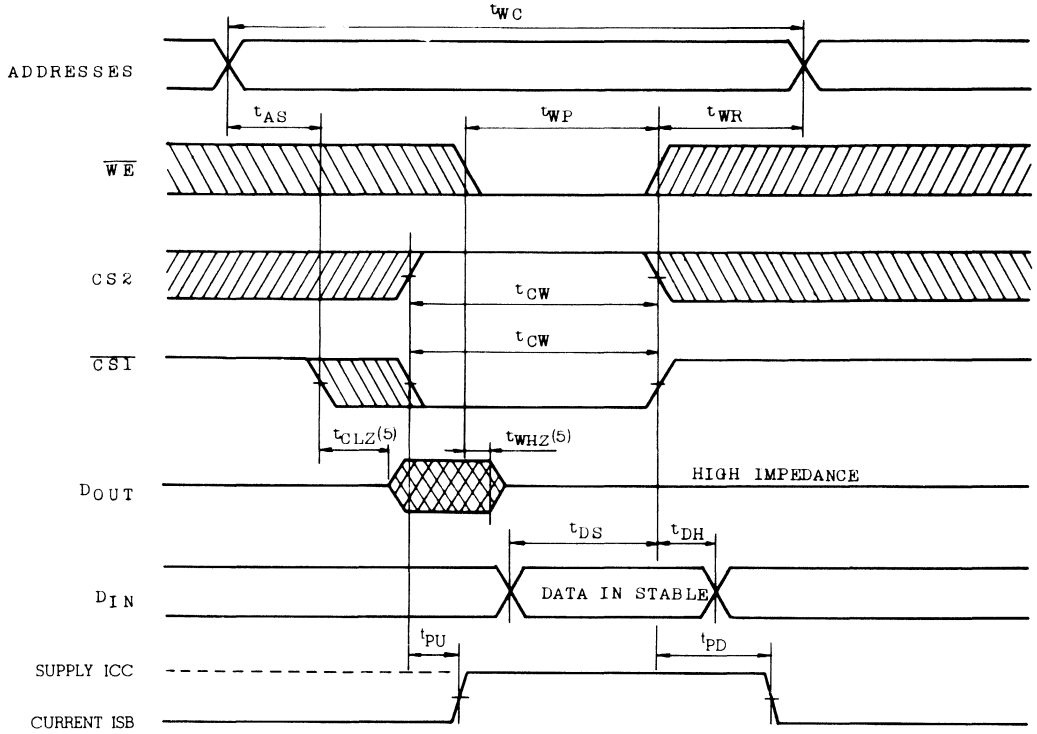


### ● WRITE CYCLE 1 (4) ( $\overline{WE}$ Controlled Write)

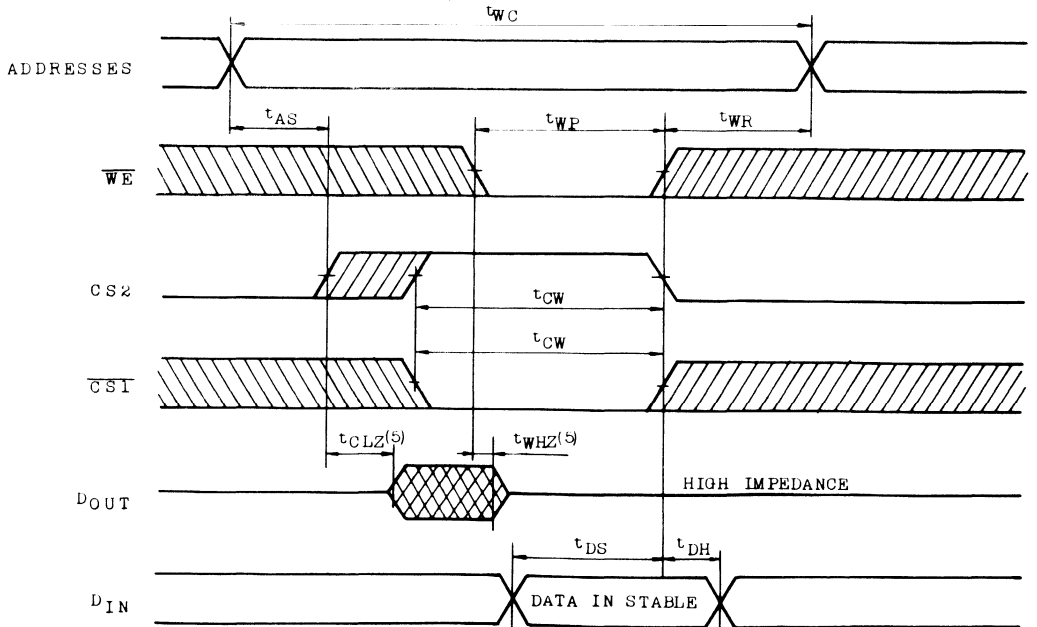


# TMM2064P-10, TMM2064P-12 TMM2064P-15

## ● WRITE CYCLE 2 (4) ( $\overline{CS1}$ Controlled Write)



## ● WRITE CYCLE 3 (4) ( $CS2$ Controlled Write)



# TMM2064P-10, TMM2064P-12 TMM2064P-15

Note :

1.  $\overline{WE}$  is High for Read Cycle.
2. Assuming that  $\overline{CS1}$  Low transition or  $\overline{CS2}$  High transition occurs coincident with or after  $\overline{WE}$  Low transition, Outputs remain in a high impedance state.
3. Assuming that  $\overline{CS1}$  High transition or  $\overline{CS2}$  Low transition occurs coincident with or prior to  $\overline{WE}$  High transition, Outputs remain in a high impedance state.
4. Assuming that  $\overline{OE}$  is High for Write Cycle, Outputs are in high impedance state during this period.
5. These parameters are specified as follows and measured by using the load shown in Fig. 1.
  - (A)  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{WLZ}$ .....Output Enable Time
  - (B)  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$ .....Output Disable Time

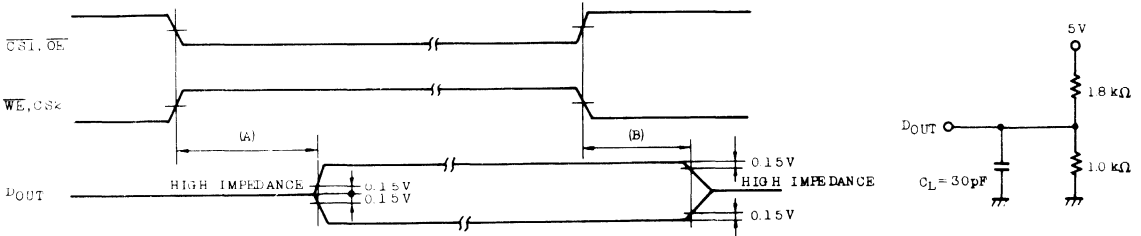
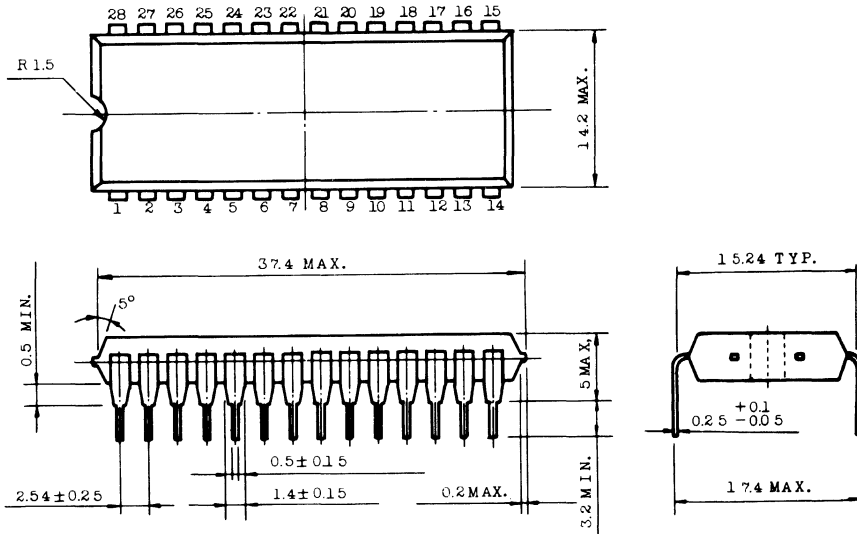


Fig. 1 Output load condition for enable disable time measurement.

## OUTLINE DRAWINGS

Unit: mm



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No.28 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described. no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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# TOSHIBA MOS MEMORY PRODUCT

8,192 WORD × 8 BIT CMOS STATIC RAM  
SILICON GATE CMOS

TC5563APL-10, TC5563APL-12  
TC5563APL-15

PRELIMINARY

## DESCRIPTION

The TC5563APL is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns.

When CE<sub>2</sub> is a logical low or CE<sub>1</sub> is a logical high, the device is placed in low power standby mode in which standby current is 2μA typically. The TC5563APL has three control inputs. Two chip enables (CE<sub>1</sub>, CE<sub>2</sub>) allow for device selection and data retention control, and an output enable input

(OE) provides fast memory access. Thus the TC5563APL is suitable for use in various micro-processor application systems where high speed, low power, and battery back up are required.

The TC5563APL also features pin compatibility with the 64k bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.

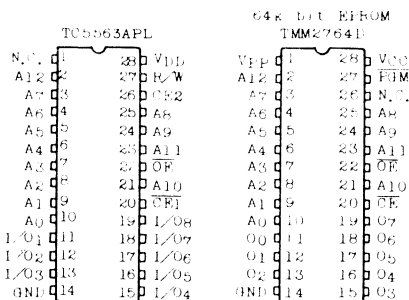
The TC5563APL is offered in a dual-in-line 28 pin 0.3 inch width plastic package.

## FEATURES

- Low Power Dissipation  
27.5mW/MHz (MAX.) Operating
- Standby Current : 100μA (Max.) Ta = 70°C
- Access Time  
TC5563APL-10 : 100ns (Max.)  
TC5563APL-12 : 120ns (Max.)  
TC5563APL-15 : 150ns (Max.)
- 5V Single Power Supply

- Power Down Features : CE<sub>2</sub>, CE<sub>1</sub>
- Fully Static Operation
- Data Retention Supply Voltage : 2.0~5.5V
- Directly TTL Compatible
- All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package Type)

## PIN CONNECTION (TOP VIEW)



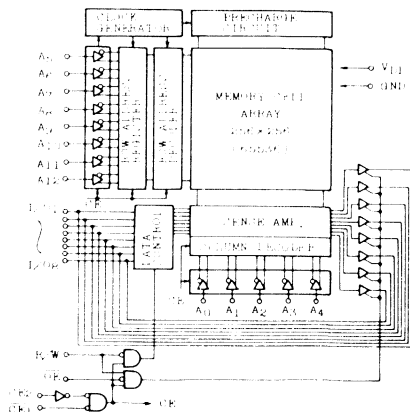
## PIN NAMES

A <sub>0</sub> ~A <sub>12</sub>	Address Inputs
R <sub>2</sub> W	Read Write Control Input
OE	Output Enable Input
CE <sub>1</sub> , CE <sub>2</sub>	Chip Enable Inputs
I/O <sub>0</sub> ~I/O <sub>3</sub>	Data Input/Output
V <sub>DD</sub>	Power (+5V)
GND	Ground
N. C.	No Connection

Package Type	Device Name
600 mil DIP	*TC5565APL
300 mil DIP (Slim Package)	TC5563APL
Flat Package(SOP)	*TC5565AFL

\* ) See TC5565APL Technical Data.

## BLOCK DIAGRAM



# TC5563APL-10, TC5563APL-12 TC5563APL-15

## OPERATION MODE

OPERATION MODE	CE <sub>1</sub>	CE <sub>2</sub>	OE	R/W	I/O <sub>1</sub> ~I/O <sub>n</sub>	POWER
Read	L	H	L	H	D <sub>OUT</sub>	I <sub>DD0</sub>
Write	L	H	*	L	D <sub>IN</sub>	I <sub>DD0</sub>
Output Deselect	L	H	H	H	High-Z	I <sub>DD0</sub>
Standby	H	*	*	*	High-Z	I <sub>DD5</sub>
	*	L	*	*	High-Z	I <sub>DD5</sub>

\* : H or L

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.3~7.0	V
V <sub>IN</sub>	Input Voltage	-0.3*~7.0	V
V <sub>I/O</sub>	Input and Output Voltage	-0.5~V <sub>DD</sub> +0.5	V
P <sub>D</sub>	Power Dissipation	0.8	W
T <sub>SOLDER</sub>	Soldering Temperature	260±10	C·Sec
T <sub>STG</sub>	Storage Temperature	-55~150	C
T <sub>OPR</sub>	Operating Temperature	0~70	C

\* : -3.0V at Pulse width 50ns

## D. C RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3*	—	0.8	V
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	—	5.5	V

\* : -3.0V at Pulse width 50ns

## D. C and OPERATING CHARACTERISTICS (Ta=0~70°C, V<sub>DD</sub>=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> =0~V <sub>DD</sub>	—	—	±1.0	μA	
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> =2.4V	-1.0	—	—	mA	
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> =0.4V	4.0	—	—	mA	
I <sub>LO</sub>	Output Leakage Current	CE <sub>1</sub> =V <sub>IH</sub> or CE <sub>2</sub> =V <sub>IL</sub> or R/W=V <sub>IL</sub> or OE=V <sub>IH</sub> V <sub>OUT</sub> =0~V <sub>DD</sub>	—	—	±1.0	μA	
I <sub>DD01</sub>	Operating Current	V <sub>DD</sub> =5.5V I <sub>out</sub> =0mA CE <sub>1</sub> =V <sub>IL</sub> CE <sub>2</sub> =V <sub>IH</sub> Other Input =V <sub>IH</sub> /V <sub>IL</sub>	t <sub>CYCLE</sub> =1μs	—	—	10	mA
			t <sub>CYCLE</sub> =Min. cycle	—	—	45	mA
I <sub>DD02</sub>	Operating Current	V <sub>DD</sub> =5.5V CE <sub>1</sub> =0.2V CE <sub>2</sub> =V <sub>DD</sub> -0.2V Other Input I <sub>out</sub> =0mA =V <sub>DD</sub> -0.2V/0.2V	t <sub>CYCLE</sub> =1μs	—	—	5	mA
			t <sub>CYCLE</sub> =Min. cycle	—	—	40	mA
I <sub>DD51</sub>	Standby Current	CE <sub>1</sub> =V <sub>IH</sub> or CE <sub>2</sub> =V <sub>IL</sub>	—	—	3	mA	
*I <sub>DD52</sub>	Standby Current	CE <sub>1</sub> =V <sub>DD</sub> -0.2V or CE <sub>2</sub> =0.2V V <sub>DD</sub> =2.0~5.5V	—	2	100	μA	

\* : In standby mode with CE<sub>1</sub>≥V<sub>DD</sub>-0.2V, these specification limits are guaranteed under the condition of CE<sub>2</sub>≥V<sub>DD</sub>-0.2V or CE<sub>2</sub>≤0.2V.

# TC5563APL-10, TC5563APL-12 TC5563APL-15

## CAPACITANCE (Ta = 25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = GND	10	pF

Note: This parameter periodically sampled is not 100% tested.

## A. C. CHARACTERISTICS (Ta = 0 ~ 70°C, V<sub>DD</sub> = 5V ± 10%)

### Read Cycle

SYMBOL	PARAMETER	TC5563APL-10		TC5563APL-12		TC5563APL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	100	—	120	—	150	—	ns
t <sub>ACC</sub>	Address Access Time	—	100	—	120	—	150	ns
t <sub>CE1</sub>	CE1 Access Time	—	100	—	120	—	150	ns
t <sub>CE2</sub>	CE2 Access Time	—	100	—	120	—	150	ns
t <sub>OE</sub>	Output Enable to Output Valid	—	50	—	60	—	70	ns
t <sub>COF</sub>	Chip Enable (CE1, CE2) to Output in Low-Z	10	—	10	—	15	—	ns
t <sub>OEF</sub>	Output Enable to Output in Low-Z	5	—	5	—	5	—	ns
t <sub>OD</sub>	Chip Enable (CE1, CE2) to Output in High-Z	—	35	—	40	—	50	ns
t <sub>ODS</sub>	Output Enable to Output in High-Z	—	35	—	40	—	50	ns
t <sub>OH</sub>	Output Data Hold Time	20	—	20	—	20	—	ns

### Write Cycle

SYMBOL	PARAMETER	TC5563APL-10		TC5563APL-12		TC5563APL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	100	—	120	—	150	—	ns
t <sub>WP</sub>	Write Pulse Width	60	—	70	—	90	—	ns
t <sub>CW</sub>	Chip Selection to End of Write	80	—	85	—	100	—	ns
t <sub>AS</sub>	Address Set up Time	0	—	0	—	0	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	ns
t <sub>ODW</sub>	R/W to Output in High-Z	—	35	—	40	—	50	ns
t <sub>OEW</sub>	R/W to Output in Low-Z	5	—	5	—	10	—	ns
t <sub>DS</sub>	Data Set Up Time	40	—	50	—	60	—	ns
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	ns

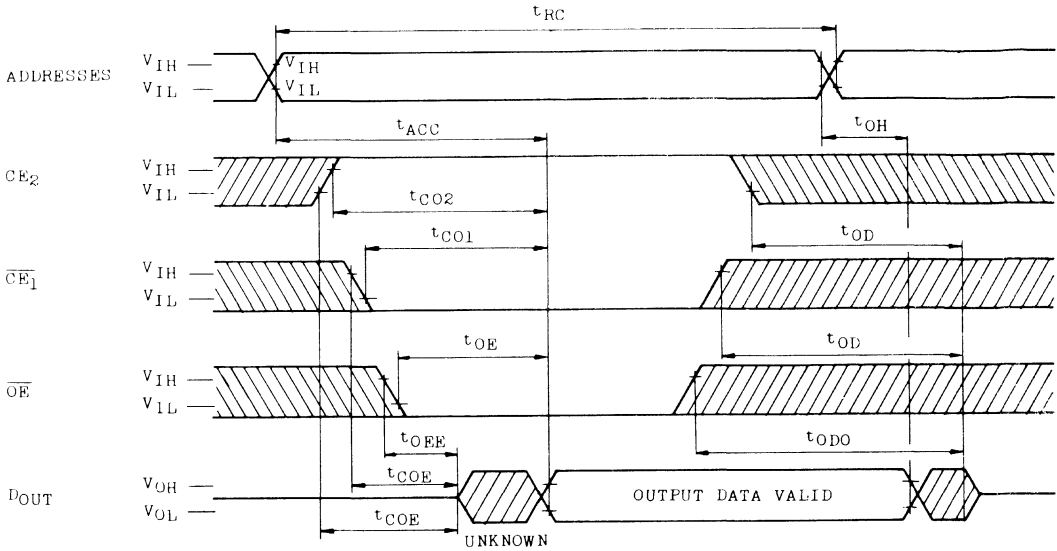
## A. C. TEST CONDITIONS

Output Load	: 100pF + 1 TTL Gate
Input Pulse Level	: 0.6V, 2.4V
Timing Measurement	V <sub>IN</sub> : 0.8V, 2.2V
Reference Level	V <sub>OUT</sub> : 0.8V, 2.2V
	: 5ns

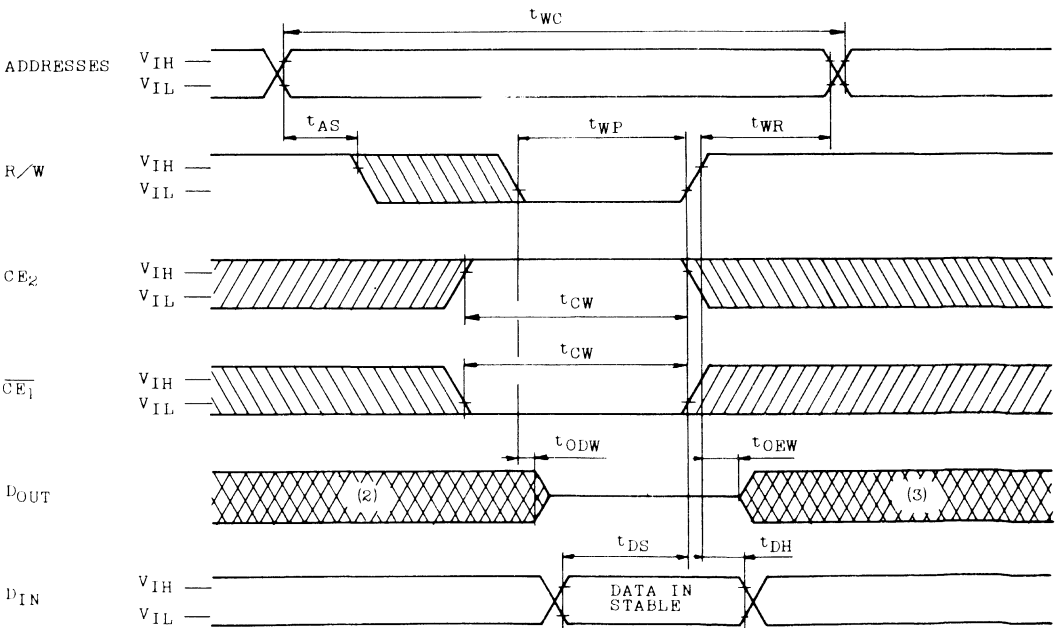
# TC5563APL-10, TC5563APL-12 TC5563APL-15

## TIMING WAVEFORMS

### ● READ CYCLE (1)

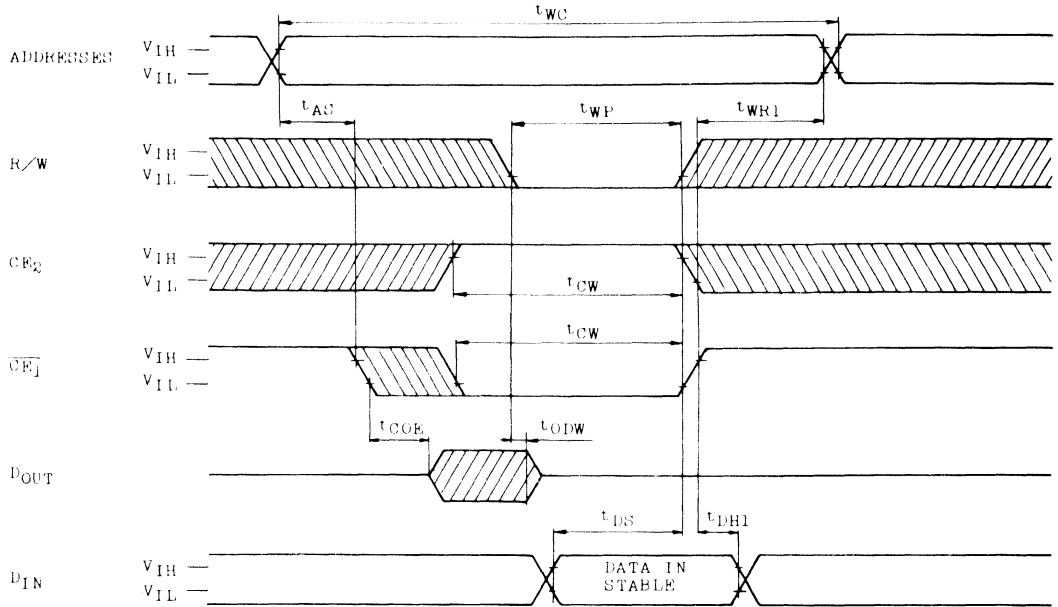


### ● WRITE CYCLE 1 (4) (R/W Controlled Write)

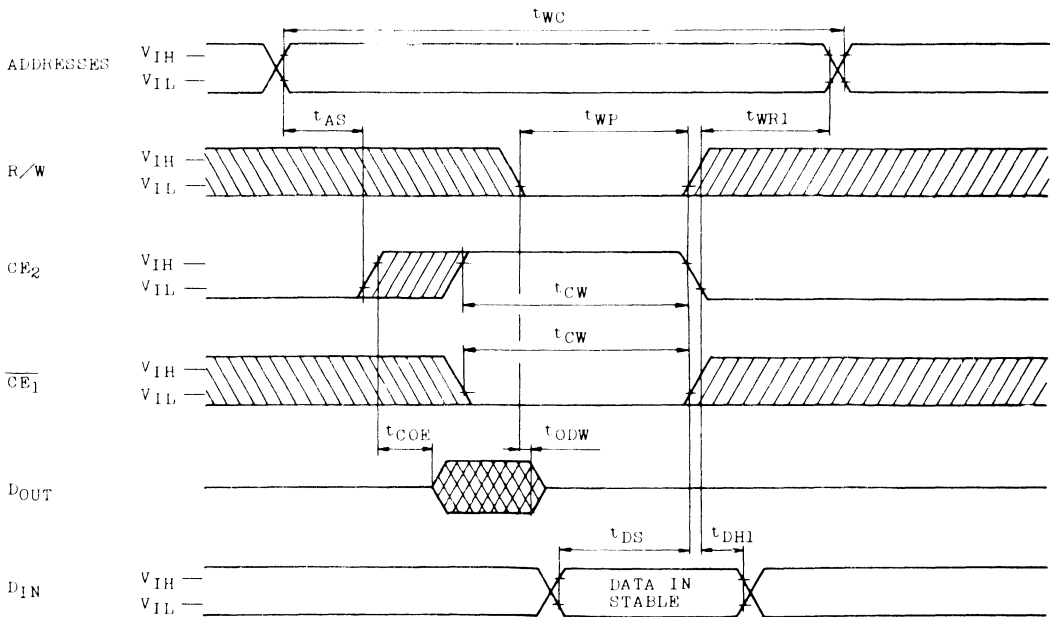


# TC5563APL-10, TC5563APL-12 TC5563APL-15

● WRITE CYCLE 2 (4) ( $\overline{CE1}$  Controlled Write)



● WRITE CYCLE 3 (4) ( $CE2$  Controlled Write)



# TC5563APL-10, TC5563APL-12 TC5563APL-15

Note :

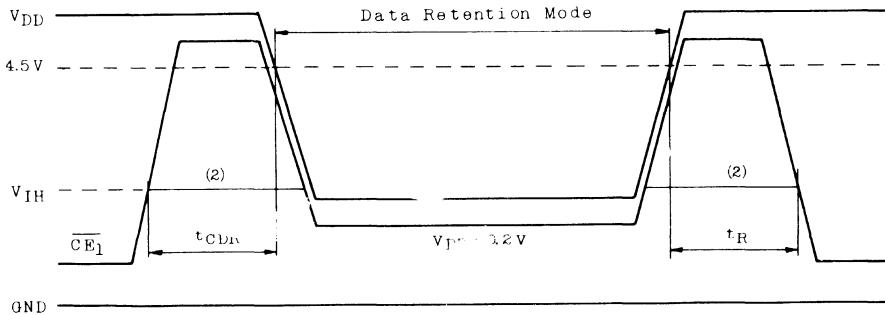
1. R/W is High for Read cycle,
2. Assuming that  $\overline{CE}_1$  low transition of  $CE_2$  High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that  $\overline{CE}_1$  High transition or  $CE_2$  Low transition occurs coincident with or prior to R/W High transition Outputs remain in a high impedance state.
4. Assuming that  $\overline{OE}$  is High for Write Cycle, Outputs are in high impedance state during this period

## DATA RETENTION CHARACTERISTICS (Ta=0-70°C)

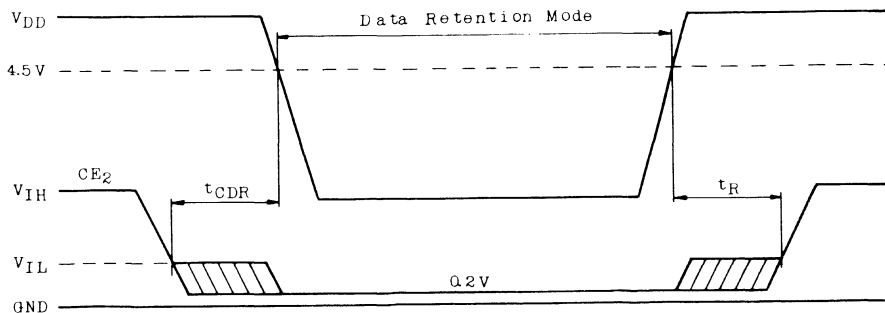
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{DH}$	Data Retention Supply Voltage	2.0	—	5.5	V
$I_{DDS2}$	Standby Supply Current	$V_{DD}=3.0V$	—	50	$\mu A$
		$V_{DD}=5.5V$	—	100	$\mu A$
$t_{CDR}$	Chip Deselection to Data Retention Mode	0	—	—	$\mu s$
$t_R$	Recovery Time	$t_{RC}^*$	—	—	ns

\* : Read cycle time.

### ● $\overline{CE}_1$ Controlled Data Retention Mode (1)



### ● $CE_2$ Controlled Data Retention Mode (3)



# TC5563APL-10, TC5563APL-12 TC5563APL-15

Note :

1. In  $\overline{CE}_1$  controlled data retention mode, minimum standby current mode is achieved under the condition of  $CE_2 \leq 0.2V$  or  $CE_2 \geq V_{DD} - 0.2V$ .
2. If the  $V_{IH}$  of  $\overline{CE}_1$  is 2.2V in operation,  $I_{DDSI}$  current flows during the period that the  $V_{DD}$  voltage is going down from 4.5V to 2.4V.
3. In  $CE_2$  controlled data retention mode, minimum standby current mode is achieved under the condition of  $CE_2 \leq 0.2V$ .

## DEVICE INFORMATION

The TC5563APL is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure.

This peak current may induce the noise on  $V_{DD}/GND$  lines. Thus the use of about  $0.1\mu F$  decoupling capacitor for every device is recommended to eliminate such noise.

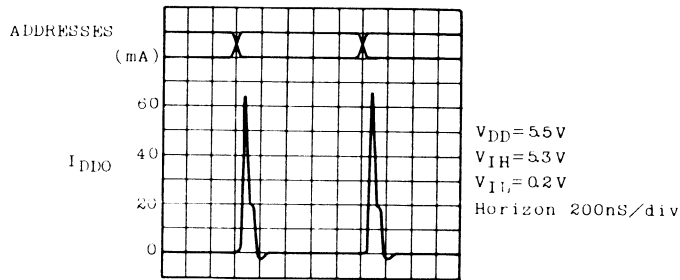
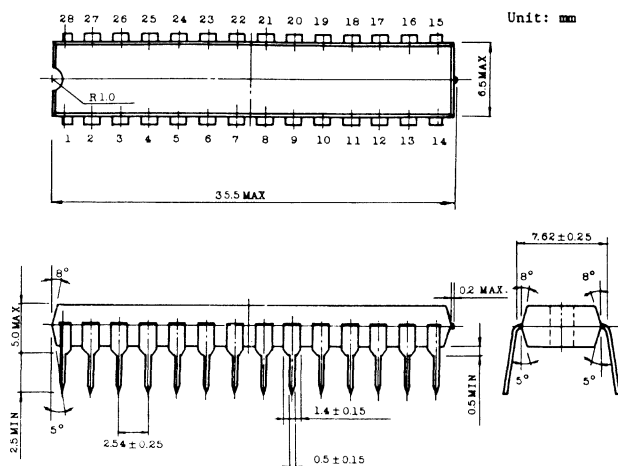


Fig. TYPICAL CURRENT WAVEFORMS

# TC5563APL-10, TC5563APL-12 TC5563APL-15

## OUTLINE DRAWINGS

### ● DIP 28 PIN OUTLINE DRAWING (6D28A-P)



Note : Lead pitch is 2.54 and tolerance is  $\pm 0.25$  against theoretical center of each lead that is obtained on the basis of No. 1 and No. 28 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described in circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.  
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# TOSHIBA MOS MEMORY PRODUCT

8,192 WORD × 8 BIT  
CMOS STATIC RAM  
SILICON GATE CMOS

TC5563APL-10L, TC5563APL-12L  
TC5563APL-15L

PRELIMINARY

## DESCRIPTION

The TC5563APL is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns. When CE<sub>2</sub> is a logical low or CE<sub>1</sub> is a logical high, the device is placed in low power standby mode in which standby current is 0.6μA typically. The TC5563APL has three control inputs. Two chip enables (CE<sub>1</sub>, CE<sub>2</sub>) allow for device selection and data retention control, and an output enable input (OE) provides fast memory

access. Thus the TC5563APL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC5563APL also features pin compatibility with the 64k bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.

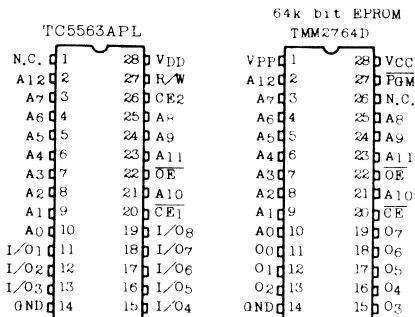
The TC5563APL is offered in a dual-in-line 28 pin 0.3 inch width plastic package.

## FEATURES

- Low Power Dissipation  
27.5mW/MHz (MAX.) Operating
- Standby Current : 1μA (Max.) Ta=25°C
- Access Time  
TC5563APL-10L : 100ns (Max.)  
TC5563APL-12L : 120ns (Max.)  
TC5563APL-15L : 150ns (Max.)

- 5V Single Power Supply
- Power Down Features : CE<sub>2</sub>, CE<sub>1</sub>
- Fully Static Operation
- Data Retention Supply Voltage : 2.0~5.5V
- Directly TTL Compatible  
: All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package Type)

## PIN CONNECTION (TOP VIEW)



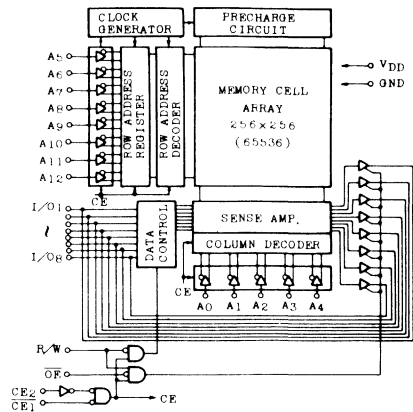
## PIN NAMES

A <sub>0</sub> ~A <sub>12</sub>	Address Inputs
R/W	Read/Write Control Input
OE	Output Enable Input
CE <sub>1</sub> , CE <sub>2</sub>	Chip Enable Inputs
I/O <sub>1</sub> ~I/O <sub>8</sub>	Data Input/Output
V <sub>DD</sub>	Power (+5V)
GND	Ground
N. C.	No Connection

Package Type	Device Name
600 mil DIP	*TC5565APL
300 mil DIP (Slim Package)	TC5563APL
Flat Package(SOP)	*TC5565AFL

\* : See TC5565APL/AFL Technical Data.

## BLOCK DIAGRAM



# TC5563APL-10L, TC5563APL-12L TC5563APL-15L

## OPERATION MODE

OPERATION MODE	CE <sub>1</sub>	CE <sub>2</sub>	OE	R/W	I/O <sub>1</sub> ~I/O <sub>8</sub>	POWER
Read	L	H	L	H	D <sub>OUT</sub>	I <sub>DD0</sub>
Write	L	H	*	L	D <sub>IN</sub>	I <sub>DD0</sub>
Output Deselect	L	H	H	H	High-Z	I <sub>DD0</sub>
Standby	H	*	*	*	High-Z	I <sub>DD5</sub>
	*	L	*	*	High-Z	I <sub>DD5</sub>

\* : H or L

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.3~7.0	V
V <sub>IN</sub>	Input Voltage	-0.3*~7.0	V
V <sub>I/O</sub>	Input and Output Voltage	-0.5~V <sub>DD</sub> +0.5	V
P <sub>D</sub>	Power Dissipation	0.8	W
T <sub>SOLDER</sub>	Soldering Temperature	260±10	°C·Sec
T <sub>STG</sub>	Storage Temperature	-55~150	°C
T <sub>OPR</sub>	Operating Temperature	0~70	°C

\* : -3.0V at Pulse width 50ns

## D. C RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3*	—	0.8	V
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	—	5.5	V

\* : -3.0V at Pulse width 50ns

# TC5563APL-10L, TC5563APL-12L TC5563APL-15L

## D. C and OPERATING CHARACTERISTICS (Ta=0~70°C, VDD=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> =0~V <sub>DD</sub>	—	—	±1.0	μA	
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> =2.4V	-1.0	—	—	mA	
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> =0.4V	4.0	—	—	mA	
I <sub>LO</sub>	Output Leakage Current	$\overline{CE}_1=V_{IH}$ or $CE_2=V_{IL}$ or R/W=V <sub>IL</sub> or $\overline{OE}=V_{IH}$ V <sub>OUT</sub> =0~V <sub>DD</sub>	—	—	±1.0	μA	
I <sub>DD01</sub>	operating Current	V <sub>DD</sub> =5.5V I <sub>out</sub> =0mA $\overline{CE}_1=V_{IL}$ CE <sub>2</sub> =V <sub>IH</sub> Other Input=V <sub>IH</sub> /V <sub>IL</sub>	t <sub>cycle</sub> =1μs	—	—	10	mA
			t <sub>cycle</sub> =Min. cycle	—	—	45	
I <sub>DD02</sub>	Operating Current	V <sub>DD</sub> =5.5V $\overline{CE}_1=0.2V$ CE <sub>2</sub> =V <sub>DD</sub> -0.2V Other Input I <sub>out</sub> =0mA =V <sub>DD</sub> -0.2V/0.2V	t <sub>cycle</sub> =1μs	—	—	5	mA
			t <sub>cycle</sub> =Min. cycle	—	—	40	
I <sub>DDs1</sub>	Standby Current	$\overline{CE}_1=V_{IH}$ or CE <sub>2</sub> =V <sub>IL</sub>	—	—	3	mA	
*I <sub>DDs2</sub>	Standby Current	$\overline{CE}_1=V_{DD}-0.2V$ or CE <sub>2</sub> =0.2V	Ta=25°C	—	0.6	1.0	μA
			Ta=0~70°C	—	—	30	

\* : In standby mode with  $\overline{CE}_1 \geq V_{DD} - 0.2V$ , these specification limits are guaranteed under the condition of CE<sub>2</sub> ≥ V<sub>DD</sub> - 0.2V or CE<sub>2</sub> ≤ 0.2V

## CAPACITANCE (Ta=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> =GND	10	pF

Note: This parameter periodically sampled is not 100% tested.

# TC5563APL-10L, TC5563APL-12L TC5563APL-15L

## A. C. CHARACTERISTICS (Ta=0~70°C, VDD=5V±10%)

### Read Cycle

SYMBOL	PARAMETER	TC5563APL-10L		TC5563APL-12L		TC5563APL-15L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	100	—	120	—	150	—	ns
t <sub>ACC</sub>	Address Access Time	—	100	—	120	—	150	
t <sub>CO1</sub>	CE1 Access Time	—	100	—	120	—	150	
t <sub>CO2</sub>	CE2 Access Time	—	100	—	120	—	150	
t <sub>OE</sub>	Output Enable to Output Valid	—	50	—	60	—	70	
t <sub>COF</sub>	Chip Enable (CE1, CE2) to Output in Low-Z	10	—	10	—	15	—	
t <sub>OEZ</sub>	Output Enable to Output in Low-Z	5	—	5	—	5	—	
t <sub>OD</sub>	Chip Enable (CE1, CE2) to Output in High-Z	—	35	—	40	—	50	
t <sub>ODO</sub>	Output Enable to Output in High-Z	—	35	—	40	—	50	
t <sub>OH</sub>	Output Data Hold Time	20	—	20	—	20	—	

### Write Cycle

SYMBOL	PARAMETER	TC5563APL-10L		TC5563APL-12L		TC5563APL-15L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	100	—	120	—	150	—	ns
t <sub>WP</sub>	Write Pulse Width	60	—	70	—	90	—	
t <sub>CW</sub>	Chip Selection to End of Write	80	—	85	—	100	—	
t <sub>AS</sub>	Address Set up Time	0	—	0	—	0	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	
t <sub>ODW</sub>	R/W to Output in High-Z	—	35	—	40	—	50	
t <sub>OEW</sub>	R/W to Output in Low-Z	5	—	5	—	10	—	
t <sub>DS</sub>	Data Set Up Time	40	—	50	—	60	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	

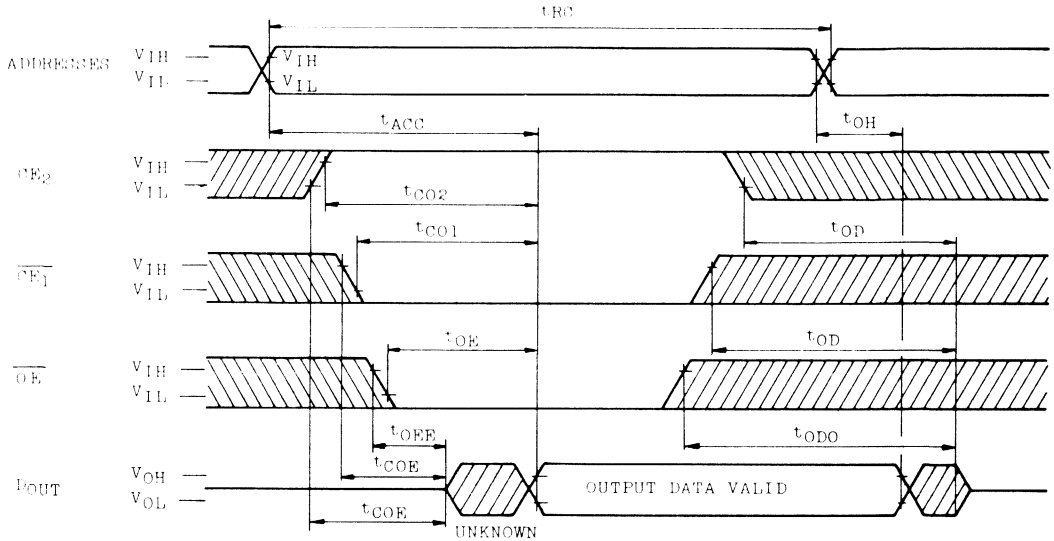
## A. C. TEST CONDITIONS

Output Load	: 100pF + 1 TTL Gate
Input Pulse Level	: 0.6V, 2.4V
Timing Measurement	V <sub>in</sub> : 0.8V, 2.2V
Reference Level	V <sub>out</sub> : 0.8V, 2.2V
t <sub>r</sub> , t <sub>f</sub>	: 5ns

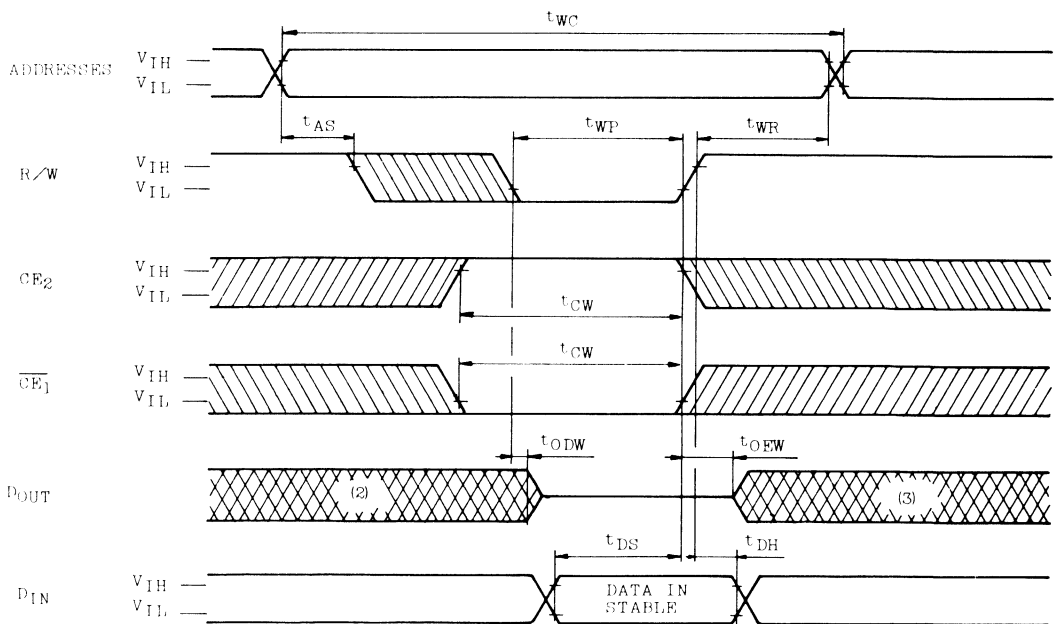
# TC5563APL-10L, TC5563APL-12L TC5563APL-15L

## TIMING WAVEFORMS

### ● READ CYCLE (1)

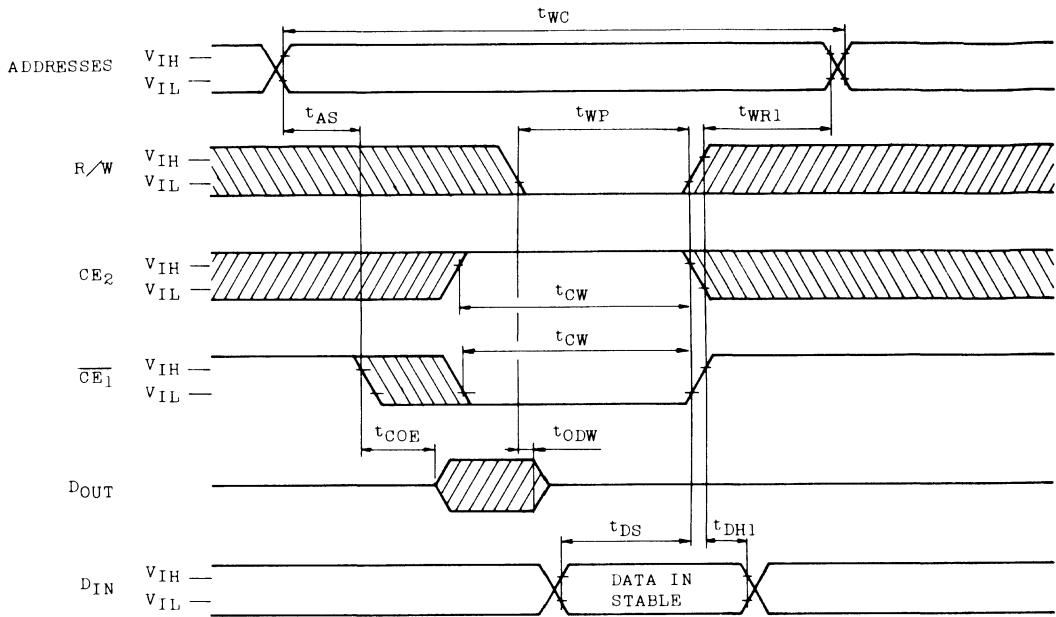


### ● WRITE CYCLE 1 (4) (R/W Controlled Write)

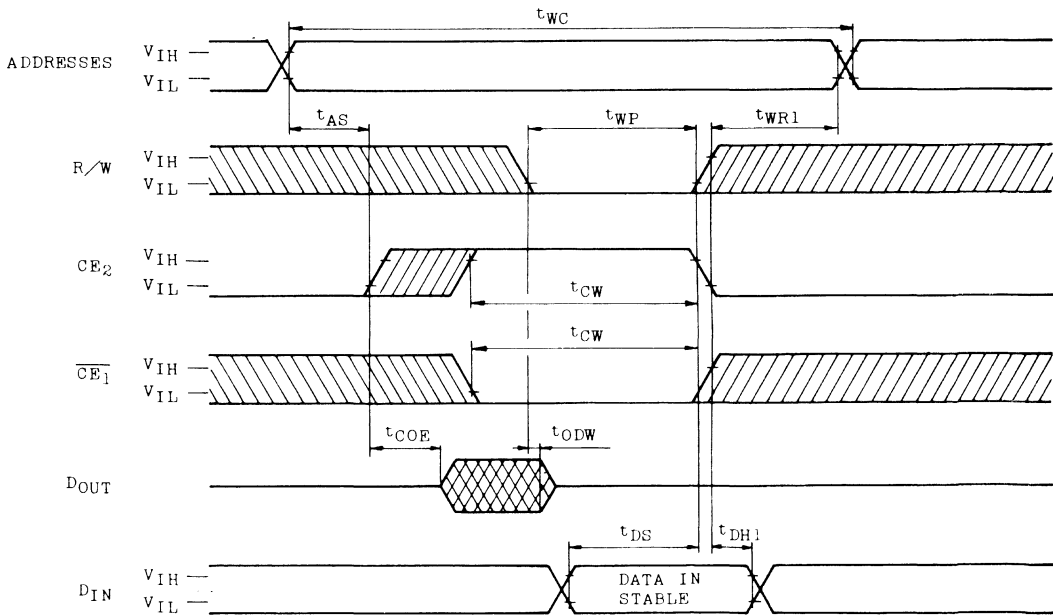


# TC5563APL-10L, TC5563APL-12L TC5563APL-15L

## ● WRITE CYCLE 2 (4) ( $\overline{CE}_1$ Controlled Write)



## ● WRITE CYCLE 3 (4) ( $CE_2$ Controlled Write)



# TC5563APL-10L, TC5563APL-12 TC5563APL-15L

Note :

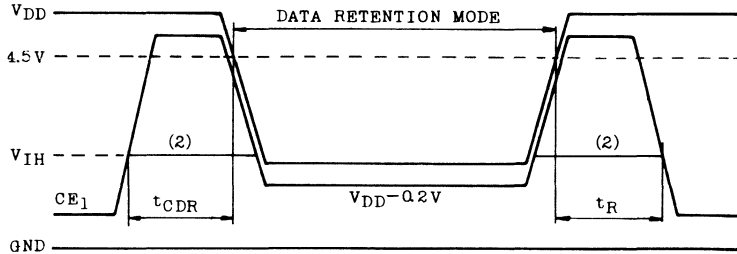
1. R/W is High for Read Cycle.
2. Assuming that  $\overline{CE}_1$  Low transition of  $CE_2$  High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that  $\overline{CE}_1$  High transition or  $CE_2$  Low transition occurs coincident with or prior to R/W High transition, Outputs remain in a high impedance state.
4. Assuming that  $\overline{OE}$  is High for Write Cycle, Outputs are in high impedance state during this period.

## DATA RETENTION CHARACTERISTICS (Ta=0~70°C)

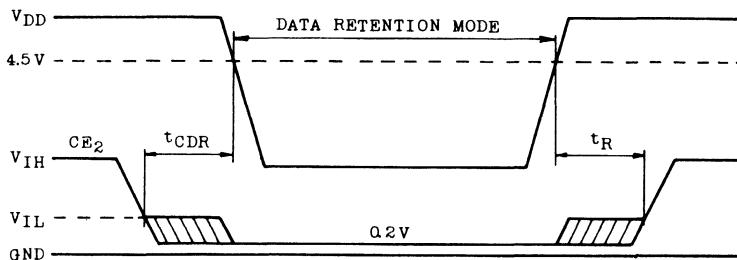
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{DH}$	Data Retention Supply Voltage	2.0	—	5.5	V
$I_{DDS2}$	Stand by Supply Current	$V_{DD}=3.0V$	—	15	$\mu A$
		$V_{DD}=5.5V$	—	30	
$t_{CDR}$	Chip Deselection to Data Retention Mode	0	—	—	$\mu s$
$t_R$	Recovery Time	$t_{RC}^*$	—	—	ns

\* : Read cycle time.

### ● $\overline{CE}_1$ Controlled Data Retention Mode (1)



### ● $CE_2$ Controlled Data Retention Mode (3)



# TC5563APL-10L, TC5563APL-12L TC5563APL-15L

Note :

1. In  $\overline{CE}_1$  controlled data retention mode, minimum standby current mode is achieved under the condition of  $CE_2 \leq 0.2V$  or  $CE_2 \geq V_{DD} - 0.2V$ .
2. If the  $V_{IH}$  of  $\overline{CE}_1$  is 2.2V in operation,  $I_{DD1}$  current flows during the period that the  $V_{DD}$  voltage is going down from 4.5V to 2.4V.
3. In  $CE_2$  controlled data retention mode, minimum standby current mode is achieved under the condition of  $CE_2 \leq 0.2V$ .

## DEVICE INFORMATION

The TC5563APL/F is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure. This peak current may induce the noise on  $V_{DD}/GND$  lines. Thus the use of about 0.1  $\mu F$  decoupling capacitor for every device is recommended to eliminate such noise.

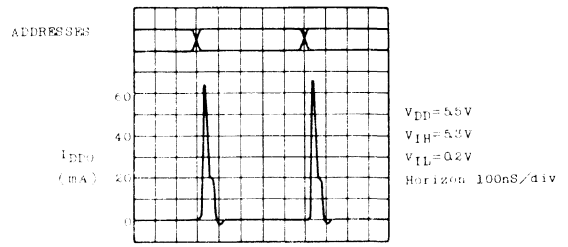
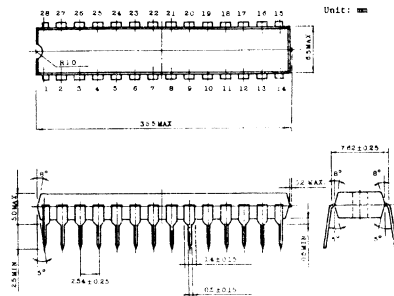


Fig. 1. TYPICAL CURRENT WAVEFORMS

### ● DIP 28 PIN OUTLINE DRAWING (6D28A-P)



Note : Lead pitch is 2.54 and tolerance is  $\pm 0.25$  against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.  
C. May, 1986 Toshiba Corporation



# TOSHIBA MOS MEMORY PRODUCT

**TC5565APL-10, TC5565APL-12, TC5565APL-15**  
**TC5565AFL-10, TC5565AFL-12, TC5565AFL-15**

## DESCRIPTION

The TC5565APL/AFL is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns. When CE2 is a logical low or CE1 is a logical high, the device is placed in low power standby mode in which standby current is 2µA typically. The TC5565APL/AFL has three control inputs. Two chip enable (CE1, CE2) allow for device selection and data retention control, and an output enable input (OE) provides fast memory access. Thus the TC5565APL/AFL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. The TC5565APL also features pin compatibility with the 64k bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems. The TC5565APL is offered in a dual-in-line 28 pin standard plastic package. The TC5565AFL is offered in 28 pin mini Flat Package.

## FEATURES

- Low Power Dissipation  
27.5mW/MHz(Max.) Operating
- Standby Current : 100µA(Max.) Ta=70°C
- Access Time  
TC5565APL/AFL-10 : 100ns(Max.)  
TC5565APL/AFL-12 : 120ns(Max.)  
TC5565APL/AFL-15 : 150ns(Max.)
- 5V Single Power Supply
- Power Down Features: CE2, CE1
- Fully Static Operation
- Data Retention Supply Voltage: 2.0~5.5V

- Directly TTL Compatible  
: All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package Type)

Package Type	Device Name
600 mil DIP	TC5565APL
300 mil DIP (Slim Package)	*TC5563APL
Flat Package (SOP)	TC5565AFL

\*) See TC5563APL Technical Data.

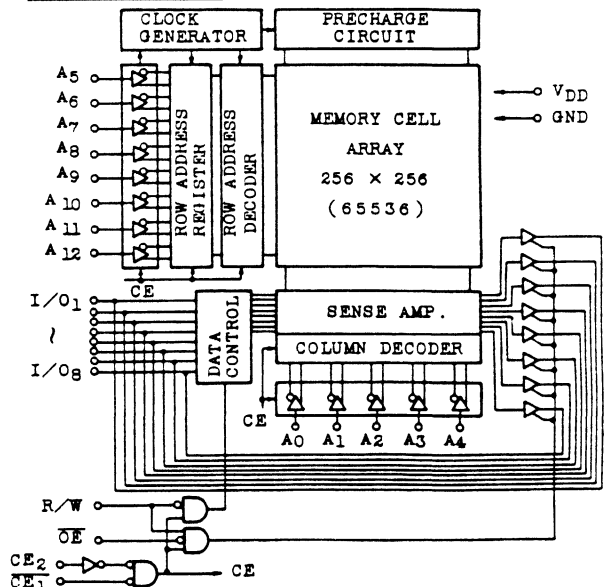
## PIN CONNECTION (TOP VIEW)

TC5565APL, AFL				64k bit EPROM TMM2764D			
N.C.	1	28	VDD	VPP	1	28	VCC
A12	2	27	R/W	A12	2	27	PGM
A7	3	26	CE2	A7	3	26	N.C.
A6	4	25	A8	A6	4	25	A8
A5	5	24	A9	A5	5	24	A9
A4	6	23	A11	A4	6	23	A11
A3	7	22	OE	A3	7	22	OE
A2	8	21	A10	A2	8	21	A10
A1	9	20	CE1	A1	9	20	CE
A0	10	19	I/O8	A0	10	19	O7
I/O1	11	18	I/O7	O0	11	18	O6
I/O2	12	17	I/O6	O1	12	17	O5
I/O3	13	16	I/O5	O2	13	16	O4
GND	14	15	I/O4	GND	14	15	O3

## PIN NAMES

A0~A12	Address Inputs
R/W	Read/Write Control Input
OE	Output Enable Input
CE1, CE2	Chip Enable Inputs
I/O1~I/O8	Data Input/Output
VDD	Power (+5V)
GND	Ground
N.C.	No Connection

## BLOCK DIAGRAM



**TC5565APL-10, TC5565APL-12, TC5565APL-15**  
**TC5565AFL-10, TC5565AFL-12, TC5565AFL-15**

OPERATION MODE

OPERATION MODE	$\overline{CE}1$	CE2	$\overline{OE}$	R/W	I/O1-I/O8	POWER
Read	L	H	L	H	DOUT	I <sub>DDO</sub>
Write	L	H	*	L	DIN	I <sub>DDO</sub>
Output Deselect	L	H	H	H	High-Z	I <sub>DDO</sub>
Standby	H	*	*	*	High-Z	I <sub>DDS</sub>
	*	L	*	*	High-Z	I <sub>DDS</sub>

\* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.3~7.0	V
V <sub>IN</sub>	Input Voltage	*-0.3~7.0	V
V <sub>I/O</sub>	Input and Output Voltage	-0.5-V <sub>DD</sub> +0.5	V
P <sub>D</sub>	Power Dissipation	1.0/0.6**	W
T <sub>solder</sub>	Soldering Temperature	260±10	°C·sec
T <sub>stg</sub>	Storage Temperature	-55~150	°C
T <sub>opr</sub>	Operating Temperature	0~70	°C

\* -3.0V at pulse width 50ns MAX.      \*\* Flat package

D.C RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	-	0.8	V
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	-	5.5	V

**TC5565APL-10, TC5565APL-12, TC5565APL-15**  
**TC5565AFL-10, TC5565AFL-12, TC5565AFL-15**

D.C and OPERATING CHARACTERISTICS (Ta=0~70°C, VDD=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
IIL	Input Leakage Current	VIN=0~VDD	-	-	±1.0	μA		
IOH	Output High Current	VOH=2.4V	-1.0	-	-	mA		
IOL	Output Low Current	VOL=0.4V	4.0	-	-	mA		
ILO	Output Leakage Current	CE1=VIH or CE2=VOL or R/W=VIL or OE=VIH VOUT=0~VDD	-	-	±1.0	μA		
IDDO1	Operating Current	VDD=5.5V CE1=VIL CE2=VIH Other input= VIH/VIL	tcycle=1.0μs		-	-	10	mA
			TC5565APL-10	tcycle=100ns	-	-	45	mA
			TC5565APL-12	tcycle=120ns	-	-	40	mA
			TC5565APL-15	tcycle=150ns	-	-	35	mA
IDDO2	Operating Current	VDD=5.5V CE1=0.2V CE2=VDD-0.2V Other input= VDD-0.2V/0.2V	tcycle=1.0μs		-	-	5	mA
			TC5565APL-10	tcycle=100ns	-	-	40	mA
			TC5565APL-12	tcycle=120ns	-	-	35	mA
			TC5565APL-15	tcycle=150ns	-	-	30	mA
IDDS1	Standby Current	CE1=VIH or CE2=VIL	-	-	3	mA		
*IDDS2		CE1=VDD-0.2V or CE2=0.2V	VDD=5.5V	-	2	100	μA	
			VDD=3.0V	-	1	50	μA	

Note \* : In standby mode with CE1 ≥ VDD-0.2V, these specification limits are guaranteed under the condition of CE2 ≥ VDD-0.2V or CE2 ≤ 0.2V.

CAPACITANCE (Ta=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CIN	Input Capacitance	VIN=GND	-	-	10	pF
COUT	Output Capacitance	VOUT=GND	-	-	10	pF

Note : This parameter periodically sampled is not 100% tested.

**TC5565APL-10, TC5565APL-12, TC5565APL-15**  
**TC5565AFL-10, TC5565AFL-12, TC5565AFL-15**

A.C. CHARACTERISTICS ( $T_a=0\sim70^\circ\text{C}$ ,  $V_{DD}=5\text{V}\pm 10\%$ )

Read Cycle

SYMBOL	PARAMETER	TC5565APL-10 TC5565AFL-10		TC5565APL-12 TC5565AFL-12		TC5565APL-15 TC5565AFL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{RC}$	Read Cycle Time	100	-	120	-	150	-	ns
$t_{ACC}$	Address Access Time	-	100	-	120	-	150	ns
$t_{CO1}$	$\overline{CE1}$ Access Time	-	100	-	120	-	150	ns
$t_{CO2}$	$CE2$ Access Time	-	100	-	120	-	150	ns
$t_{OE}$	Output Enable to Output Valid	-	50	-	60	-	70	ns
$t_{COE}$	Chip Enable ( $\overline{CE1}$ , $CE2$ ) to Output in Low-Z	10	-	10	-	15	-	ns
$t_{OEE}$	Output Enable to Output in Low-Z	5	-	5	-	5	-	ns
$t_{OD}$	Chip Enable ( $\overline{CE1}$ , $CE2$ ) to Output in High-Z	-	35	-	40	-	50	ns
$t_{ODO}$	Output Enable to Output in High-Z	-	35	-	40	-	50	ns
$t_{OH}$	Output Data Hold Time	20	-	20	-	20	-	ns

Write Cycle

SYMBOL	PARAMETER	TC5565APL-10 TC5565AFL-10		TC5565APL-12 TC5565AFL-12		TC5565APL-15 TC5565AFL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{WC}$	Write Cycle Time	100	-	120	-	150	-	ns
$t_{WP}$	Write Pulse Width	60	-	70	-	90	-	ns
$t_{CW}$	Chip Selection to End of Write	80	-	85	-	100	-	ns
$t_{AS}$	Address Set up Time	0	-	0	-	0	-	ns
$t_{WR}$	Write Recovery Time	0	-	0	-	0	-	ns
$t_{ODW}$	R/W to Output High-Z	-	35	0	40	-	50	ns
$t_{OEW}$	R/W to Output Low-Z	5	-	5	-	10	-	ns
$t_{DS}$	Data Set up Time	40	-	50	-	60	-	ns
$t_{DH}$	Data Hold Time	0	-	0	-	0	-	ns

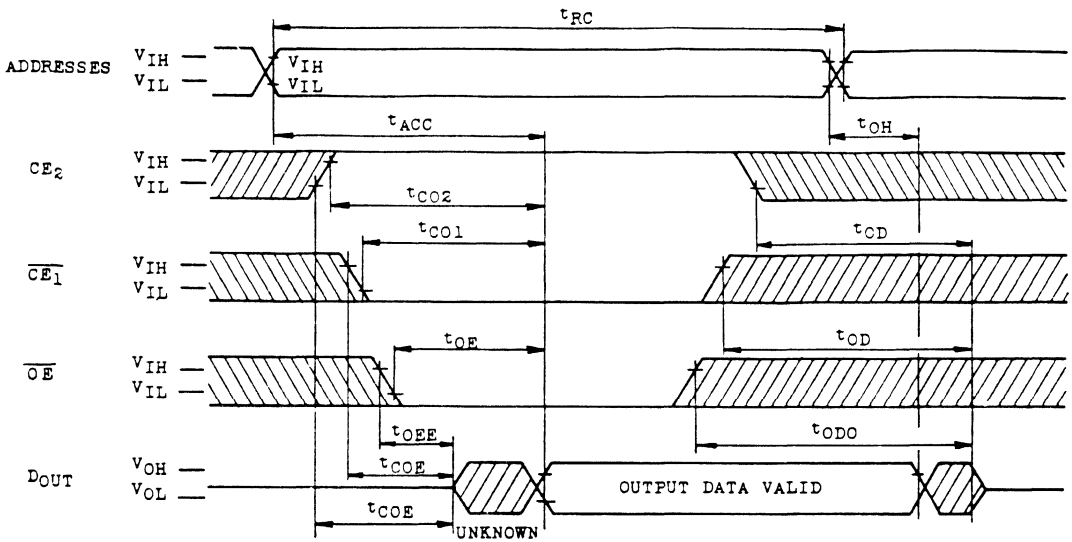
A.C. TEST CONDITION

Output Load : 100pF + 1 TTL Gate  
 Input Pulse Level : 0.6V, 2.4V  
 Timing Measurement  $V_{IN}$  : 0.8V, 2.2V  
 Reference Level  $V_{OUT}$  : 0.8V, 2.2V  
 $t_r$ ,  $t_f$  : 5ns

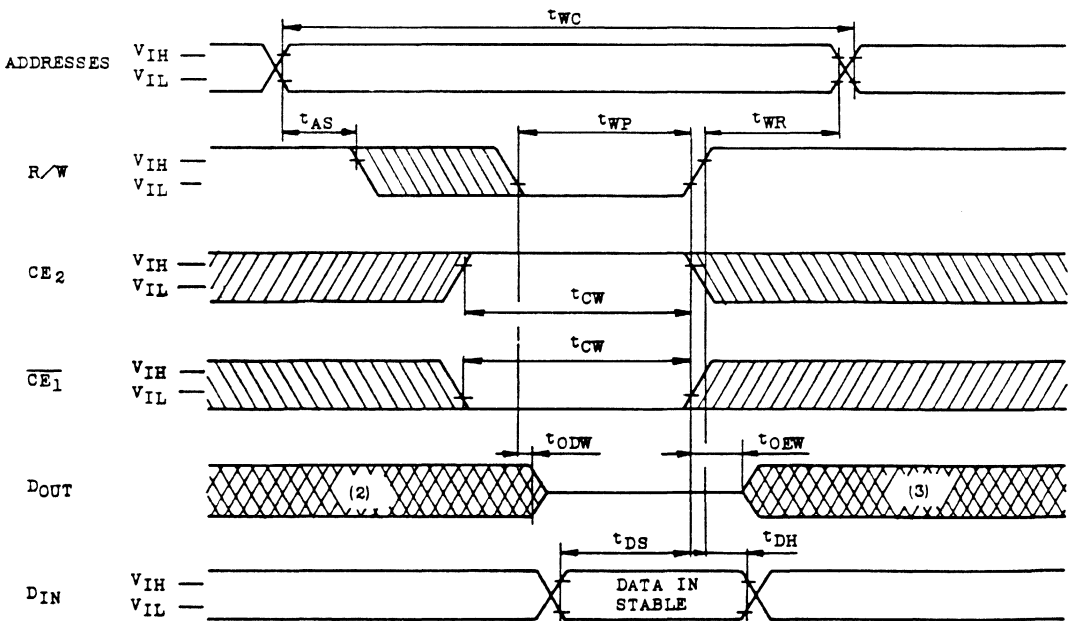
**TC5565APL-10, TC5565APL-12, TC5565APL-15  
TC5565AFL-10, TC5565AFL-12, TC5565AFL-15**

TIMING WAVEFORMS

READ CYCLE (1)

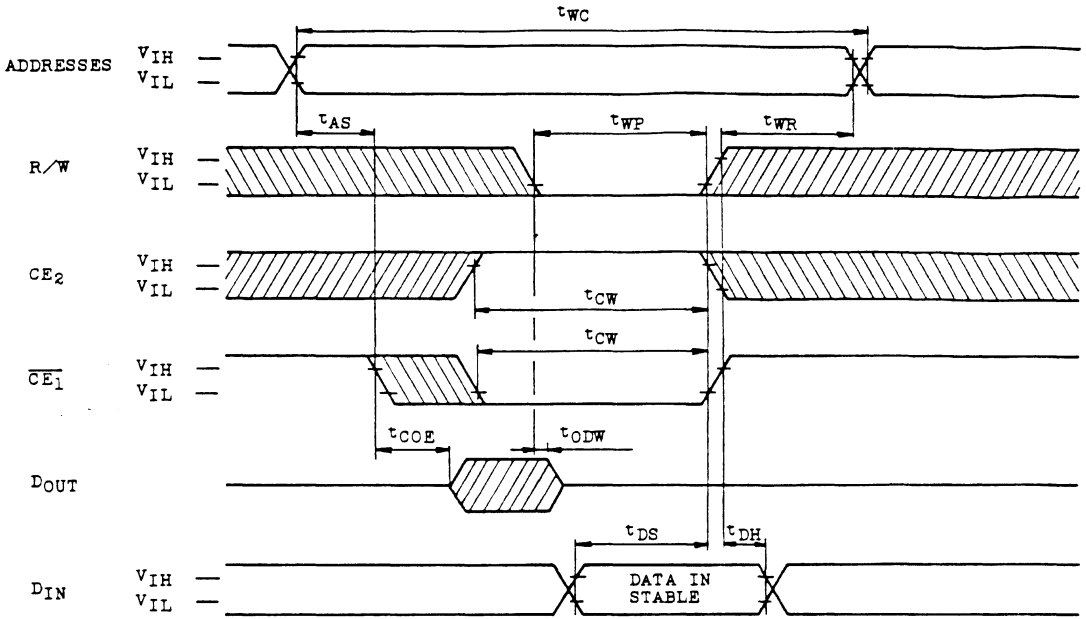


WRITE CYCLE 1 (4) (R/W Controlled Write)

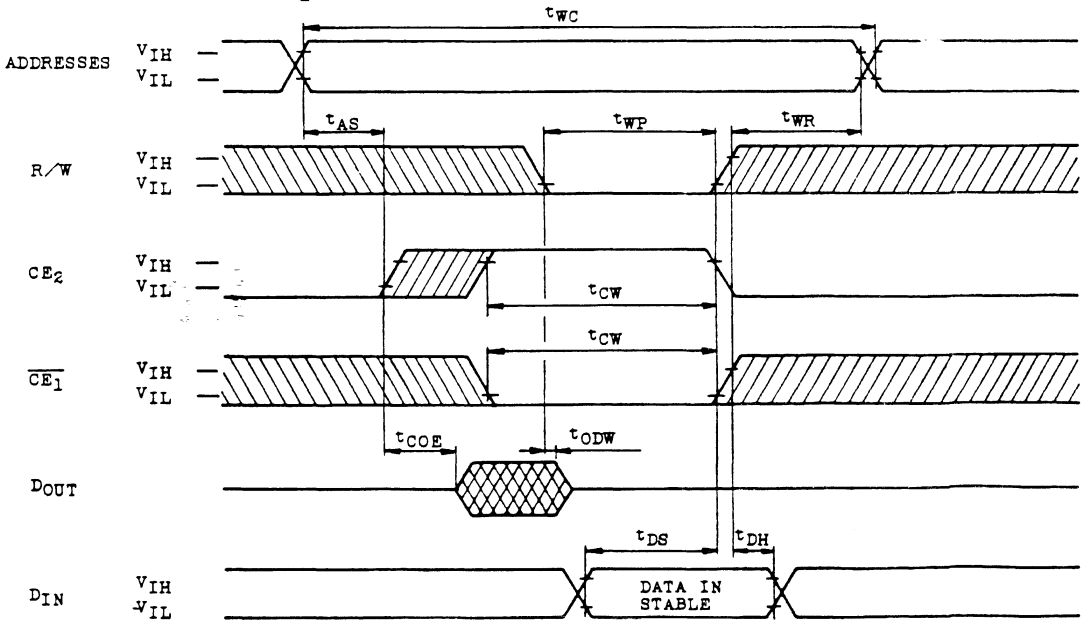


**TC5565APL-10, TC5565APL-12, TC5565APL-15**  
**TC5565AFL-10, TC5565AFL-12, TC5565AFL-15**

WRITE CYCLE 2 (4) ( $\overline{CE_1}$  Controlled Write)



WRITE CYCLE 3 (4) ( $CE_2$  Controlled Write)



**TC5565APL-10, TC5565APL-12, TC5565APL-15**  
**TC5565AFL-10, TC5565AFL-12, TC5565AFL-15**

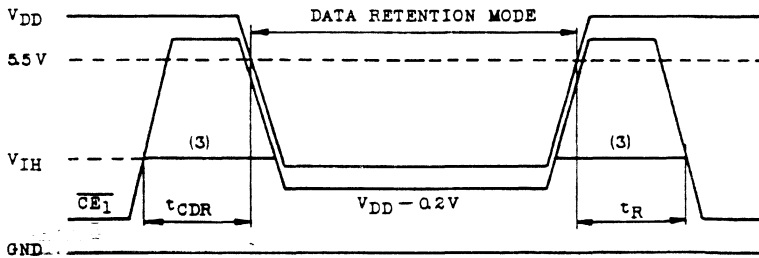
- Note 1. R/W is High for Read Cycle.
2. Assuming that  $\overline{CE}_1$  Low transition or  $\overline{CE}_2$  High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
  3. Assuming that  $\overline{CE}_1$  High transition or  $\overline{CE}_2$  Low transition occur coincident with or prior to R/W High transition, Outputs remain in a high impedance state.
  4. Assuming that  $\overline{OE}$  is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS ( $T_a=0-70^\circ\text{C}$ )

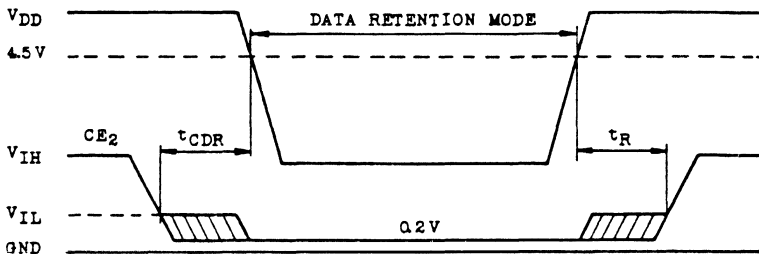
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{DH}$	Data Retention Supply Voltage	2.0	-	5.5	V
$I_{DD2}$	Stand by Supply Current	$V_{DD}=3.0\text{V}$	-	50	$\mu\text{A}$
		$V_{DD}=5.5\text{V}$	-	100	
$t_{CDR}$	Chip Deselection to Data Retention Mode	0	-	-	$\mu\text{s}$
$t_R$	Recovery Time	$t_{RC}(1)$	-	-	$\mu\text{s}$

Note (1) : Read cycle time.

$\overline{CE}_1$  Controlled Data Retention Mode (2)



$\overline{CE}_2$  Controlled Data Retention Mode (4)



**TC5565APL-10, TC5565APL-12, TC5565APL-15**  
**TC5565AFL-10, TC5565AFL-12, TC5565AFL-15**

- Note 2 : In  $\overline{CE}_1$  controlled data retention mode, minimum standby current mode is achieved under the condition of  $CE_2 \leq 0.2V$  or  $CE_2 \geq V_{DD} - 0.2V$ .
- 3 : If the  $V_{IH}$  of  $\overline{CE}_1$  is 2.2V in operation,  $I_{DDS1}$  current flows during the period that the  $V_{DD}$  voltage is going down from 4.5V to 2.4V.
- 4 : In  $CE_2$  controlled data retention mode, minimum standby current mode is achieved under the condition of  $CE_2 \leq 0.2V$ .

DEVICE INFORMATION

The TC5565APL/AFL is an synchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure.

This peak current may induce the noise on  $V_{DD}/GND$  lines. Thus the use of about 0.1 $\mu$ F decoupling capacitor for every device is recommended to eliminate such noise.

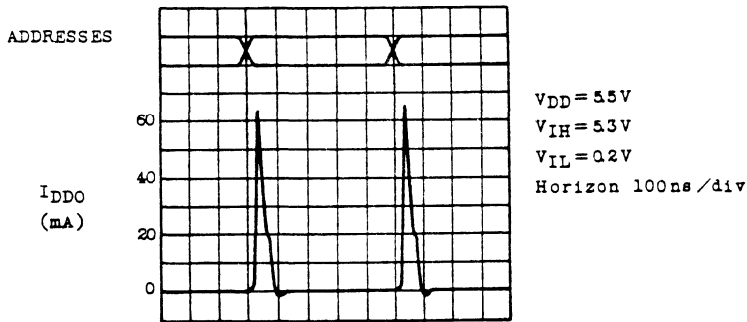


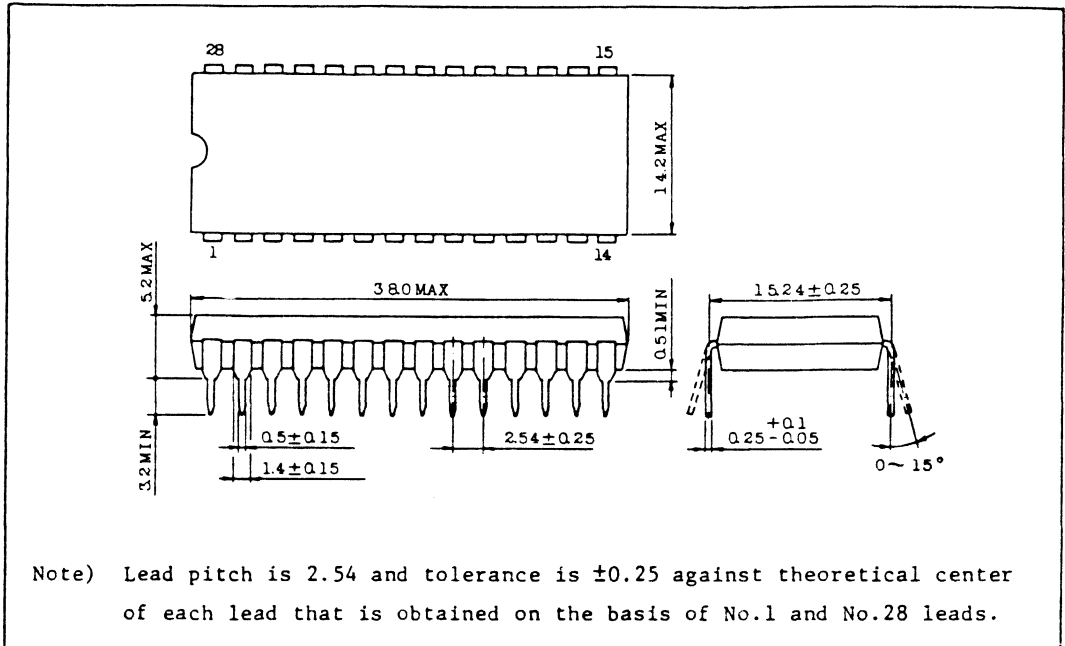
Fig. TYPICAL CURRENT WAVEFORMS



**TC5565APL-10, TC5565APL-12, TC5565APL-15**  
**TC5565AFL-10, TC5565AFL-12, TC5565AFL-15**

DIP 28 PIN OUTLINE DRAWING (6D28A-P)

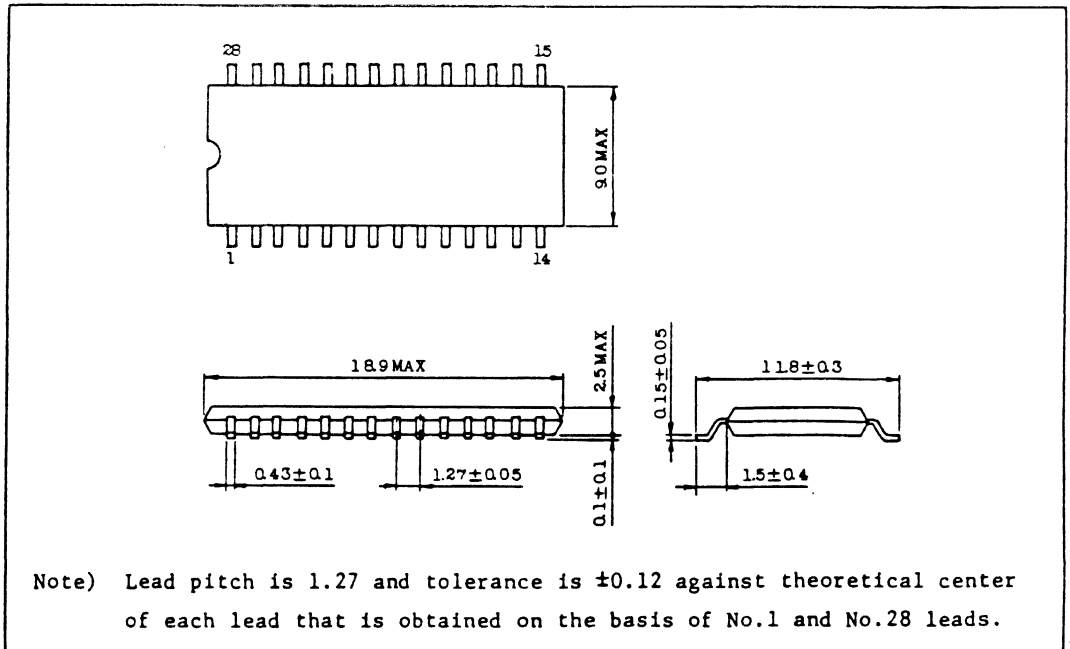
Unit in mm



Note) Lead pitch is 2.54 and tolerance is  $\pm 0.25$  against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

MFP 28 PIN OUTLINE DRAWING (F28GC-P)

Unit in mm



Note) Lead pitch is 1.27 and tolerance is  $\pm 0.12$  against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.



# TOSHIBA MOS MEMORY PRODUCT

8,192 WORD × 8 BIT  
CMOS STATIC RAM  
SILICON GATE CMOS

TC5565APL-10L, TC5565APL-12L, TC5565APL-15L  
TC5565AFL-10L, TC5565AFL-12L, TC5565AFL-15L

## DESCRIPTION

The TC5565APL/AFL is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns. When CE<sub>2</sub> is a logical low or  $\overline{CE}_1$  is a logical high, the device is placed in low power standby mode in which standby current is 0.6μA typically. The TC5565APL/AFL has three control inputs. Two chip enables ( $\overline{CE}_1$ , CE<sub>2</sub>) allow for device selection and data retention control, and an output enable ( $\overline{OE}$ ) provides fast mem-

ory access. Thus the TC5565APL/AFL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC5565APL/AFL also features pin compatibility with the 64k bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.

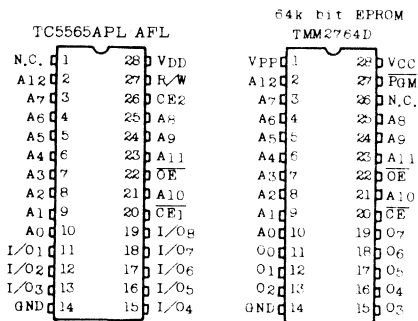
The TC5565APL/AFL is offered in a dual-in-line 28 pin standard plastic package.

## FEATURES

- Low Power Dissipation  
27.5mW/MHz (MAX.) Operating
- Standby Current : 1μA (MAX.) Ta = 25°C
- Access Time  
TC5565APL/AFL-10L : 100ns (MAX.)  
TC5565APL/AFL-12L : 120ns (MAX.)  
TC5565APL/AFL-15L : 150ns (MAX.)

- 5V Single Power Supply
- Power Down Features : CE<sub>2</sub>,  $\overline{CE}_1$
- Fully Static Operation
- Data Retention Supply Voltage : 2.0~5.5V
- Directly TTL Compatible  
: All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package Type)

## PIN CONNECTION (TOP VIEW)



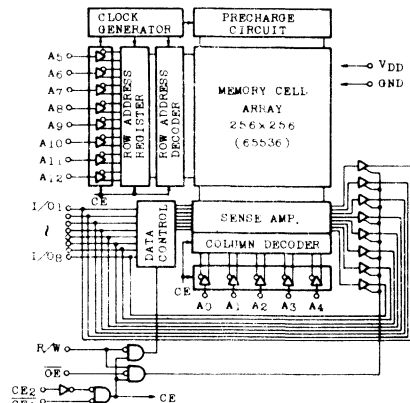
## NAMES

A <sub>0</sub> ~A <sub>12</sub>	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
CE <sub>1</sub> , CE <sub>2</sub>	Chip Enable Inputs
I/O <sub>1</sub> ~I/O <sub>8</sub>	Data Input/Output
V <sub>DD</sub>	Power (+5V)
GND	Ground
N. C.	No Connection

Package Type	Device Name
600 mil DIP	TC5565APL
300 mil DIP (Slim Package)	*TC5563APL
Flat Package(SOP)	TC5565AFL

\* : See TC5563APL Technical Data.

## BLOCK DIAGRAM



# TC5565APL-10L, TC5565APL-12L, TC5565APL-15L TC5565AFL-10L, TC5565AFL-12L, TC5565AFL-15L

## OPERATION MODE

OPERATION MODE	$\overline{CE}_1$	$CE_2$	$\overline{OE}$	R/W	I/O <sub>1</sub> ~I/O <sub>8</sub>	POWER
Read	L	H	L	H	D <sub>OUT</sub>	I <sub>DDO</sub>
Write	L	H	*	L	D <sub>IN</sub>	I <sub>DDO</sub>
Output Deselect	L	H	H	H	High-Z	I <sub>DDO</sub>
Standby	H	*	*	*	High-Z	I <sub>DDs</sub>
	*	L	*	*	High-Z	I <sub>DDs</sub>

\* : H or L

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.3~7.0	V
V <sub>IN</sub>	Input Voltage	-0.3*~7.0	V
V <sub>I/O</sub>	Input and Output Voltage	-0.5~V <sub>DD</sub> +0.5	V
P <sub>D</sub>	Power Dissipation	1.0/0.6**	W
T <sub>SOLDER</sub>	Soldering Temperature	260•10	°C•Sec
T <sub>STG</sub>	Storage Temperature	-55~150	°C
T <sub>OPR</sub>	Operating Temperature	0~70	°C

\* : -3.0V at Pulse width 50ns

\*\* : Flat package

## D. C RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3*	—	0.8	V
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	—	5.5	V

\* : -3.0V at Pulse width 50ns

# TC5565APL-10L, TC5565APL-12L, TC5565APL-15L TC5565AFL-10L, TC5565AFL-12L, TC5565AFL-15L

## D. C and OPERATING CHARACTERISTICS (Ta=0~70°C, VDD=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0~V <sub>DD</sub>	—	—	±1.0	μA	
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4V	-1.0	—	—	mA	
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4V	4.0	—	—	mA	
I <sub>LO</sub>	Output Leakage Current	$\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IL}$ or R/W = V <sub>IL</sub> or $\overline{OE} = V_{IH}$ V <sub>OUT</sub> = 0~V <sub>DD</sub>	—	—	±1.0	μA	
I <sub>DD01</sub>	operating Current	V <sub>DD</sub> = 5.5V I <sub>out</sub> = 0mA $\overline{CE}_1 = V_{IL}$ CE <sub>2</sub> = V <sub>IH</sub> Other Input = V <sub>IH</sub> /V <sub>IL</sub>	t <sub>cycle</sub> = 1μs	—	—	10	mA
			t <sub>cycle</sub> = Min. cycle	—	—	45	
I <sub>DD02</sub>	Operating Current	V <sub>DD</sub> = 5.5V $\overline{CE}_1 = 0.2V$ CE <sub>2</sub> = V <sub>DD</sub> - 0.2V Other Input I <sub>out</sub> = 0mA = V <sub>DD</sub> - 0.2V/0.2V	t <sub>cycle</sub> = 1μs	—	—	5	mA
			t <sub>cycle</sub> = Min. cycle	—	—	40	
I <sub>DD01</sub>	Standby Current	$\overline{CE}_1 = V_{IH}$ or CE <sub>2</sub> = V <sub>IL</sub>	—	—	3	mA	
*I <sub>DD02</sub>	Standby Current	CE <sub>1</sub> = V <sub>DD</sub> - 0.2V or CE <sub>2</sub> = 0.2V	Ta = 25°C	—	0.6	1.0	μA
			Ta = 0~70°C	—	—	30	

\* : In standby mode with  $\overline{CE}_1 \geq V_{DD} - 0.2V$ , these specification limits are guaranteed under the condition of CE<sub>2</sub> ≥ V<sub>DD</sub> - 0.2V or CE<sub>2</sub> ≤ 0.2V.

## CAPACITANCE (Ta = 25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = GND	10	pF

Note : This parameter periodically sampled is not 100% tested.

# TC5565APL-10L, TC5565APL-12L, TC5565APL-15L TC5565AFL-10L, TC5565AFL-12L, TC5565AFL-15L

## A. C. CHARACTERISTICS (Ta=0~70°C, VDD=5V±10%)

### Read Cycle

SYMBOL	PARAMETER	TC5565APL-10L TC5565AFL-10L		TC5565APL-12L TC5565AFL-12L		TC5565APL-15L TC5565AFL-15L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	100	—	120	—	150	—	ns
t <sub>ACC</sub>	Address Access Time	—	100	—	120	—	150	
t <sub>CO1</sub>	CE1 Access Time	—	100	—	120	—	150	
t <sub>CO2</sub>	CE2 Access Time	—	100	—	120	—	150	
t <sub>OE</sub>	Output Enable to Output Valid	—	50	—	60	—	70	
t <sub>COE</sub>	Chip Enable (CE1, CE2) to Output in Low-Z	10	—	10	—	15	—	
t <sub>OEE</sub>	Output Enable to Output in Low-Z	5	—	5	—	5	—	
t <sub>OD</sub>	Chip Enable (CE1, CE2) to Output in High-Z	—	35	—	40	—	50	
t <sub>ODD</sub>	Output Enable to Output in High-Z	—	35	—	40	—	50	
t <sub>OH</sub>	Output Data Hold Time	20	—	20	—	20	—	

### Write Cycle

SYMBOL	PARAMETER	TC5565APL-10L TC5565AFL-10L		TC5565APL-12L TC5565AFL-12L		TC5565APL-15L TC5565AFL-15L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	100	—	120	—	150	—	ns
t <sub>WP</sub>	Write Pulse Width	60	—	70	—	90	—	
t <sub>CW</sub>	Chip Selection to End of Write	80	—	85	—	100	—	
t <sub>AS</sub>	Address Set up Time	0	—	0	—	0	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	
t <sub>ODW</sub>	R/W to Output in High-Z	—	35	—	40	—	50	
t <sub>OEW</sub>	R/W to Output in Low-Z	5	—	5	—	10	—	
t <sub>DS</sub>	Data Set Up Time	40	—	50	—	60	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	

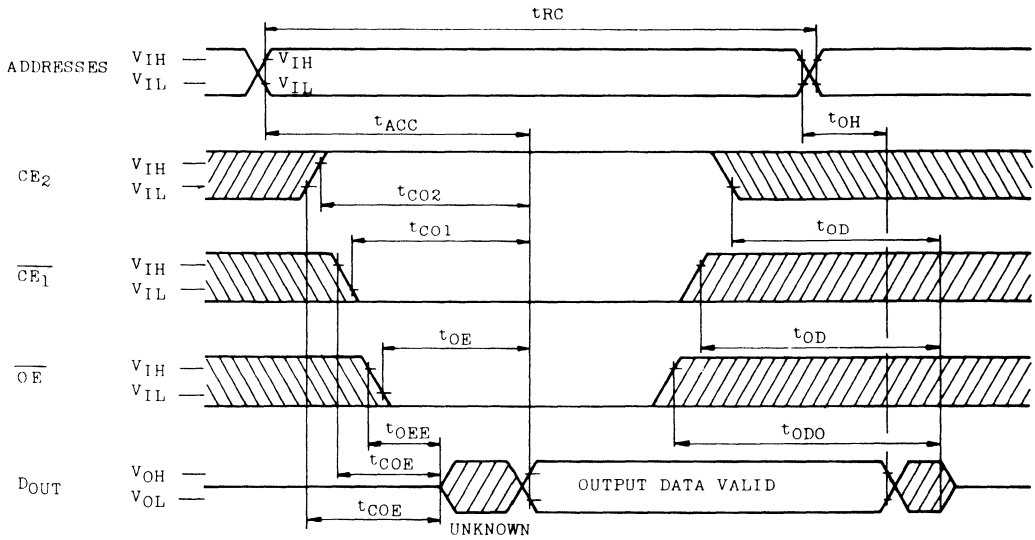
## A. C. TEST CONDITIONS

Output Load : 100pF + 1 TTL Gate  
 Input Pulse Level : 0.6V, 2.4V  
 Timing Measurement V<sub>IN</sub> : 0.8V, 2.2V  
 Reference Level V<sub>OUT</sub> : 0.8V, 2.2V  
 t<sub>r</sub>, t<sub>f</sub> : 5ns

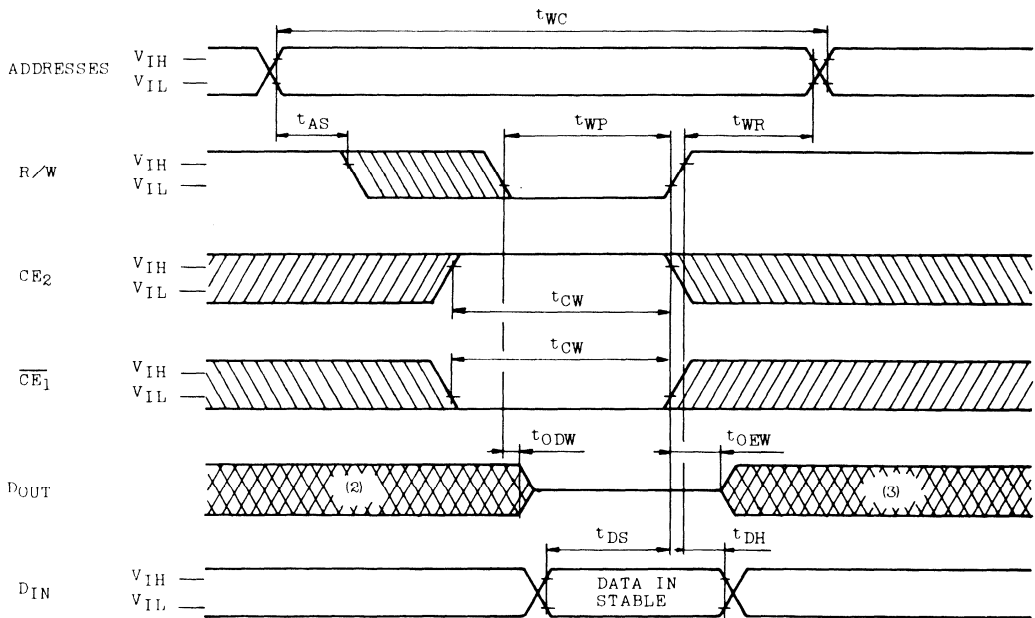
**TC5565APL-10L, TC5565APL-12L, TC5565APL-15L  
TC5565AFL-10L, TC5565AFL-12L, TC5565AFL-15L**

**TIMING WAVEFORMS**

● READ CYCLE (1)

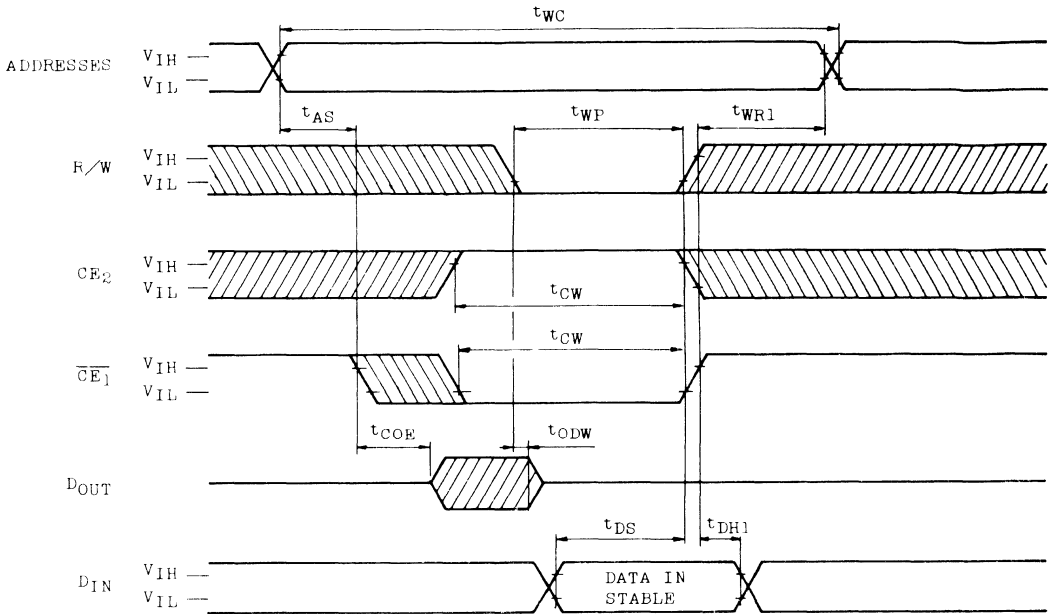


● WRITE CYCLE 1 (4) (R/W Controlled Write)

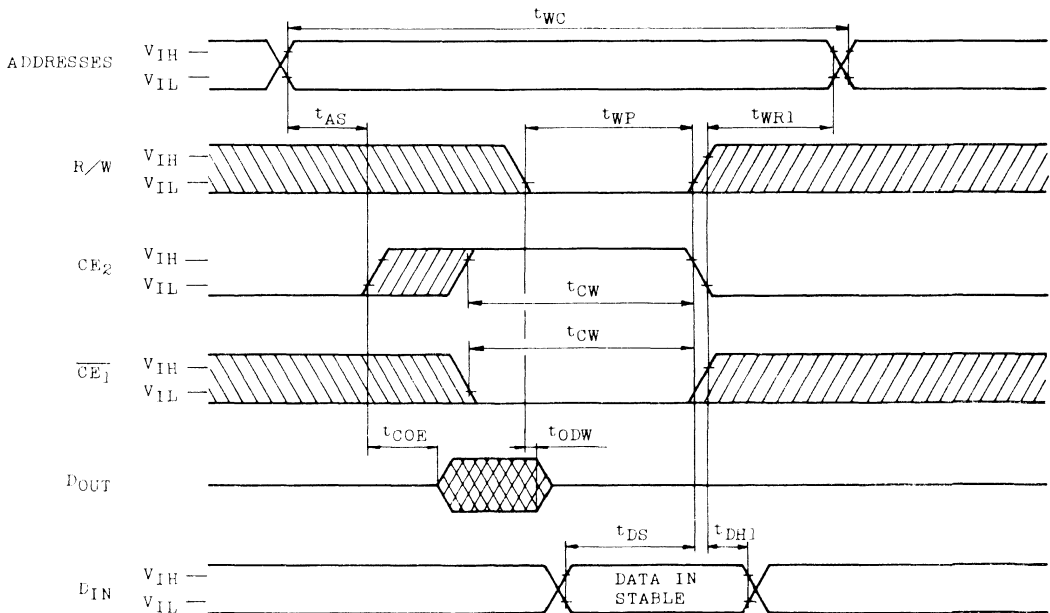


**TC5565APL-10L, TC5565APL-12L, TC5565APL-15L**  
**TC5565AFL-10L, TC5565AFL-12L, TC5565AFL-15L**

● **WRITE CYCLE 2 (4) ( $\overline{CE}_1$  Controlled Write)**



● **WRITE CYCLE 3 (4) ( $CE_2$  Controlled Write)**





# TC5565APL-10L, TC5565APL-12L, TC5565APL-15L TC5565AFL-10L, TC5565AFL-12L, TC5565AFL-15L

Note :

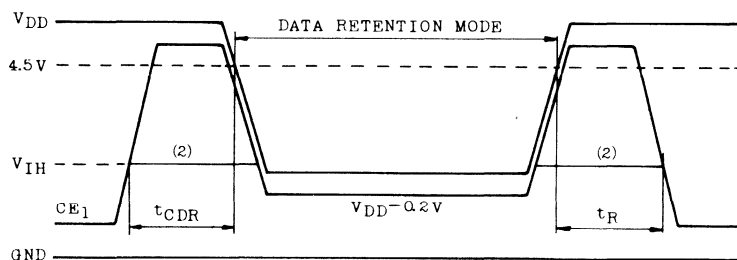
1. R/W is High for Read Cycle.
2. Assuming that  $\overline{CE}_1$  Low transition or  $CE_2$  High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that  $\overline{CE}_1$  High transition or  $CE_2$  Low transition occur coincident with or prior to R/W High transition, Outputs remain in a high impedance state.
4. Assuming that  $\overline{OE}$  is High for Write Cycle, Outputs are in high impedance state during this period.

## DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70°C)

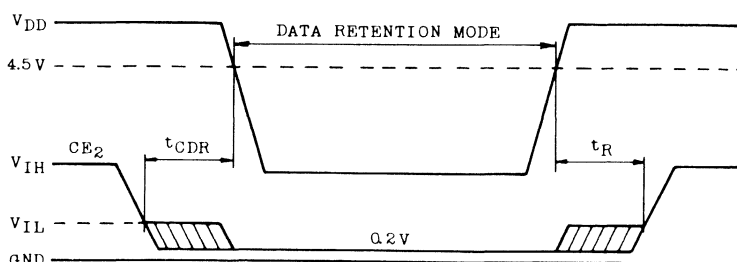
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{DH}$	Data Retention Supply Voltage	2.0	—	5.5	V
$I_{DD52}$	Stand by Supply Current	$V_{DD} = 3.0V$	—	15	$\mu A$
		$V_{DD} = 5.5V$	—	30	
$t_{CDR}$	Chip Deselection to Data Retention Mode	0	—	—	$\mu s$
$t_R$	Recovery Time	$t_{RC}^*$	—	—	ns

\* : Read cycle time.

### ● $\overline{CE}_1$ Controlled Data Retention Mode (1)



### ● $CE_2$ Controlled Data Retention Mode (3)



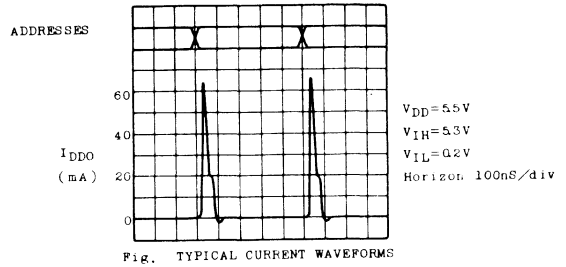
# TC5565APL-10L, TC5565APL-12L, TC5565APL-15L TC5565AFL-10L, TC5565AFL-12L, TC5565AFL-15L

Note :

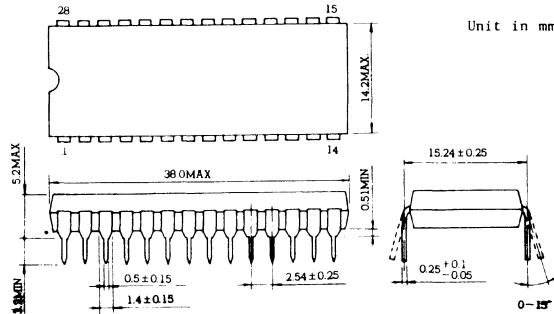
1. In  $\overline{CE}_1$  controlled data retention mode, minimum standby current mode is achieved under the condition of  $CE_2 \leq 0.2V$  or  $CE_2 \geq V_{DD} - 0.2V$ .
2. If the  $V_{IH}$  of  $\overline{CE}_1$  is 2.2V in operation,  $I_{DD1}$  current flows during the period that the  $V_{DD}$  voltage is going down from 4.5V to 2.4V.
3. In  $CE_2$  controlled data retention mode, minimum standby current mode is achieved under the condition of  $CE_2 \leq 0.2V$ .

## DEVICE INFORMATION

The TC5565APL/AFL is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure. This peak current may induce the noise on  $V_{DD}/GND$  lines. Thus the use of about 0.1  $\mu F$  decoupling capacitor for every device is recommended to eliminate such noise.

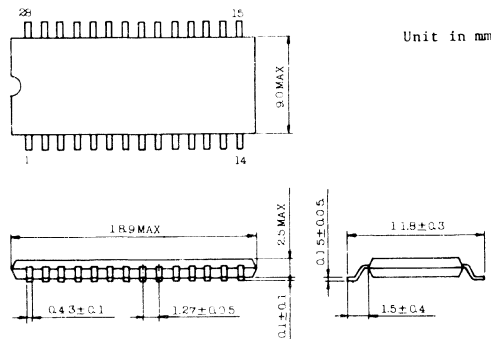


### ● DIP 28 PIN OUTLINE DRAWING (6D28A-P)



Note : Lead pitch is 2.54 and tolerance is  $\pm 0.25$  against theoretical center of each lead that is obtained on the basis of No. 1 and No. 28 leads.

### ● MFP 28 PIN OUTLINE DRAWING (F28GC-P)



Note : Lead pitch is 1.27 and tolerance is  $\pm 0.12$  against theoretical center of each lead that is obtained on the basis of No. 1 and No. 28 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described : no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry

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# TOSHIBA MOS MEMORY PRODUCT

8,192 WORD × 8 BIT CMOS STATIC RAM

TC5564APL-12, TC5564APL-15  
TC5564AFL-12, TC5564AFL-15

## DESCRIPTION

TC5564APL is 65536 bits static random access memory organized as 8192 words by 8 bits using CMOS technology, and operates with a single 5V power supply.

Advanced circuit techniques provides low power feature with a maximum operating of 5mA/MHz. Operation current depends on cycle time.

TC5564APL has three control inputs. Two chip enables (CE1, CE2) allow for device selection and data retention control. Output enable (OE) input provides fast memory access. When device is placed in standby mode with chip off state, standby current

is typically 0.01μA. So the TC5564APL is suitable for use in various microprocessor application systems where low power and battery back up are required. Ultra low standby power allow not only battery but capacitance backup.

Pin assignment of TC5564APL is pin-compatible with the 64K bits EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.

TC5564APL is offered in both a standard dual-in-line 28 pin plastic package (0.6 inch width) and small-out-line plastic flat package.

## FEATURES

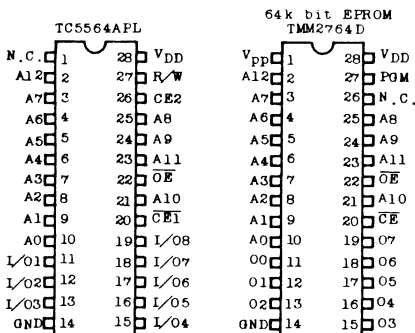
- Low Power Dissipation  
5mA/MHz (MAX.) Operating  
0.2μA (MAX.) at Ta=25°C Standby  
1.0μA (MAX.) at Ta=60°C Standby
- 5V Single Power Supply
- Low Voltage Operation : VDD=3V  
Tco=1μs (MAX.) Ta=60°C
- Fully Static Operation
- Data Retention Voltage : 2.0~5.5V
- Plastic DIP and Plastic FP Package
- Pin Compatible with 2764 type EPROM

## ● Access Time

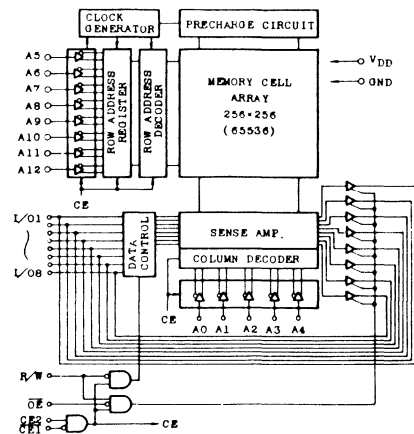
	TC5564APL-12 TC5564AFL-12	TC5564APL-15 TC5564AFL-15
Address Access Time (MAX.)	120ns	150ns
CE1 Access Time (MAX.)	120ns	150ns
CE2 Access Time (MAX.)	120ns	150ns
Output Enable Time (MAX.)	60ns	70ns

- Directly TTL Compatible : All Inputs and Outputs
- Wide Temperature Operation : -40~85°C

## PIN CONNECTION (TOP VIEW)



## BLOCK DIAGRAM



# TC5564APL-12, TC5564APL-15 TC5564AFL-12, TC5564AFL-15

## PIN NAMES

A <sub>0</sub> ~A <sub>12</sub>	Address Inputs
R/W	Read/Write Control Input
OE	Output Enable Input
CE1, CE2	Chip Enable Inputs
I/O1~I/O8	Data Input/Output
V <sub>DD</sub>	Power (+5V)
GND	Ground
N. C.	No Connection

## OPERATING MODE

Operation Mode	CE1	CE2	OE	R/W	I/O1~I/O8	Power
Read	L	H	L	H	D <sub>OUT</sub>	I <sub>DD0</sub>
Write	L	H	*	L	D <sub>IN</sub>	
Output Deselect	*	*	H	*	High-Z	I <sub>DD5</sub> I <sub>DD5</sub>
Standby	H	*	*	*	"	
	*	L	*	*	"	

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
*V <sub>DD</sub>	Power Supply Voltage	-0.3~7.0	V
V <sub>IN</sub>	Input Voltage	-0.3**~V <sub>DD</sub>	V
V <sub>I.O</sub>	Input and Output Voltage	-0.5~V <sub>DD</sub> +0.5	V
P <sub>D</sub>	Power Dissipation	1.0(0.6)***	W
T <sub>solder</sub>	Soldering Temperature	260±10	°C·sec
T <sub>stg</sub>	Storage Temperature	-55~150	°C
T <sub>opr</sub>	Operating Temperature	-40~85	°C

\* 8.5V at 100ns

\*\* -3.0V Pulse width 50ns

\*\*\* SOP

## D. C. RECOMMENDED OPERATING CONDITIONS (T<sub>a</sub> = -40~85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3*	—	0.8	V
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	—	5.5	V

\* -3.0V Pulse width 50ns

## D. C and OPERATING CHARACTERISTICS (T<sub>a</sub> = -40~85°C, V<sub>DD</sub> = 5V ± 10% Unless other wise noted)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 0~V <sub>DD</sub>	—	—	±1.0	μA
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4V	-1.0	—	—	mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4V	4.0	—	—	mA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -20μA	V <sub>DD</sub> -0.1	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 20μA	—	—	0.1	V
I <sub>LO</sub>	Output Leakage Current	CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub> or R/W = V <sub>IL</sub> or OE = V <sub>IH</sub> , V <sub>OUT</sub> = 0~V <sub>DD</sub>	—	—	±1.0	μA

# TC5564APL-12, TC5564APL-15 TC5564AFL-12, TC5564AFL-15

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT	
I <sub>DD01</sub>	Operating Current	CE1 = V <sub>IL</sub> and CE2 = V <sub>IH</sub> Other Input = V <sub>IH</sub> /V <sub>IL</sub> I <sub>OUT</sub> = 0mA	t <sub>cycle</sub> = 1 μs	—	—	10	mA	
			MIN. CYCLE	TC5564APL 12 TC5564AFL 12	—	—		45
				TC5564APL 15 TC5564AFL 15	—	—		40
I <sub>DD02</sub>	Operating Current	CE1 = 0.2V and CE2 = V <sub>DD</sub> - 0.2V, Other Input = V <sub>DD</sub> - 0.2V/0.2V I <sub>OUT</sub> = 0mA	t <sub>cycle</sub> = 1 μs	—	—	5	mA	
			MIN. CYCLE	TC5564APL 12 TC5564AFL 12	—	—		40
I <sub>DD03</sub>	Standby Current	CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub>		—	—	2	mA	
			—	—	2			
I <sub>DD02</sub>	Standby Current	CE1 = V <sub>DD</sub> - 0.2V or CE2 = 0.2V V <sub>DD</sub> = 2.0 ~ 5.5V	Ta = 25°C	—	0.01	0.2	μA	
			Ta = 60°C	—	—	1.0		

Note : (1) In standby mode with CE1 ≥ V<sub>DD</sub> - 0.2V, these specification limits are guaranteed under the condition of CE2 ≥ V<sub>DD</sub> - 0.2V or CE2 ≤ 0.2V.

(2) All voltage is measured from GND.

## CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = GND	10	pF

Note This parameter is periodically sampled and is not 100% tested.

# TC5564APL-12, TC5564APL-15 TC5564AFL-12, TC5564AFL-15

## A. C. CHARACTERISTICS

### READ CYCLE

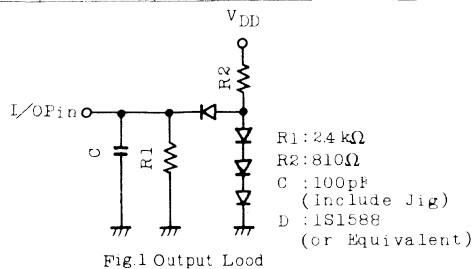
SYMBOL	PARAMETER	TC5564APL-12 TC5564AFL-12		TC5564APL-15 TC5564AFL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	120	—	150	—	ns
t <sub>ACC</sub>	Address Access Time	—	120	—	150	
t <sub>CO1</sub>	$\overline{CE1}$ Access Time	—	120	—	150	
t <sub>CO2</sub>	CE2 Access Time	—	120	—	150	
t <sub>OE</sub>	Output Enable to Output in Valid	—	60	—	70	
t <sub>COE</sub>	Chip Enable to ( $\overline{CE1}$ , CE2) Output in Low-Z	10	—	10	—	
t <sub>OEE</sub>	Output Enable to Output Low-Z	5	—	5	—	
t <sub>OD</sub>	Chip Enable ( $\overline{CE1}$ , CE2) Output in High-Z	—	60	—	70	
t <sub>ODO</sub>	Output Enable to Output High-Z	—	50	—	60	
t <sub>OH</sub>	Output Data Hold Time	20	—	20	—	

### WRITE CYCLE

SYMBOL	PARAMETER	TC5564APL-12 TC5564AFL-12		TC5564APL-15 TC5564AFL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	120	—	150	—	ns
t <sub>WP</sub>	Write Pulse Width	80	—	100	—	
t <sub>cw</sub>	Chip Selection to End of Write	100	—	120	—	
t <sub>AS</sub>	Address Set up Time	0	—	0	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	
t <sub>ODW</sub>	R/W to Output High-Z	—	60	—	70	
t <sub>OEW</sub>	R/W to Output Low-Z	10	—	10	—	
t <sub>DS</sub>	Data Set Up Time	50	—	60	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	

### A. C. TEST CONDITIONS

- Input Pulse Levels : 2.4V/0.6V
- Timing Measurement Reference Levels : 2.2V/0.8V
- Output Reference Levels : 2.2V/0.8V
- Input Pulse Rise and Fall Times : 5ns
- Output Load : See Fig. 1



# TC5564APL-12, TC5564APL-15 TC5564AFL-12, TC5564AFL-15

## 3V OPERATE SPECIFICATION

### D. C RECOMMENDED OPERATING CONDITIONS (Ta = -10~60°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	2.7	3.0	3.3	V
V <sub>IH</sub>	Input High Voltage	V <sub>DD</sub> -0.2	—	V <sub>DD</sub>	V
V <sub>IL</sub>	Input Low Voltage	0	—	0.2	V

### D. C and OPERATING CHARACTERISTICS (Ta = -10~60°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 0 ~ V <sub>DD</sub>	—	—	±1.0	μA	
I <sub>LO</sub>	Output Leakage Current	CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub> or R/W = V <sub>IL</sub> or OE = V <sub>IH</sub> V <sub>OUT</sub> = 0 ~ V <sub>DD</sub>	—	—	±1.0	μA	
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = V <sub>DD</sub> - 0.2V	-100	—	—	μA	
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.2V	100	—	—	μA	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -20μA	V <sub>DD</sub> -0.1	—	—	V	
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 20μA	—	—	0.1	V	
I <sub>DDC</sub> *	operating Current	CE1 = V <sub>IL</sub> and CE2 = V <sub>IH</sub> Other input = V <sub>DD</sub> - 0.2V/0.2V I <sub>OUT</sub> = 0mA, duty 100%	t <sub>cycle</sub> = 1μs	—	2.0	3.0	mA
			t <sub>cycle</sub> = 10μs	—	—	0.5	
I <sub>DDs</sub>	Standby Current Current	CE1 = V <sub>IL</sub> and CE2 = V <sub>IH</sub> or CE2 = V <sub>IL</sub>	Ta = 25°C	—	0.01	0.2	μA
			Ta = 60°C	—	—	1.0	

● All voltage is measured from BND

\* I<sub>DDC</sub> is slightly depending on input pulse t<sub>r</sub>, t<sub>f</sub>. If long t<sub>r</sub>, t<sub>f</sub> pulse is applied, there are some transient current at input stage. These specification is guaranteed with t<sub>r</sub>, t<sub>f</sub> ≤ 20ns

# TC5564APL-12, TC5564APL-15 TC5564AFL-12, TC5564AFL-15

## 3V OPERATE SPECIFICATION

### A. C. CHARACTERISTICS (Ta = -10~60°C, VDD=3V±10%)

#### READ CYCLE

SYMBOL	PARAMETER	MIN.	TYP.*	MAX.	UNIT
t <sub>RC</sub>	Read Cycle Time	1000	—	—	ns
t <sub>ACC</sub>	Address Access Time	—	300	1000	
t <sub>CO1</sub>	CE1 Access Time	—	300	1000	
t <sub>CO2</sub>	CE2 Access Time	—	300	1000	
t <sub>OE</sub>	Output Enable to Output Valid	—	100	200	
t <sub>OH</sub>	Output Data Hold Time	20	—	—	
t <sub>COE</sub>	Chip Enable to Output in Low Z	10	—	—	
t <sub>OEE</sub>	Output Enable to Output in Low Z	5	—	—	
t <sub>OD</sub>	Chip Enable to Output in High Z	—	—	200	
t <sub>ODO</sub>	Output Enable to Output in High Z	—	—	150	

#### WRITE CYCLE

SYMBOL	PARAMETER	MIN.	TYP.*	MAX.	UNIT
t <sub>WC</sub>	Write Cycle Time	1000	—	—	ns
t <sub>WP</sub>	Write Pulse Width	500	—	—	
t <sub>CW</sub>	Chip Selection to End of Write	800	—	—	
t <sub>AS</sub>	Address Set Up Time	100	—	—	
t <sub>WR</sub>	Write Recovery Time	100	—	—	
t <sub>US</sub>	Data Set Up Time	400	—	—	
t <sub>DH</sub>	Data Hold Time	50	—	—	
t <sub>ODW</sub>	R/W to Output High Z	—	—	200	
t <sub>OEW</sub>	R/W to Output Low Z	10	—	—	

\* Typ. condition is Ta=25°C, VDD=3V

### A. C. TEST CONDITIONS

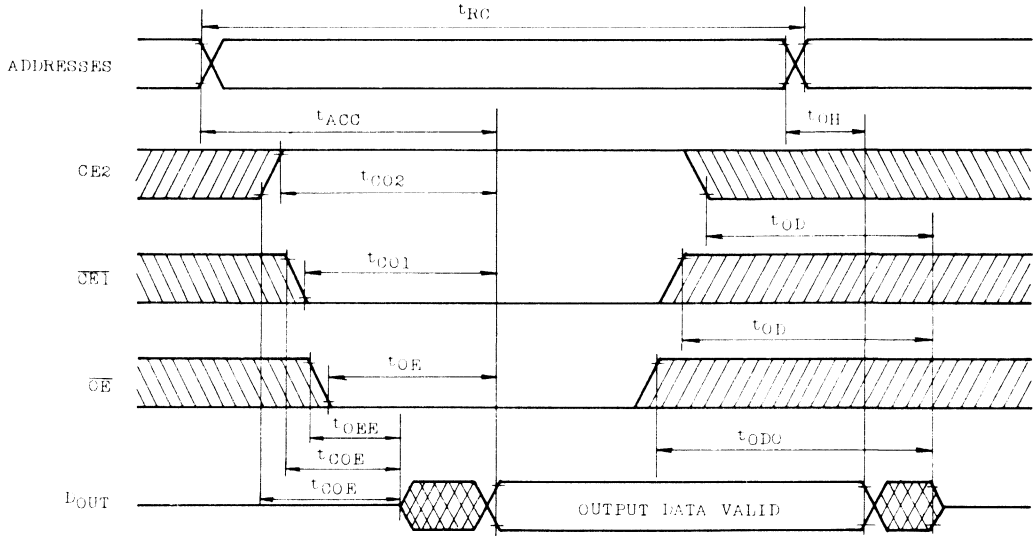
- V<sub>IN</sub>=V<sub>DD</sub>-0.2V/0.2V
- Output Reference Level : 1.5V/1.5V
- Timing Measurement Level : 1.5V/1.5V
- Input Rise and Fall Time : ≤20ns
- Output Load : 100pF (Include Jig)



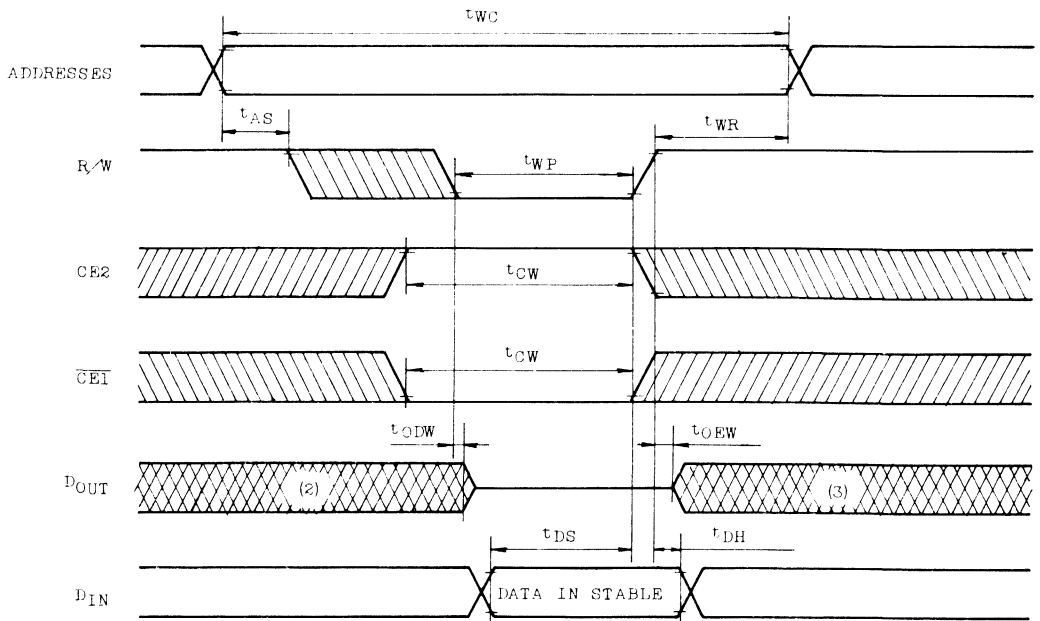
**TC5564APL-12, TC5564APL-15  
TC5564AFL-12, TC5564AFL-15**

**TIMING WAVEFORMS**

**READ CYCLE (1)**

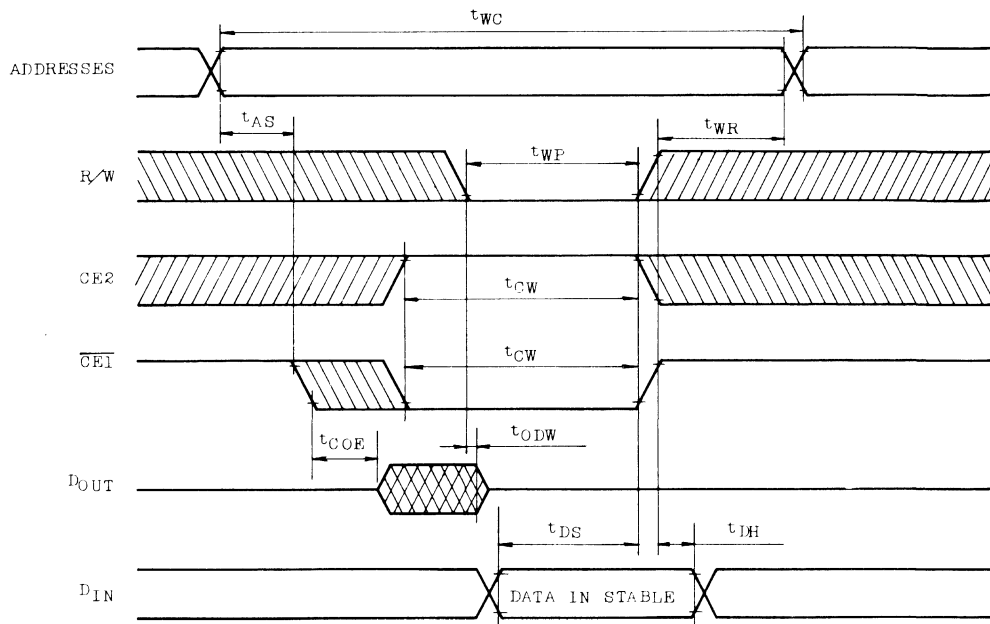


**WRITE CYCLE (R/E Controlled Write)**

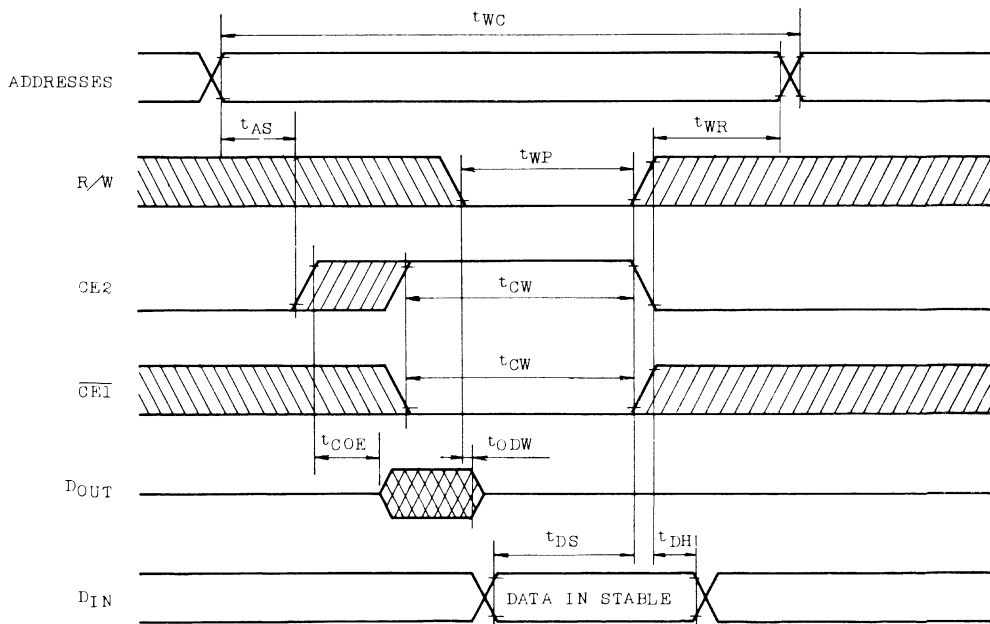


**TC5564APL-12, TC5564APL-15**  
**TC5564AFL-12, TC5564AFL-15**

WRITE CYCLE 2 (4) ( $\overline{CE1}$  Controlled Write)



WRITE CYCLE 3 (4) (CE2 Controlled Write)



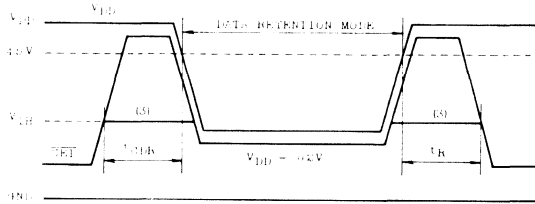
# TC5564APL-12, TC5564APL-15 TC5564AFL-12, TC5564AFL-15

Note : (1) R/W is High for Read Cycle. (2) Assuming that  $\overline{CE1}$  Low transition or CE2 High transition occurs coincident with or after R/W low transition, Outputs remain in a high impedance state. (3) Assuming that  $\overline{CE1}$  High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state. (4) Assuming that  $\overline{OE}$  is High for Write Cycle, Outputs are in high impedance state during this period.

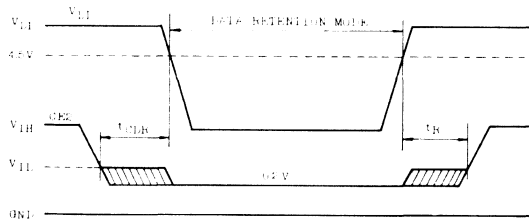
## DATA RETENTION CHARACTERISTICS (Ta = -40~85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	—	5.5	V	
I <sub>DD52</sub>	Standby Current	Ta = 25°C		0.01	0.2	μA
		Ta = 60°C		—	1.0	
t <sub>CDR</sub>	Chip Deselection to Data Retention Mode	0	—	—	μs	
t <sub>R</sub>	Recovery Time	t <sub>RC(1)</sub>	—	—	ns	

### CE1 Controlled Data Retention Mode (2)



### CE2 Controlled Data Retention Mode (4)



Note : (1) t<sub>RC</sub> : Read Cycle Time (2) In  $\overline{CE1}$  controlled data retention mode, minimum standby current mode is achieved under the condition of  $CE2 \leq 0.2V$  or  $CE2 \geq V_{DD} - 0.2V$ . (3) If the V<sub>IH</sub> of  $\overline{CE1}$  is 2.2V in operation, during the period that the V<sub>DD</sub> Voltage is going down from 4.5 to 2.4V, I<sub>DD51</sub> current flows. (4) In CE2 controlled data retention mode, minimum standby current mode is achieved under the condition of  $CE2 \leq 0.2V$ .

## DEVICE INFORMATION

The TC5564APL is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation executed by internal pulse generated from row address transient. Therefore the peak current flows

after only row address change, as is shown in the following figure.

This peak current may induce the noise on V<sub>DD</sub>/GND line. Thus the use of about 0.1μF decoupling capacitor every device is recommended to eliminate such noise.

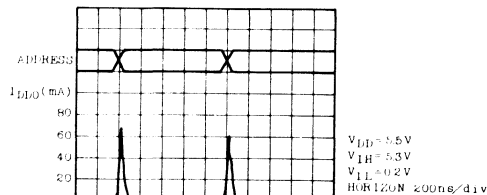
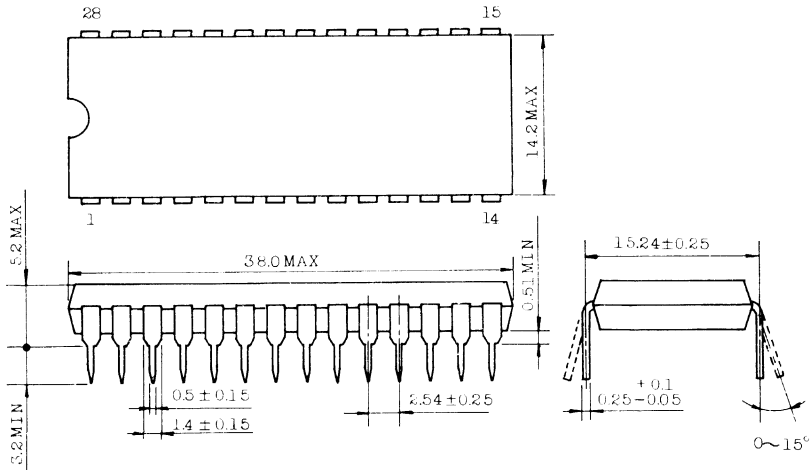


Fig. TYPICAL CURRENT WAVEFORMS

**TC5564APL-12, TC5564APL-15**  
**TC5564AFL-12, TC5564AFL-15**

DIP 28 PIN OUTLINE DRAWING (6D28A-P)

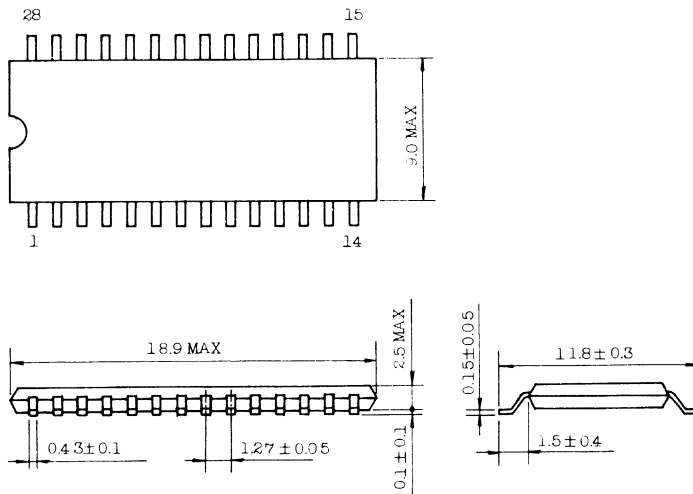
Unit in mm



Note : Lead pitch is 2.54 and tolerance is  $\pm 0.25$  against theoretical center of each lead that is obtained on the basis of No. 1 and No. 28 leads.

MFP 28 PIN OUTLINE DRAWINGS (F28GA-P)

Unit in mm



Note : Lead pitch is 1.27 and tolerance is  $\pm 0.12$  against theoretical center of each lead that is obtained on the basis of No. 1 and No. 28 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described : no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.  
 c May, 1986 Toshiba Corporation

# TOSHIBA MOS MEMORY PRODUCT

32,768 WORD × 8 BIT CMOS STATIC RAM  
SILICON GATE CMOS

TC55257PL-85, TC55257P-10/PL-10  
TC55257P-12/PL-12

## DESCRIPTION

The TC55257P is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a operating current of 5mA/MHZ(Typ.) and minimum cycle time of 85ns.

When  $\overline{CE}$  is a logical high, the device is placed in low power standby mode in which standby current is 2 $\mu$ A typically. The TC55257P has two control inputs. Chip enable ( $\overline{CE}$ ) allow for device selection and data retention control, and an output enable input ( $\overline{OE}$ ) provides fast memory access. Thus the TC55257P is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC55257P is offered in a dual-in-line 28 pin standard plastic package.

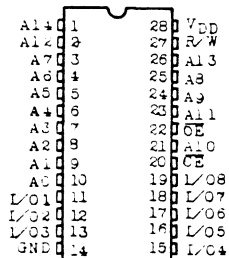
## FEATURES

- Low Power Dissipation  
27.5mW/1MHz(Max.) Operating
- Standby Current  
100 $\mu$ A(Max.): TC55257PL-85/  
PL-10/  
PL-12  
1 $\mu$ A(Max.): TC55257P-10/  
P-12
- 5V Single Power Supply
- Power Down Feature:  $\overline{CE}$
- Data Retention Supply Voltage: 2.0 ~ 5.5V
- Access Time

	TC55257PL-85	TC55257P-10 TC55257PL-10	TC55257P-12 TC55257PL-12
Access Time (Max.)	85ns	100ns	120ns
CE Access Time (Max.)	85ns	100ns	120ns
Output Enable Time(Max.)	40ns	50ns	60ns

- Directly TTL Compatible: All Inputs and Outputs
- Standard 28 pin DIP

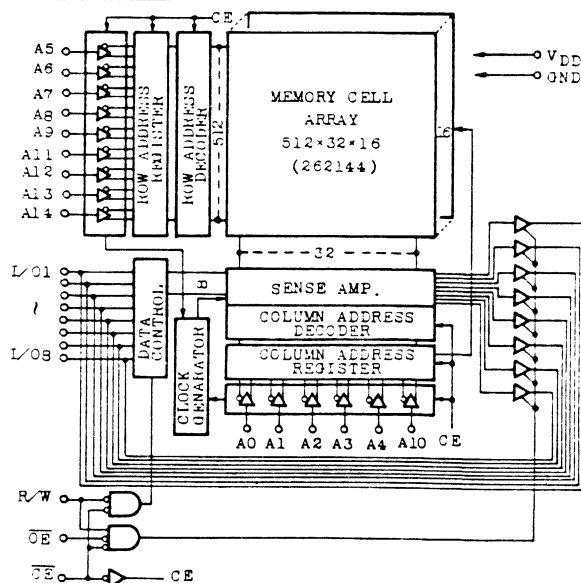
## PIN CONNECTION (TOP VIEW)



## PIN NAMES

A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V <sub>DD</sub>	Power (+5V)
GND	Ground

## BLOCK DIAGRAM



# TC55257PL-85, TC55257P-10/PL-10 TC55257P-12/PL-12

## OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O <sub>1</sub> ~ I/O <sub>8</sub>	POWER
Read	L	L	H	D <sub>OUT</sub>	I <sub>DDO</sub>
Write	L	*	L	D <sub>IN</sub>	I <sub>DDO</sub>
Output Deselect	L	H	H	High-Z	I <sub>DDO</sub>
Standby	H	*	*	High-Z	I <sub>DDS</sub>

\*) H or L

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.3 ~ 7.0	V
V <sub>IN</sub>	Input Voltage	-0.3* ~ 7.0	V
V <sub>I/O</sub>	Input and Output Voltage	-0.5 ~ V <sub>DD</sub> +0.5	V
P <sub>D</sub>	Power Dissipation	1.0	W
T <sub>solder</sub>	Soldering Temperature	260 ± 10	°C·sec
T <sub>strg</sub>	Storage Temperature	-55 ~ 150	°C
T <sub>opr</sub>	Operating Temperature	0 ~ 70	°C

\* ..... -3.0V at pulse width 50ns

## D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	-	0.8	V
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	-	5.5	V

# TC55257PL-85, TC55257P-10/PL-10 TC55257P-12/PL-12

## D.C. and OPERATING CHARACTERISTICS (Ta=0~70°C, VDD=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> =0~V <sub>DD</sub>	-	-	±1.0	μA	
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> =2.4V	-1.0	-	-	mA	
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> =0.4V	4.0	-	-	mA	
I <sub>LO</sub>	Output Leakage Current	$\overline{CE}=V_{IH}$ or R/W=V <sub>IL</sub> or $\overline{OE}=V_{IH}$ V <sub>OUT</sub> =0~V <sub>DD</sub>	-	-	±1.0	μA	
I <sub>DDO1</sub>	Operating Current (Read Cycle)*	V <sub>DD</sub> =5.5V $\overline{CE}=V_{IL}$ , R/W=V <sub>IH</sub> Other Input =V <sub>IH</sub> /V <sub>IL</sub> I <sub>OUT</sub> =0mA	t <sub>cycle</sub> =1μs	-	-	10	mA
			t <sub>cycle</sub> = Min. cycle	-	-	70	
I <sub>DDO2</sub>		V <sub>DD</sub> =5.5V $\overline{CE}=0.2V$ , R/W=V <sub>DD</sub> -0.2V Other Input =V <sub>DD</sub> -0.2V/0.2V I <sub>OUT</sub> =0mA	t <sub>cycle</sub> =1μs	-	-	.5	mA
				t <sub>cycle</sub> = Min. cycle	-	-	
I <sub>DDS1</sub>	Standby Current	$\overline{CE}=V_{IH}$	-	-	3	mA	
I <sub>DDS2</sub>	Standby Current	$\overline{CE}=V_{DD}-0.2V$	TC55257PL	-	2	100	μA
		V <sub>DD</sub> =2.0~5.5V	TC55257P	-	-	1.0	mA

\* Assuming that R/W is Low for Write Cycle, the current consumption is twice as much as that when R/W is High for Write Cycle.

## CAPACITANCE (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> =GND	10	pF

Note: This parameter periodically sampled is not 100% tested.

# TC55257PL-85, TC55257P-10/PL-10 TC55257P-12/PL-12

## A.C. CHARACTERISTICS

( $T_a=0 \sim 70^\circ\text{C}$ ,  $V_{DD}=5V \pm 10\%$ )

### Read Cycle

SYMBOL	PARAMETER	TEST CONDITION	TC55257PL-85		TC55257P-10 /PL-10		TC55257P-12 /PL-12		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{RC}$	Read Cycle Time	$V_{IN}=2.4V/0.6V$ $V_{IH}=2.2V$ $V_{IL}=0.8V$ $t_r, t_f \leq 5ns$ $V_{OH}=2.2V$ $V_{OL}=0.8V$  Output Load: $C_L(100pF)$ and 1 TTL Gate	85	-	100	-	120	-	ns
$t_{ACC}$	Address Access Time		-	85	-	100	-	120	
$t_{CO}$	$\overline{CE}$ Access Time		-	85	-	100	-	120	
$t_{OE}$	Output Enable to Output in Valid		-	40	-	50	-	60	
$t_{COE}$	Chip Enable( $\overline{CE}$ ) to Output in Low-Z		10	-	10	-	10	-	
$t_{OEE}$	Output Enable to Output in Low-Z		5	-	5	-	5	-	
$t_{OD}$	Chip Enable( $\overline{CE}$ ) to Output in High-Z		-	30	-	50	-	60	
$t_{ODO}$	Output Enable to Output in High-Z		-	30	-	40	-	50	
$t_{OH}$	Output Data Hold Time		5	-	10	-	10	-	

### Write Cycle

SYMBOL	PARAMETER	TEST CONDITION	TC55257PL-85		TC55257P-10 /PL-10		TC55257P-12 /PL-12		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{WC}$	Write Cycle Time	$V_{IN}=2.4V/0.6V$ $V_{IH}=2.2V$ $V_{IL}=0.8V$ $t_r, t_f \leq 5ns$	85	-	100	-	120	-	ns
$t_{WP}$	Write Pulse Width		60	-	70	-	80	-	
$t_{CW}$	Chip Selection to End of Write		65	-	90	-	100	-	
$t_{AS}$	Address Set up Time		0	-	0	-	0	-	
$t_{WR}$	Write Recovery Time		10	-	10	-	10	-	
$t_{ODW}$	R/W to Output High-Z		-	30	-	50	-	60	
$t_{OEW}$	R/W to Output Low-Z		10	-	10	-	10	-	
$t_{DS}$	Data Set up Time		40	-	40	-	50	-	
$t_{DH}$	Data Hold Time		0	-	0	-	0	-	

Note: Input pulse levels= $V_{IN}$

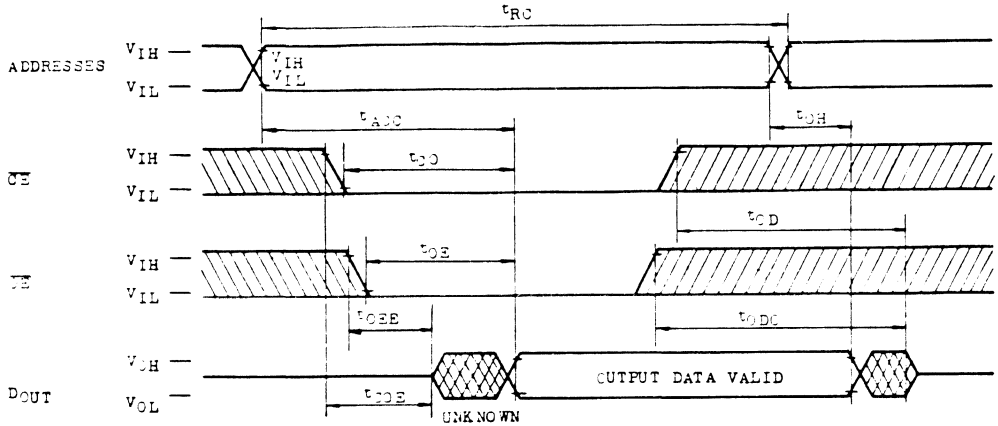
Timing Measurement Reference levels= $V_{IH}$ ,  $V_{IL}$



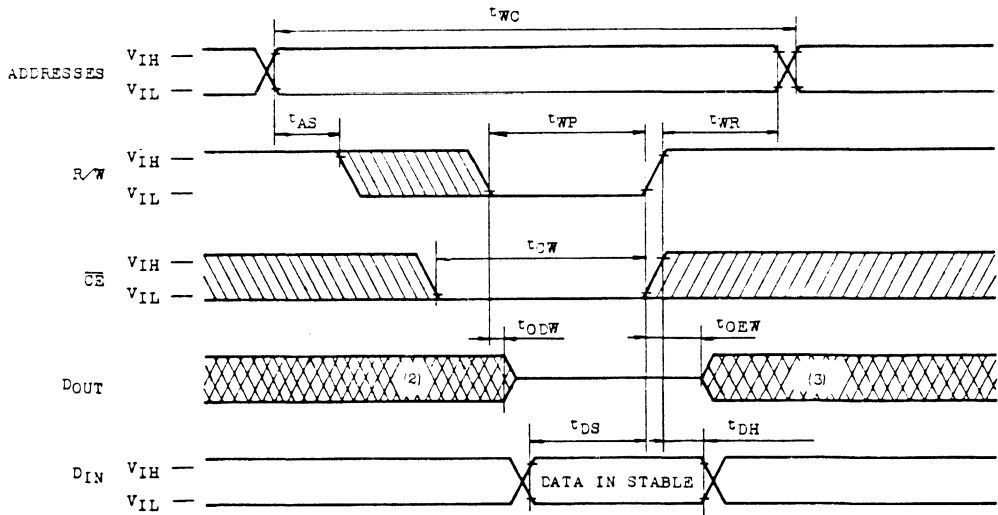
**TC55257PL-85, TC55257P-10/PL-10  
TC55257P-12/PL-12**

TIMING WAVEFORMS

READ CYCLE (1)

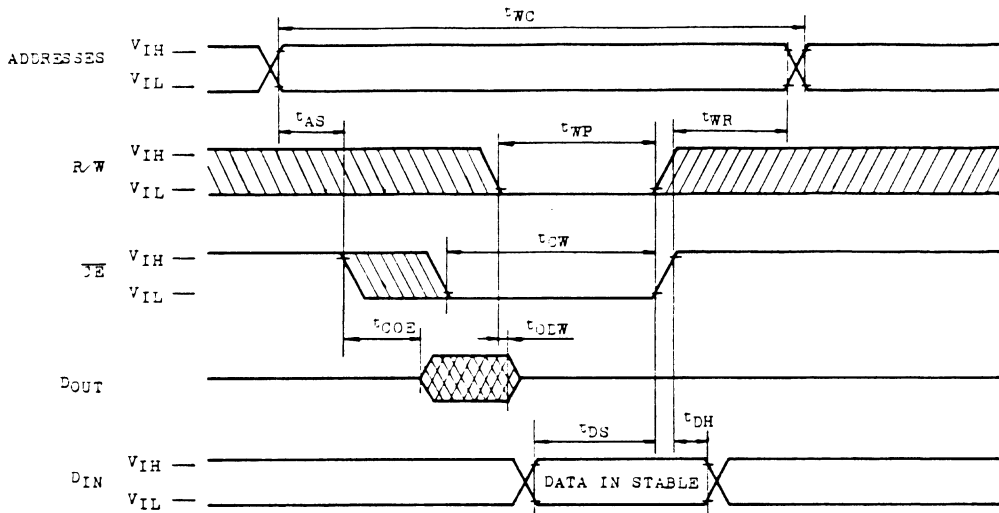


WRITE CYCLE 1 (4) (R/W Controlled Write)



**TC55257PL-85, TC55257P-10/PL-10  
TC55257P-12/PL-12**

WRITE CYCLE 2 (4) ( $\overline{CE}$  Controlled Write)



- Note: 1. R/W is High for Read Cycle.
2. Assuming that  $\overline{CE}$  low transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that  $\overline{CE}$  High transition occurs coincident with or prior to R/W High transition, Outputs remain in a high impedance state.
4. Assuming that  $\overline{OE}$  is High for Write Cycle, Outputs are in high impedance state during this period.

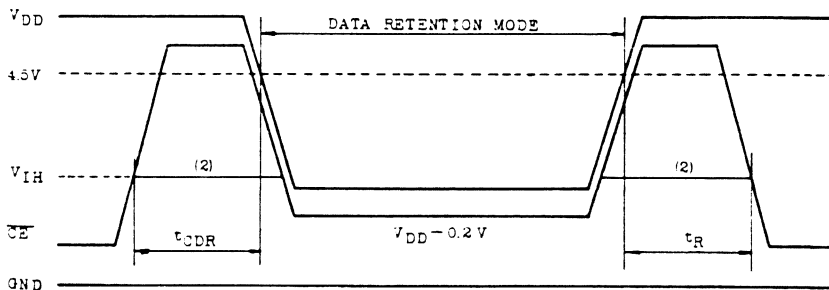
# TC55257PL-85, TC55257P-10/PL-10 TC55257P-12/PL-12

## DATA RETENTION CHARACTERISTICS (Ta=0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT	
V <sub>DH</sub>	Data Retention Supply Voltage		2.0	-	5.5	V	
I <sub>DD2</sub>	Standby Supply Current	TC55257PL	V <sub>DD</sub> =3.0V	-	-	50	μA
			V <sub>DD</sub> =5.5V	-	-	100	
		TC55257P		-	-	1.0	mA
t <sub>CDR</sub>	Chip Deselection to Data Retention Mode		0	-	-	μs	
t <sub>R</sub>	Recovery Time		t <sub>RC</sub> (1)	-	-		

Note (1): Read cycle time

### $\overline{CE}$ Controlled Data Retention Mode

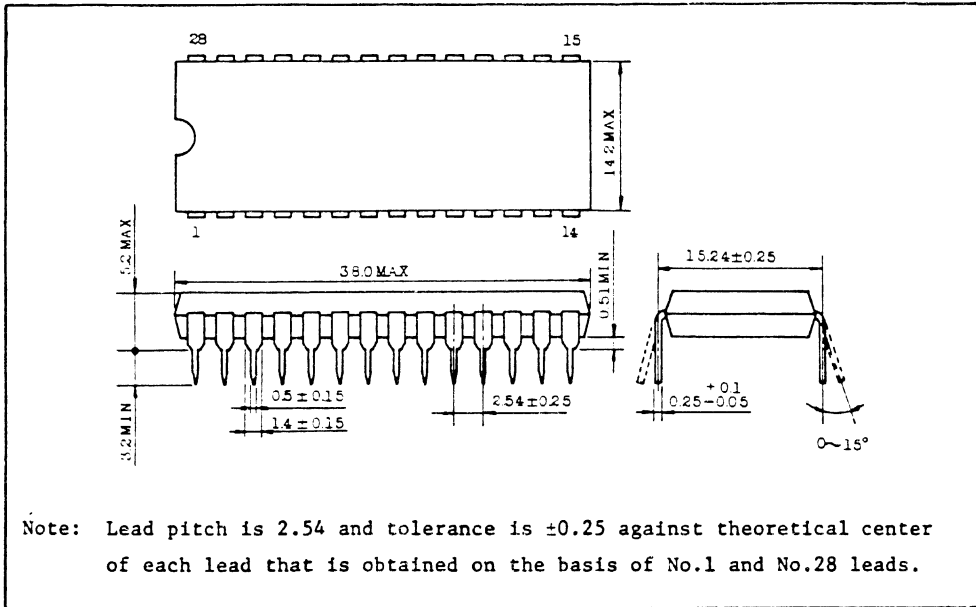


Note (2): If the V<sub>IH</sub> of  $\overline{CE}$  is 2.4V in operation, I<sub>DD1</sub> current flows during the period that the V<sub>DD</sub> voltage is going down from 4.5V to 2.4V.

**TC55257PL-85, TC55257P-10/PL-10  
TC55257P-12/PL-12**

DIP 28 PIN OUTLINE DRAWING (6D28A-P)

Unit in mm



Note: Lead pitch is 2.54 and tolerance is  $\pm 0.25$  against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

# TOSHIBA MOS MEMORY PRODUCT

**32,768 WORD × 8 BIT CMOS STATIC RAM**  
 SILICON GATE CMOS  
 PRELIMINARY

**TC55257AP-10/APL-10/AP-12/APL-12**  
**TC55257AF-10/AFL-10/AF-12/AFL-12**

## DESCRIPTION

The TC55257AP is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and minimum cycle time of 100ns/120ns.

When  $\overline{CE}$  is a logical high, the device is placed in low power standby mode in which standby current is 2 $\mu$ A typically. The TC55257AP has two control inputs. Chip enable ( $\overline{CE}$ ) allow for device selection and data retention control, and an output enable input ( $\overline{OE}$ ) provides fast memory access. Thus the TC55257AP is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

TC55257AP is offered in both a standard dual-in-line 28 pin plastic package (0.6 inch width) and small-out-line plastic flat package.

## FEATURES

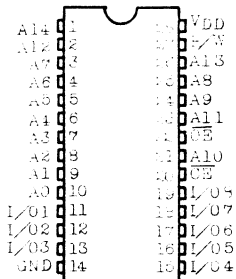
- Low Power Dissipation  
 27.5mW/MHz (Max.) Operating
- Standby Current  
 100 $\mu$ A (Max.): TC55257APL-10/APL-12  
 /AFL-10/AFL-12  
 1mA (Max.): TC55257AP-10/AP-12  
 /AF-10/AF-12
- 5V Single Power Supply
- Power Down Feature:  $\overline{CE}$
- Data Retention Supply Voltage:  
 2.0 ~ 5.5V

### • Access Time

	TC55257AP-10/APL-10 AF-10/AFL-10	TC55257AP-12/APL-12 AF-12/AFL-12
Access Time (MAX.)	100ns	120ns
CE Access Time (MAX.)	100ns	120ns
Output Enable Time (MAX.)	50ns	60ns

- Directly TTL Compatible: All Inputs and Outputs
- Plastic DIP and Plastic FP Package

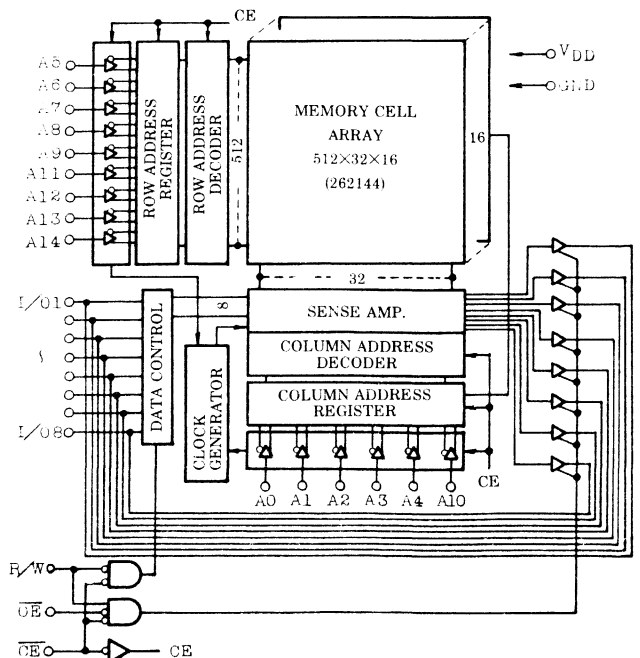
## PIN CONNECTION (TOP VIEW)



## PIN NAMES

A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
VDD	Power (+5V)
GND	Ground

## BLOCK DIAGRAM



# TC55257AP-10/APL-10/AP-12/APL-12

## TC55257AF-10/AFL-10/AF-12/AFL-12

### OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	L	H	D <sub>OUT</sub>	I <sub>DDO</sub>
Write	L	*	L	D <sub>IN</sub>	I <sub>DDO</sub>
Output Deselect	L	H	H	High-Z	I <sub>DDO</sub>
Standby	H	*	*	High-Z	I <sub>DDS</sub>

\*) H or L

### MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.3 ~ 7.0	V
V <sub>IN</sub>	Input Voltage	-0.3* ~ 7.0	V
V <sub>I/O</sub>	Input and Output Voltage	-0.5 ~ V <sub>DD</sub> +0.5	V
P <sub>D</sub>	Power Dissipation	1.0	W
T <sub>solder</sub>	Soldering Temperature	260 ± 10	°C · sec
T <sub>strg</sub>	Storage Temperature	-55 ~ 150	°C
T <sub>opr</sub>	Operating Temperature	0 ~ 70	°C

\* ..... -3.0V at pulse width 50ns

### D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	-	0.8	V
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	-	5.5	V

**TC55257AP-10/APL-10/AP-12/APL-12**  
**TC55257AF-10/AFL-10/AF-12/AFL-12**

**D.C. and OPERATING CHARACTERISTICS** ( $T_a=0 \sim 70^\circ\text{C}$ ,  $V_{DD}=5V \pm 10\%$ )

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
$I_{IL}$	Input Leakage Current	$V_{IN}=0 \sim V_{DD}$	-	-	+1.0	$\mu\text{A}$	
$I_{OH}$	Output High Current	$V_{OH}=2.4\text{V}$	-1.0	-	-	mA	
$I_{OL}$	Output Low Current	$V_{OL}=0.4\text{V}$	4.0	-	-	mA	
$I_{LO}$	Output Leakage Current	$\overline{CE}=V_{IH}$ or $R/W=V_{IL}$ or $\overline{OE}=V_{IH}$ $V_{OUT}=0 \sim V_{DD}$	-	-	+1.0	$\mu\text{A}$	
$I_{DDO1}$	Operating Current (Read Cycle)*	$V_{DD}=5.5\text{V}$ $\overline{CE}=V_{IL}$ , $R/W=V_{IH}$ Other Input $=V_{IH}/V_{IL}$ $I_{OUT}=0\text{mA}$	$t_{\text{cycle}}=1\mu\text{s}$	-	-	10	mA
			$t_{\text{cycle}}=$ Min. cycle	-	-	45	
$I_{DDO2}$		$V_{DD}=5.5\text{V}$ $\overline{CE}=0.2\text{V}$ , $R/W=V_{DD}-0.2\text{V}$ Other Input $=V_{DD}-0.2\text{V}/0.2\text{V}$ $I_{OUT}=0\text{mA}$	$t_{\text{cycle}}=1\mu\text{s}$	-	-	5	mA
			$t_{\text{cycle}}=$ Min. cycle	-	-	40	
$I_{DDS1}$	Standby Current	$\overline{CE}=V_{IH}$	-	-	3	mA	
$I_{DDS2}$	Standby Current	$\overline{CE}=V_{DD}-0.2\text{V}$ $V_{DD}=2.0 \sim 5.5\text{V}$	TC55257APL/ AFL	-	2	100	$\mu\text{A}$
			TC55257AP/AF	-	-	1.0	mA

\* Assuming that R/W is Low for Write Cycle, the current consumption is twice as much as that when R/W is High for Write Cycle

**CAPACITANCE** ( $T_a=25^\circ\text{C}$ ,  $f=1\text{MHz}$ )

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
$C_{IN}$	Input Capacitance	$V_{IN}=\text{GND}$	10	pF
$C_{OUT}$	Output Capacitance	$V_{OUT}=\text{GND}$	10	pF

Note: This parameter periodically sampled is not 100% tested.

# TC55257AP-10/APL-10/AP-12/APL-12

## TC55257AF-10/AFL-10/AF-12/AFL-12

A.C. CHARACTERISTICS (Ta=0 ~ 70°C, V<sub>DD</sub>=5V±10%)

### Read Cycle

SYMBOL	PARAMETER	TEST CONDITION	TC55257AP-10/APL-10 AF-10/AFL-10		TC55257AF-12/APL-12 AF-12/AFL-12		UNIT
			MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	V <sub>IN</sub> =2.4V/0.6V	100	-	120	-	ns
t <sub>ACC</sub>	Address Access Time	V <sub>IH</sub> =2.2V	-	100	-	120	
t <sub>CO</sub>	$\overline{CE}$ Access Time	V <sub>IL</sub> =0.8V	-	100	-	120	
t <sub>OE</sub>	Output Enable to Output in Valid	t <sub>r</sub> , t <sub>f</sub> ≤ 5ns V <sub>OH</sub> =2.2V	-	50	-	60	
t <sub>COE</sub>	Chip Enable ( $\overline{CE}$ ) to Output in Low-Z	V <sub>OL</sub> =0.8V	10	-	10	-	
t <sub>OEE</sub>	Output Enable to Output in Low-Z	Output Load: C <sub>L</sub> (100pF) and 1 TTL Gate	5	-	5	-	
t <sub>OD</sub>	Chip Enable ( $\overline{CE}$ ) to Output in High-Z		-	50	-	60	
t <sub>ODO</sub>	Output Enable to Output in High-Z		-	40	-	50	
t <sub>OH</sub>	Output Data Hold Time		10	-	10	-	

### Write Cycle

SYMBOL	PARAMETER	TEST CONDITION	TC55257AP-10/APL-10 AF-10/AFL-10		TC55257AF-12/APL-12 AF-12/AFL-12		UNIT
			MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	V <sub>IN</sub> =2.4V/0.6V	100	-	120	-	ns
t <sub>WP</sub>	Write Pulse Width	V <sub>IH</sub> =2.2V	70	-	80	-	
t <sub>CW</sub>	Chip Selection to End of Write	V <sub>IL</sub> =0.8V t <sub>r</sub> , t <sub>f</sub> ≤ 5ns	90	-	100	-	
t <sub>AS</sub>	Address Set up Time		0	-	0	-	
t <sub>WR</sub>	Write Recovery Time		10	-	10	-	
t <sub>ODW</sub>	R/W to Output High-Z		-	50	-	60	
t <sub>OEW</sub>	R/W to Output Low-Z		10	-	10	-	
t <sub>DS</sub>	Data Set up Time		40	-	50	-	
t <sub>DH</sub>	Data Hold Time		0	-	0	-	

Note: Input pulse levels=V<sub>IN</sub>

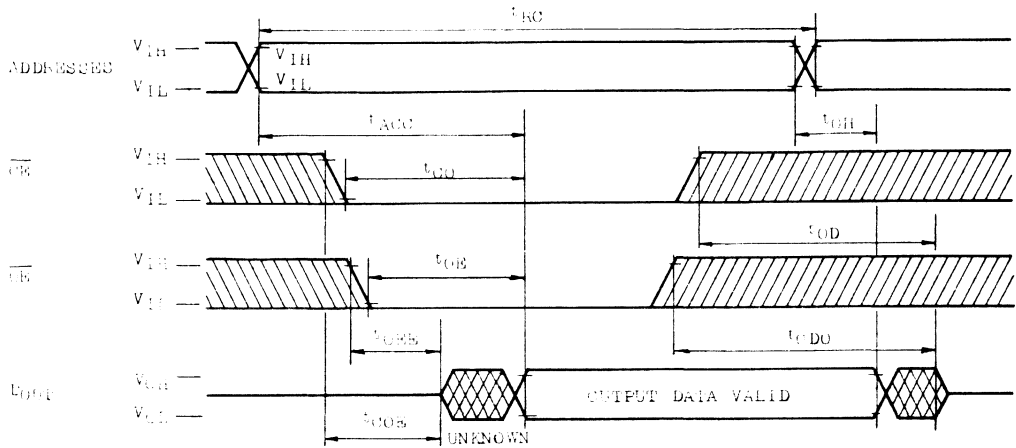
Timing Measurement Reference Levels=V<sub>IH</sub>, V<sub>IL</sub>



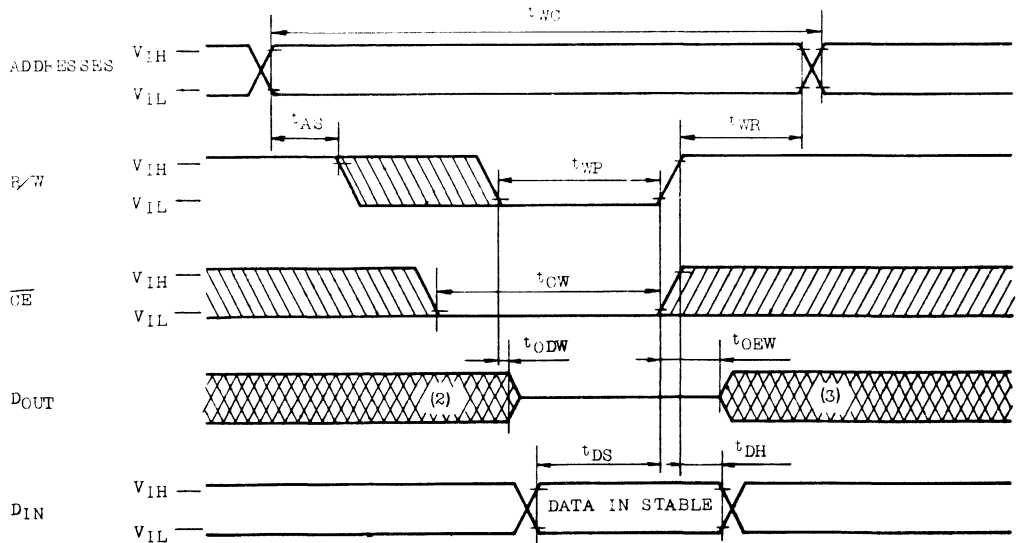
**TC55257AP-10/APL-10/AP-12/APL-12**  
**TC55257AF-10/AFL-10/AF-12/AFL-12**

TIMING WAVEFORMS

READ CYCLE (1)

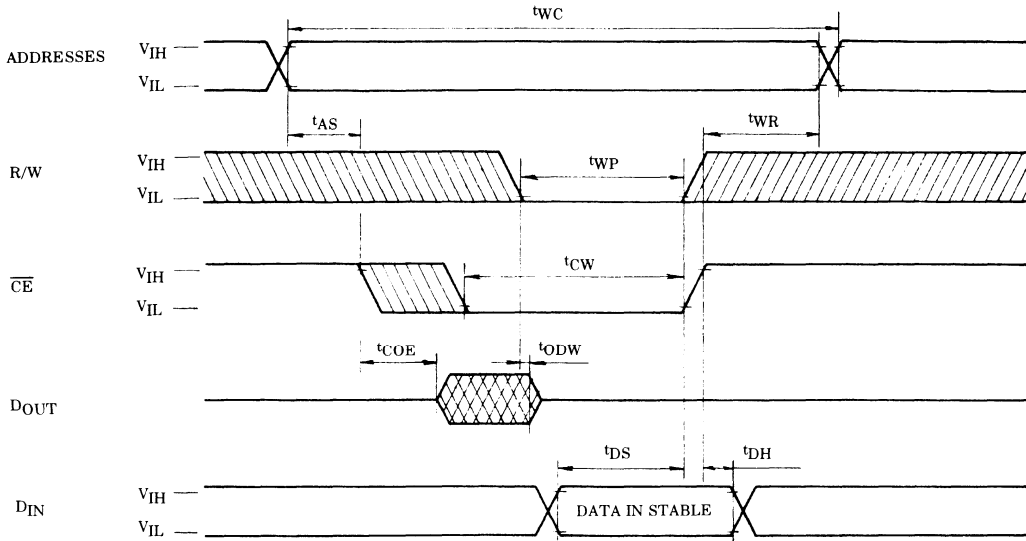


WRITE CYCLE 1 (4) (R/W Controlled Write)



**TC55257AP-10/APL-10/AP-12/APL-12**  
**TC55257AF-10/AFL-10/AF-12/AFL-12**

WRITE CYCLE 2 (4) ( $\overline{CE}$  Controlled Write)



- Note: 1. R/W is High for Read Cycle.
2. Assuming that  $\overline{CE}$  low transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
  3. Assuming that  $\overline{CE}$  High transition occurs coincident with or prior to R/W High transition, Outputs remain in a high impedance state.
  4. Assuming that  $\overline{OE}$  is High for Write Cycle, Outputs are in high impedance state during this period.

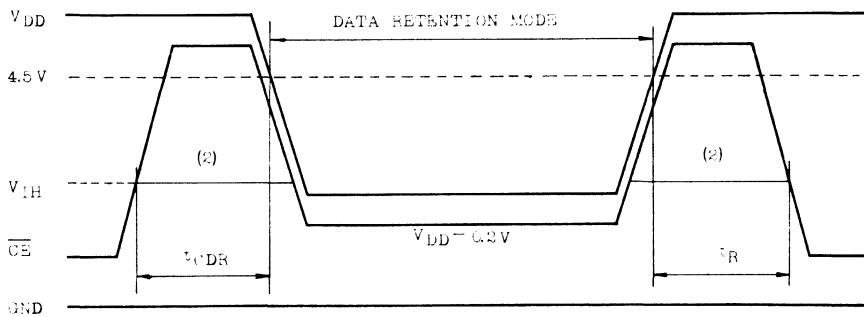
**TC55257AP-10/APL-10/AP-12/APL-12**  
**TC55257AF-10/AFL-10/AF-12/AFL-12**

**DATA RETENTION CHARACTERISTICS** (Ta=0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT	
V <sub>DH</sub>	Data Retention Supply Voltage		2.0	-	5.5	V	
I <sub>DDS2</sub>	Standby Supply Current	TC55257APL /AFL	V <sub>DD</sub> =3.0V	-	-	50	μA
			V <sub>DD</sub> =5.5V	-	-	100	
		TC55257AP/AF			-	-	1.0
t <sub>CDR</sub>	Chip Deselection to Data Retention Mode		0	-	-	μs	
t <sub>R</sub>	Recovery Time		t <sub>RC</sub> (1)	-	-		

Note (1): Read Cycle Time

**$\overline{CE}$  Controlled Data Retention Mode**

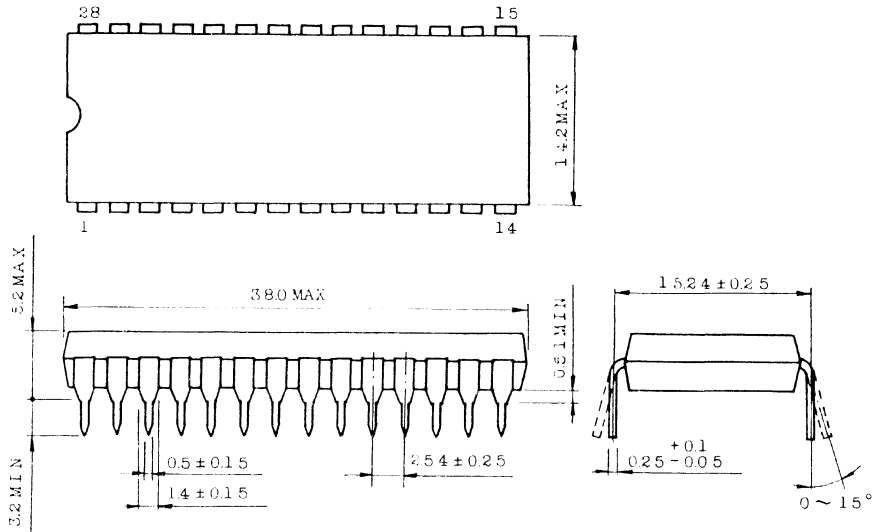


Note (2): If the V<sub>IH</sub> of  $\overline{CE}$  is 2.4V in operation, I<sub>DDS1</sub> current flows during the period that the V<sub>DD</sub> voltage is going down from 4.5V to 2.4V.

**TC55257AP-10/APL-10/AP-12/APL-12**  
**TC55257AF-10/AFL-10/AF-12/AFL-12**

DIP 28 PIN OUTLINE DRAWING (6D28A-P)

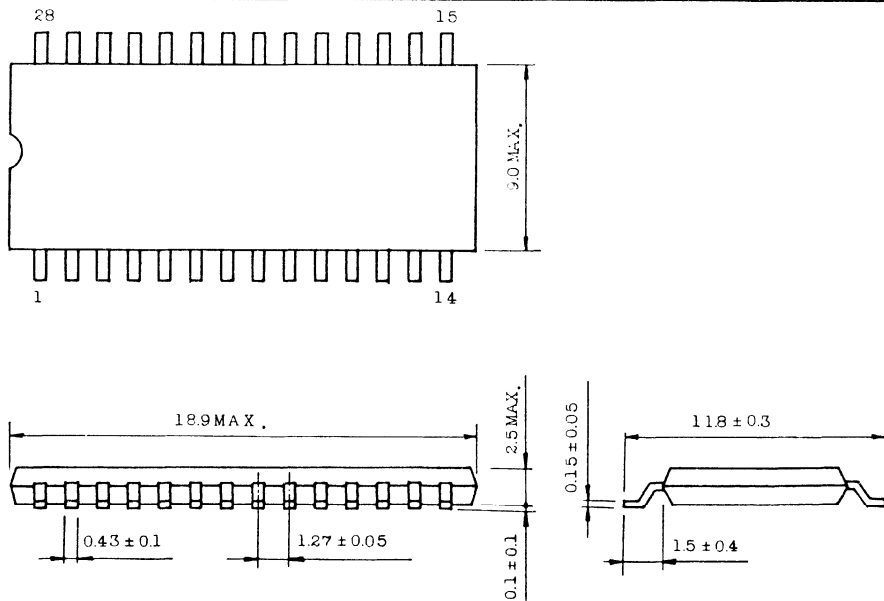
Unit in mm



Note: Lead pitch is 2.54 and tolerance is  $\pm 0.25$  against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

MFP 28 PIN OUTLINE DRAWINGS (F28GA-P)

Unit in mm



Note: Lead pitch is 1.27 and tolerance is  $\pm 0.12$  against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

# TOSHIBA MOS MEMORY PRODUCT

**32,768 WORD × 8 CMOS PSEUDO STATIC RAM**  
 SILICON MONOLITHIC  
 SILICON GATE CMOS

**TC51832P-85, TC51832P-10**  
**TC51832P-12**

## DESCRIPTION

The TC51832P is a 256K bit high speed CMOS pseudo static RAM organized as 32,768 words by 8 bits. The TC51832P utilized one transistor dynamic memory cell with CMOS peripheral circuit to provide large capacity, high speed and low power features. System oriented features include single power supply of 5V±10% tolerance. The OE/RFSH input allows two types of refresh operation — auto refresh and self refresh. The TC51832P also features static RAM like write function that the input data is written into the memory cell at the rising edge of R/W, thus being easy to interface with microprocessor. The TC51832P is pin-compatible with 256K bit CMOS static RAM - TC55257P and is moulded a standard 0.6 inch width plastic DIP.

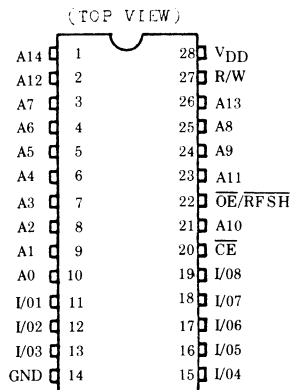
## FEATURES

- Organization: 32,768 word × 8 bit
- Fast Access Time and Cycle Time
- Single Power Supply: 5V±10%
- Static RAM like Write Function
- All inputs and outputs: TTL Compatible

	TC51832P-85	TC51832P-10	TC51832P-12
t <sub>CEA</sub> $\overline{CE}$ Access Time	35ns	100ns	120ns
t <sub>OEA</sub> $\overline{OE}$ Access Time	35ns	40ns	50ns
ERC Cycle Time	135ns	160ns	190ns

- Low Power Dissipation
  - Operating : 303mW(TC51832P-85)
  - 248mW(TC51832P-10)
  - 220mW(TC51832P-12)
- Standby : 5.5mW
- Self Refresh: 5.5mW
- Two types of Refresh Operation Capability
  - Auto Refresh
  - Self Refresh
- Pin Compatible with 256K bit CMOS Static RAM TC55257P

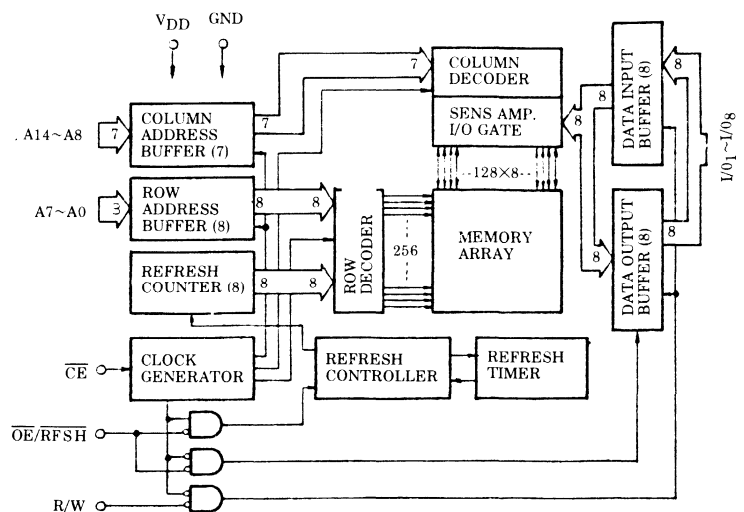
## PIN CONNECTION



## PIN NAMES

A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE/RFSH}$	Output Enable/Refresh Input
$\overline{CE}$	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V <sub>DD</sub>	Power (+5V)
GND	Ground

## BLOCK DIAGRAM



# TC51832P-85, TC51832P-10 TC51832P-12

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTES
V <sub>IN</sub>	Input Voltage	-1.0 ~ 7.0	V	1
V <sub>OUT</sub>	Output Voltage	-1.0 ~ 7.0	V	
V <sub>DD</sub>	Power Supply Voltage	-1.0 ~ 7.0	V	
T <sub>OPR</sub>	Operating Temperature	0 ~ 70	°C	
T <sub>STG</sub>	Storage Temperature	-55 ~ 150	°C	
T <sub>SOLDER</sub>	Soldering Temperature · Time	260 · 10	°C · sec	
P <sub>D</sub>	Power Dissipation	600	mW	
I <sub>OUT</sub>	Short Circuit Output Current	50	mA	

## D.C. RECOMMENDED OPERATING CONDITIONS (Ta=0 ~ 70°C)

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT	NOTES
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V	2
V <sub>IH</sub>	Input High Voltage	2.4	-	6.5	V	
V <sub>IL</sub>	Input low Voltage	-1.0	-	0.8	V	

## D.C. ELECTRICAL CHARACTERISTICS (V<sub>DD</sub>=5V±10%, Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES	
I <sub>DDO</sub>	OPERATING CURRENT	TC51832P-85	-	55	mA	3,4
	Average Power Supply Operating Current ( $\overline{CE}$ , Address Cycling: $t_{RC}=t_{RC\ MIN}$ )	TC51832P-10	-	45		
		TC51832P-12	-	40		
I <sub>DDSI</sub>	STANDBY CURRENT 1 Power Supply Standby Current, TTL Level Input ( $\overline{CE}=\overline{OE}/\overline{RFSH}=V_{IH}$ )	-	1	mA		
I <sub>DDF</sub>	SELF REFRESH CURRENT Average Power Supply Self Refresh Current ( $\overline{CE}=V_{DD}-0.2V$ , $\overline{OE}/\overline{RFSH}=0.2V$ )	-	1	mA		
I <sub>I(L)</sub>	INPUT LEAKAGE CURRENT Input Leakage Current, any Input ( $0V \leq V_{IN} \leq V_{DD}$ , All Other Inputs not under Test=0V)	-10	10	μA		
I <sub>O(L)</sub>	OUTPUT LEAKAGE CURRENT (D <sub>OUT</sub> is disable, $0V \leq V_{OUT} \leq V_{DD}$ )	-10	10	μA		
V <sub>OH</sub>	OUTPUT HIGH LEVEL Output "H" Level Voltage (I <sub>OUT</sub> =-5mA)	2.4	-	V		
V <sub>OL</sub>	OUTPUT LOW LEVEL Output "L" Level Voltage (I <sub>OUT</sub> =4.2mA)	-	0.4	V		

# TC51832P-85, TC51832P-10 TC51832P-12

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V<sub>DD</sub>=5V±10%, T<sub>a</sub>=0~70°C) (Notes 5, 6, 7, 8, 9)

SYMBOL	PARAMETER	TC51832P-85		TC51832P-10		TC51832P-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t <sub>RC</sub>	Random Read or Write Cycle Time	135	-	160	-	190	-	ns	
t <sub>RW</sub>	Read Write Cycle Time	200	-	240	-	280	-	ns	
t <sub>CE</sub>	$\overline{CE}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t <sub>P</sub>	$\overline{CE}$ Precharge Time	40	-	50	-	60	-	ns	
t <sub>CEA</sub>	$\overline{CE}$ Access Time	-	85	-	100	-	120	ns	
t <sub>OEA</sub>	$\overline{OE}$ Access Time	-	35	-	40	-	50	ns	
t <sub>CLZ</sub>	$\overline{CE}$ to Output in Low-Z	10	-	10	-	10	-	ns	
t <sub>OLZ</sub>	$\overline{OE}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t <sub>MLZ</sub>	R/W to Output in Low-Z	0	-	0	-	0	-	ns	
t <sub>CHZ</sub>	$\overline{CE}$ to Output in High-Z	0	20	0	30	0	30	ns	10
t <sub>OHZ</sub>	$\overline{OE}$ to Output in High-Z	0	20	0	30	0	30	ns	10
t <sub>MHZ</sub>	R/W to Output in High-Z	0	20	0	30	0	30	ns	10
t <sub>OHC</sub>	$\overline{OE}$ Hold Time Referenced to $\overline{CE}$	0	-	0	-	0	-	ns	
t <sub>OSC</sub>	$\overline{OE}$ Set-Up Time Referenced to $\overline{CE}$	10	-	10	-	10	-	ns	
t <sub>RCS</sub>	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t <sub>RCH</sub>	Read Command Hold Time	0	-	0	-	0	-	ns	
t <sub>WP</sub>	Write Pulse Width	60	-	70	-	85	-	ns	
t <sub>WCH</sub>	Write Command Hold Time	60	-	70	-	85	-	ns	
t <sub>CWL</sub>	Write Command to $\overline{CE}$ Lead Time	60	-	70	-	85	-	ns	
t <sub>DSW</sub>	Data Set-Up Time Referenced to R/W	35	-	40	-	50	-	ns	11
t <sub>DSC</sub>	Data Set-Up Time Referenced to $\overline{CE}$	35	-	40	-	50	-	ns	11
t <sub>DHW</sub>	Data Hold Time Referenced to R/W	0	-	0	-	0	-	ns	11
t <sub>DHC</sub>	Data Hold Time Referenced to $\overline{CE}$	0	-	0	-	0	-	ns	11
t <sub>ASC</sub>	Address Set-Up Time	0	-	0	-	0	-	ns	12
t <sub>AHC</sub>	Address Hold Time	20	-	25	-	30	-	ns	12
t <sub>FC</sub>	Auto Refresh Cycle Time	135	-	160	-	190	-	ns	
t <sub>RFD</sub>	$\overline{CE}$ to $\overline{RFSH}$ Delay Time	40	-	50	-	60	-	ns	

**TC51832P-85, TC51832P-10  
TC51832P-12**

(Continued)

SYMBOL	PARAMETER	TC51832P-85		TC51832P-10		TC51832P-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$t_{FAP}$	$\overline{RFSH}$ Pulse Width (Auto Refresh Cycle)	80	8,000	80	8,000	80	8,000	ns	13
$t_{FP}$	$\overline{RFSH}$ Precharge Time	30	-	30	-	30	-	ns	13
$t_{FCE}$	$\overline{RFSH}$ Active to $\overline{CE}$ Delay Time	160	-	190	-	225	-	ns	13
$t_{FSR}$	$\overline{RFSH}$ Precharge to $\overline{CE}$ Delay Time (Auto Refresh Cycle)	65	-	80	-	95	-	ns	13
$t_{FAS}$	$\overline{RFSH}$ Pulse Width (Self Refresh Cycle)	8,000	-	8,000	-	8,000	-	ns	13
$t_{FRS}$	$\overline{RFSH}$ Precharge to $\overline{CE}$ Delay Time (Self Refresh Cycle)	160	-	190	-	225	-	ns	13
$t_{FST}$	$\overline{RFSH}$ Set-Up Time (Refresh Counter Test Cycle)	10	30	10	30	10	30	ns	
$t_{FHT}$	$\overline{RFSH}$ Hold Time (Refresh Counter Test Cycle)	65	8,000	65	8,000	65	8,000	ns	
$t_{REF}$	Refresh Period	-	4	-	4	-	4	ms	
$t_T$	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	



# TC51832P-85, TC51832P-10 TC51832P-12

CAPACITANCE ( $V_{DD}=5V\pm 10\%$ ,  $f=1\text{MHz}$ ,  $T_a=0\sim 70^\circ\text{C}$ )

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0 ~ A14)	-	5	pF
CI2	Input Capacitance ( $\overline{CE}$ , $\overline{OE}/\overline{RFSH}$ , R/W)	-	7	pF
CIO	Input/Output Capacitance (I/O1 ~ I/O8)	-	7	pF

NOTES:

- 1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are reference to GND.
- 3)  $I_{DDO}$  depend on cycle rate.
- 4)  $I_{DDO}$  depend on output loading. Specified value are obtained with the output open.
- 5) An initial pause of 1ms with high  $\overline{CE}$  and high  $\overline{OE}/\overline{RFSH}$  is required after power-up before proper device operation is achieved.
- 6) AC measurements assume  $t_T=5\text{ns}$ .
- 7)  $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- 8) Measured with a load equivalent to 2 TTL loads and 100pF.
- 9) The  $\overline{OE}/\overline{RFSH}$  input operates as the output enable input( $\overline{OE}$ ) and refresh control input( $\overline{RFSH}$ ) under the condition of that  $\overline{CE}=V_{IL}$  and  $\overline{OE}=V_{IH}$ , respectively.
- 10)  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$  define the time at which the output achieves the open circuit condition and is not reference to output voltage levels.
- 11) In write cycles, the input data is latched at the earlier of R/W or  $\overline{CE}$  rising edge. Therefore the input data must be valid during set-up time( $t_{DSW}$ ,  $t_{DSC}$ ) and hold time( $t_{DHW}$ ,  $t_{DHC}$ ).
- 12) All address are latched at the falling edge of  $\overline{CE}$ . Therefore must be valid during  $t_{ASC}$  and  $t_{AHC}$ .
- 13) Two refresh operation - auto refresh and self refresh are determined by the  $\overline{OE}/\overline{RFSH}$  pulse width under the condition of  $\overline{CE}=V_{IH}$ .

Auto refresh:  $\overline{OE}/\overline{RFSH}$  pulse width  $\leq t_{FAP}(\text{max.})$

Self refresh:  $\overline{OE}/\overline{RFSH}$  pulse width  $\geq t_{FAS}(\text{min.})$

The following timing parameter must be kept before device proper operation is achieved after refresh.

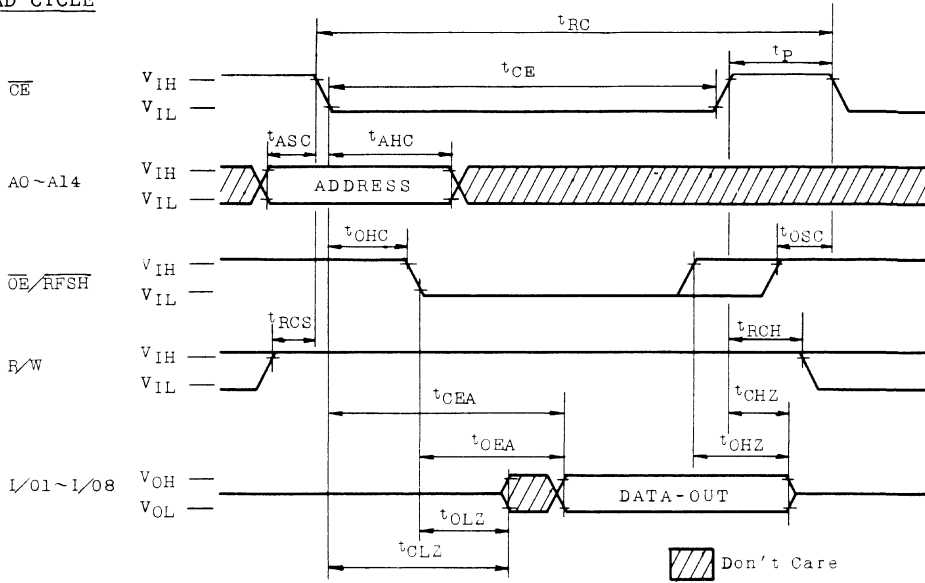
Auto refresh:  $t_{FCE}$  and  $t_{FSR}$

Self refresh:  $t_{FRS}$

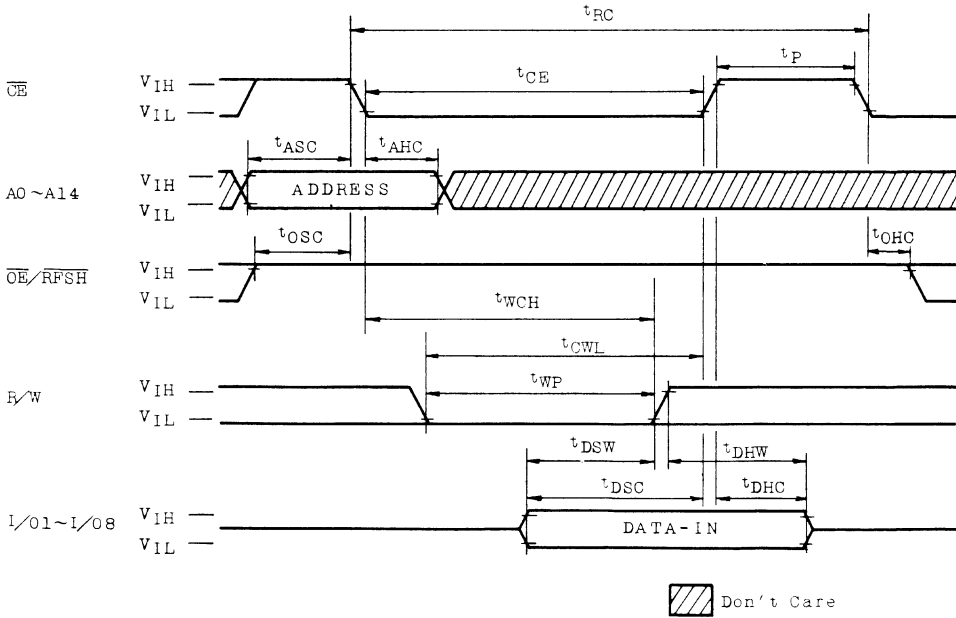
# TC51832P-85, TC51832P-10 TC51832P-12

## TIMING CHART

### READ CYCLE

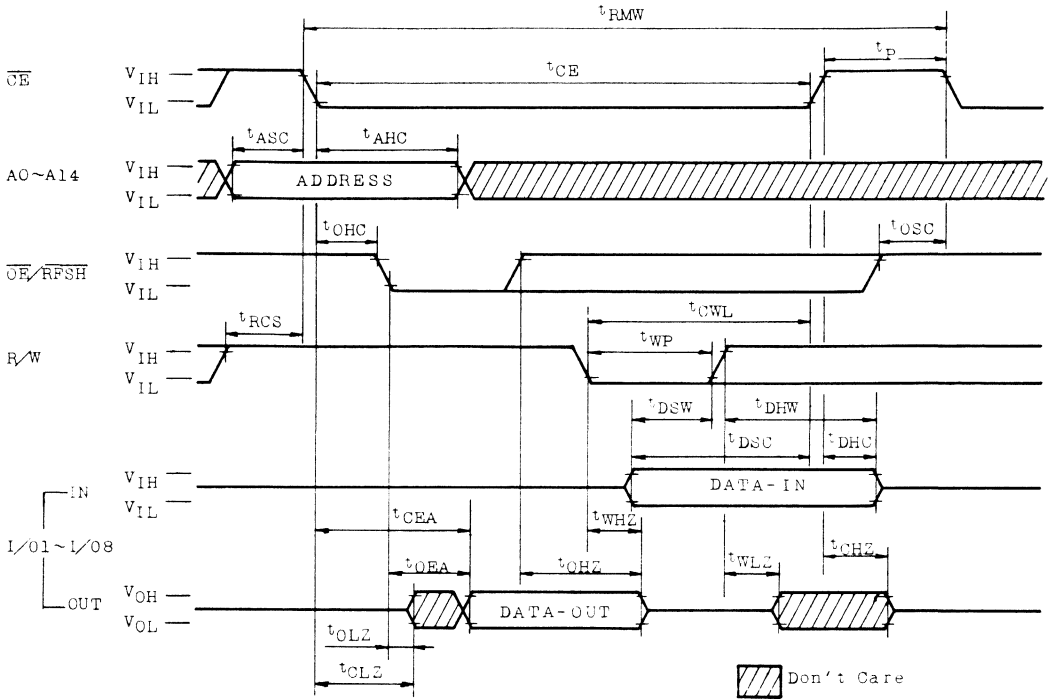


### WRITE CYCLE

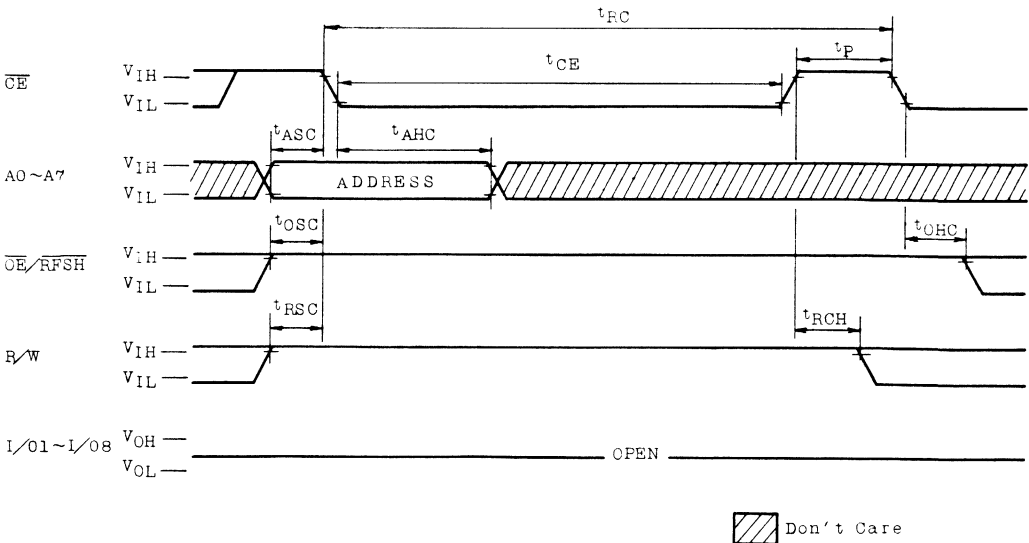


# TC51832P-85, TC51832P-10 TC51832P-12

## READ WRITE CYCLE

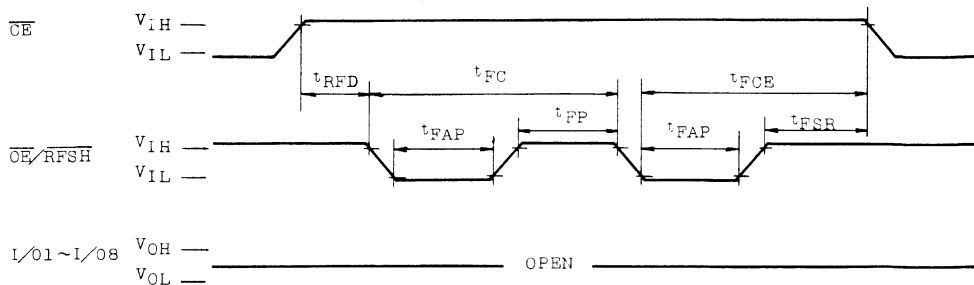


## $\overline{CE}$ ONLY REFRESH CYCLE



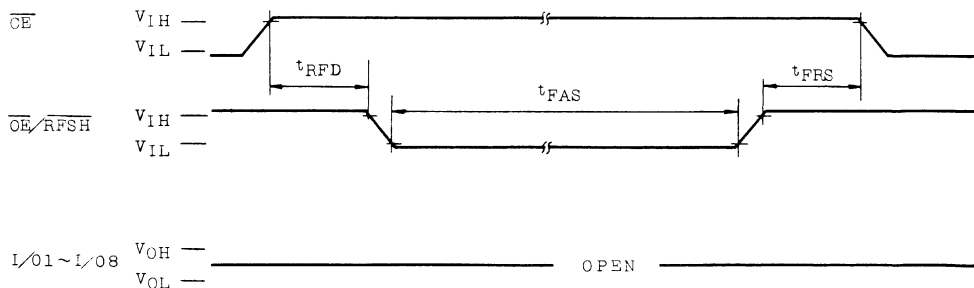
# TC51832P-85, TC51832P-10 TC51832P-12

## AUTO REFRESH CYCLE



Note) A0~A14, R/W = Don't Care

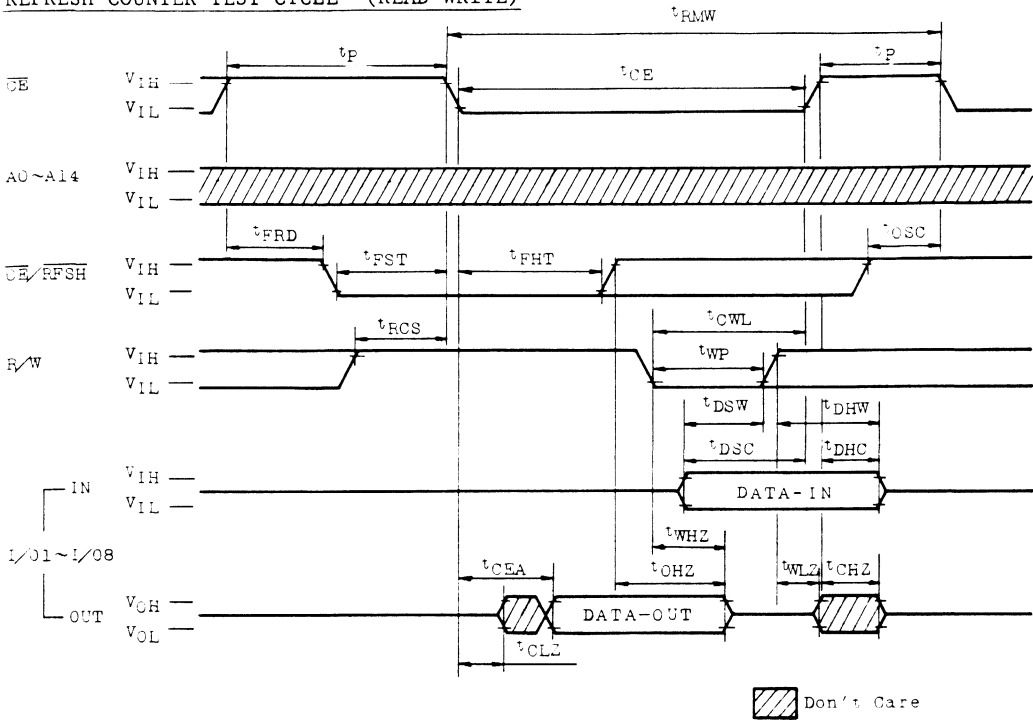
## SELF REFRESH CYCLE



Note) A0~A14, R/W = Don't Care

# TC51832P-85, TC51832P-10 TC51832P-12

REFRESH COUNTER TEST CYCLE (READ WRITE)



## REFRESH COUNTER TEST

The internal refresh operation of TC51832P can be tested by REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and fixed zero as column address.

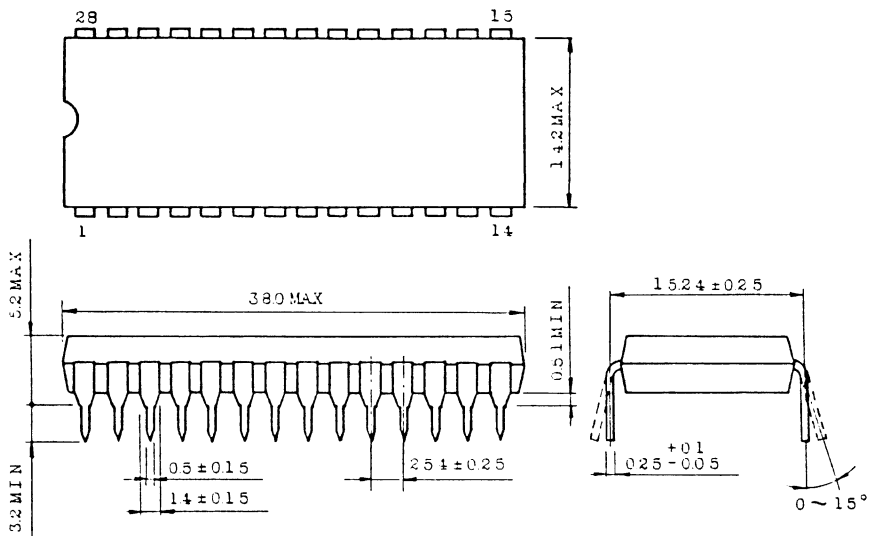
The test procedure is as follows.

- ① Write "0" into all the memory cells at normal write mode.
- ② Read "0" out and write "1" in each cell by performing REFRESH COUNTER TEST.  
Repeat this operation 256 times.
- ③ Check "1" out of 256 bits at normal read mode, which was written at ②
- ④ Read "1" out and write "0" in each cell by performing REFRESH COUNTER TEST.  
Repeat this operation 256 times.
- ⑤ Check "0" out of 256 bits at normal read mode, which was written at ④
- ⑥ Perform the above ① to ⑤ the complement data.

**TC51832P-85, TC51832P-10  
TC51832P-12**

OUTLINE DRAWINGS (6D28A-P)

Unit in mm



NOTES: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads. All dimensions are in millimeters.

# TOSHIBA MOS MEMORY PRODUCT

**32,768 WORD × 8 CMOS PSEUDO STATIC RAM**  
 SILICON MONOLITHIC  
 SILICON GATE CMOS

**TC51832PL-85, TC51832PL-10**  
**TC51832PL-12**

## DESCRIPTION

The TC51832PL is a 256K bit high speed CMOS pseudo static RAM organized as 32,768 words by 8 bits. The TC51832PL utilized one transistor dynamic memory cell with CMOS peripheral circuit to provide large capacity, high speed and low power features. System oriented features include single power supply of 5V±10% tolerance. The  $\overline{OE}/\overline{RFSH}$  input allows two types of refresh operation — auto refresh and self refresh. The TC51832PL also features static RAM like write function that the input data is written into the memory cell at the rising edge of R/W, thus being easy to interface with microprocessor. The TC51832PL is a pin-compatible with 256K bit CMOS static RAM - TC55257P and is moulded a standard 0.6 inch width plastic DIP.

## FEATURES

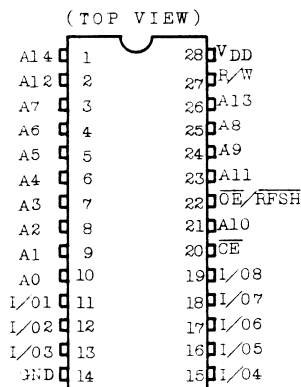
- Organization: 32,768 word 8 bit
- Fast Access Time and Cycle Time

	TC51832PL-85	TC51832PL-10	TC51832PL-12
$t_{CEA} \overline{CE}$ Access Time	35ns	100ns	120ns
$t_{OEA} \overline{OE}$ Access Time	35ns	40ns	50ns
$t_{RC}$ Cycle Time	135ns	160ns	190ns

- Single Power Supply: 5V±10%
- Static RAM like Write Function

- All inputs and outputs: TTL Compatible
- Low Power Dissipation
  - Operating : 303mW(TC51832PL-85)
  - 248mW(TC51832PL-10)
  - 220mW(TC51832PL-12)
  - Standby : 1.1mW
  - Self Refresh: 1.1mW
- Two types of Refresh Operation Capability
  - Auto Refresh
  - Self Refresh
- Pin compatible with 256K bit CMOS Static RAM TC55257P

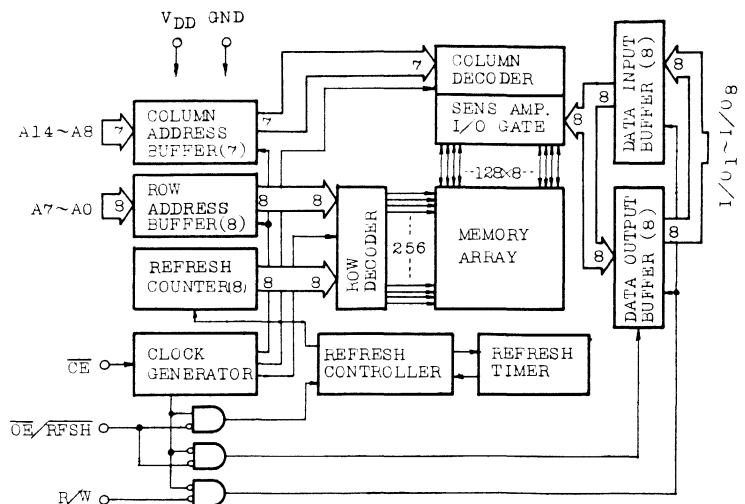
## PIN CONNECTION



## PIN NAMES

A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}/\overline{RFSH}$	Output Enable/Refresh Input
$\overline{CE}$	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V <sub>DD</sub>	Power (+5V)
GND	Ground

## BLOCK DIAGRAM



# TC51832PL-85, TC51832PL-10 TC51832PL-12

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTES
V <sub>IN</sub>	Input Voltage	-1.0 ~ 7.0	V	1
V <sub>OUT</sub>	Output Voltage	-1.0 ~ 7.0	V	1
V <sub>DD</sub>	Power Supply Voltage	-1.0 ~ 7.0	V	1
T <sub>OPR</sub>	Operating Temperature	0 ~ 70	°C	1
T <sub>STG</sub>	Storage Temperature	-55 ~ 150	°C	1
T <sub>SOLDER</sub>	Soldering Temperature · Time	260 · 10	°C·sec	1
P <sub>D</sub>	Power Dissipation	600	mW	1
I <sub>OUR</sub>	Short Circuit Output Current	50	mA	1

## D.C. RECOMMENDED OPERATING CONDITIONS (Ta=0 ~ 70°C)

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT	NOTES
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V	2
V <sub>IH</sub>	Input High Voltage	2.4	-	6.5	V	2
V <sub>IL</sub>	Input Low Voltage	-1.0	-	0.8	V	2

## D.C. ELECTRICAL CHARACTERISTICS (V<sub>DD</sub>=5V±10%, Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES	
I <sub>DDO</sub>	OPERATING CURRENT	TC51832PL-85	-	55	mA	3, 4
	Average Power Supply Operating Current ( $\overline{CE}$ , Address Cycling: $t_{RC}=t_{RC\ MIN}$ )	TC51832PL-10	-	45		
		TC51832PL-12	-	40		
I <sub>DD1</sub>	STANDBY CURRENT 1 Power Supply Standby Current, TTL Level Input ( $\overline{CE}=\overline{OE}/\overline{RFSH}=V_{IH}$ )	-	1	mA		
I <sub>DD2</sub>	STANDBY CURRENT 2 Power Supply Standby Current, CMOS Level Input ( $\overline{CE}=\overline{OE}/\overline{RFSH}=V_{DD}-0.2V$ )	-	0.2	mA		
I <sub>DDF</sub>	SELF REFRESH CURRENT Average Power Supply Self Refresh Current ( $\overline{CE}=V_{DD}-0.2V$ , $\overline{OE}/\overline{RFSH}=0.2V$ )	-	0.2	mA		
I <sub>I(L)</sub>	INPUT LEAKAGE CURRENT Input Leakage Current, any Input ( $0V \leq V_{IN} \leq V_{DD}$ , All Other Inputs not under Test=0V)	-10	10	μA		
I <sub>O(L)</sub>	OUTPUT LEAKAGE CURRENT (DOUT is disable, $0V \leq V_{OUT} \leq V_{DD}$ )	-10	10	μA		
V <sub>OH</sub>	OUTPUT HIGH LEVEL Output "H" Level Voltage (I <sub>OUT</sub> =-5mA)	2.4	-	V		
V <sub>OL</sub>	OUTPUT LOW LEVEL Output "L" Level Voltage (I <sub>OUT</sub> =4.2mA)	-	0.4	V		



# TC51832PL-85, TC51832PL-10 TC51832PL-12

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V<sub>DD</sub>=5V±10%, T<sub>a</sub>=0~70°C) (Notes 5, 6, 7, 8, 9)

SYMBOL	PARAMETER	TC51832PL-85		TC51832PL-10		TC51832PL-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t <sub>RC</sub>	Random Read or Write Cycle Time	135	-	160	-	190	-	ns	
t <sub>RMW</sub>	Read Write Cycle Time	200	-	240	-	280	-	ns	
t <sub>CE</sub>	$\overline{CE}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t <sub>P</sub>	$\overline{CE}$ Precharge Time	40	-	50	-	60	-	ns	
t <sub>CEA</sub>	$\overline{CE}$ Access Time	-	85	-	100	-	120	ns	
t <sub>OEa</sub>	$\overline{OE}$ Access Time	-	35	-	40	-	50	ns	
t <sub>CLZ</sub>	$\overline{CE}$ to Output in Low-Z	10	-	10	-	10	-	ns	
t <sub>OLZ</sub>	$\overline{OE}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t <sub>WLZ</sub>	R/W to Output in Low-Z	0	-	0	-	0	-	ns	
t <sub>CHZ</sub>	$\overline{CE}$ to Output in High-Z	0	20	0	30	0	30	ns	10
t <sub>OHZ</sub>	$\overline{OE}$ to Output in High-Z	0	20	0	30	0	30	ns	10
t <sub>WHZ</sub>	R/W to Output in High-Z	0	20	0	30	0	30	ns	10
t <sub>OHC</sub>	$\overline{OE}$ Hold Time Referenced to $\overline{CE}$	0	-	0	-	0	-	ns	
t <sub>OSC</sub>	$\overline{OE}$ Set-Up Time Referenced to $\overline{CE}$	10	-	10	-	10	-	ns	
t <sub>RCS</sub>	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t <sub>RCH</sub>	Read Command Hold Time	0	-	0	-	0	-	ns	
t <sub>WP</sub>	Write Pulse Width	60	-	70	-	35	-	ns	
t <sub>WCH</sub>	Write Command Hold Time	60	-	70	-	35	-	ns	
t <sub>CWL</sub>	Write Command to $\overline{CE}$ Lead Time	60	-	70	-	35	-	ns	
t <sub>DSW</sub>	Data Set-Up Time Referenced to R/W	35	-	40	-	50	-	ns	11
t <sub>DSC</sub>	Data Set-Up Time Referenced to $\overline{CE}$	35	-	40	-	50	-	ns	11
t <sub>DHW</sub>	Data Hold Time Referenced to R/W	0	-	0	-	0	-	ns	11
t <sub>DHC</sub>	Data Hold Time Referenced to $\overline{CE}$	0	-	0	-	0	-	ns	11
t <sub>ASC</sub>	Address Set-Up Time	0	-	0	-	0	-	ns	12
t <sub>AHC</sub>	Address Hold Time	20	-	25	-	30	-	ns	12
t <sub>FC</sub>	Auto Refresh Cycle Time	135	-	160	-	190	-	ns	
t <sub>RFD</sub>	$\overline{CE}$ to RFSH Delay Time	40	-	50	-	60	-	ns	

# TC51832PL-85, TC51832PL-10 TC51832PL-12

(Continued)

SYMBOL	PARAMETER	TC51832PL-85		TC51832PL-10		TC51832PL-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$t_{FAP}$	$\overline{RFSH}$ Pulse Width (Auto Refresh Cycle)	80	8,000	80	8,000	80	8,000	ns	13
$t_{FP}$	$\overline{RFSH}$ Precharge Time	30	-	30	-	30	-	ns	13
$t_{FCE}$	$\overline{RFSH}$ Active to $\overline{CE}$ Delay Time	160	-	190	-	225	-	ns	13
$t_{FSR}$	$\overline{RFSH}$ Precharge to $\overline{CE}$ Delay Time(Auto Refresh Cycle)	65	-	80	-	95	-	ns	13
$t_{FAS}$	$\overline{RFSH}$ Pulse Width (Self Refresh Cycle)	8,000	-	8,000	-	8,000	-	ns	13
$t_{FRS}$	$\overline{RFSH}$ Precharge to $\overline{CE}$ Delay Time (Self Refresh Cycle)	160	-	190	-	225	-	ns	13
$t_{FST}$	$\overline{RFSH}$ Set-Up Time (Refresh Counter Test Cycle)	10	30	10	30	10	30	ns	
$t_{FHT}$	$\overline{RFSH}$ Hold Time (Refresh Counter Test Cycle)	65	8,000	65	3,000	65	8,000	ns	
$t_{REF}$	Refresh Period	-	4	-	4	-	4	ms	
$t_T$	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

CAPACITANCE ( $V_{DD}=5V\pm 10\%$ ,  $f=1MHz$ ,  $T_a=0\sim 70^\circ C$ )

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0 ~ A14)	-	5	pF
CI2	Input Capacitance ( $\overline{CE}$ , $\overline{OE}/\overline{RFSH}$ , R/W)	-	7	pF
CIO	Input/Output Capacitance (I/O1 ~ I/O8)	-	7	pF

# TC51832PL-85, TC51832PL-10 TC51832PL-12

## NOTES:

- 1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are reference to GND.
- 3)  $I_{DDO}$  depend on cycle rate.
- 4)  $I_{DDO}$  depend on output loading. Specified value are obtained with the output open.
- 5) An initial pause of lms with high  $\overline{CE}$  and high  $\overline{OE}/\overline{RFSH}$  is required after power-up before proper device operation is achieved.
- 6) AC measurements assume  $t_T=5ns$ .
- 7)  $V_{IH}(min.)$  and  $V_{IL}(max.)$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- 8) Measured with a load equivalent to 2 TTL loads and 100pF.
- 9) The  $\overline{OE}/\overline{RFSH}$  input operates as the output enable input ( $\overline{OE}$ ) and refresh control input ( $\overline{RFSH}$ ) under the condition of that  $\overline{CE}=V_{IL}$  and  $\overline{CE}=V_{IH}$ , respectively.
- 10)  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$  define the time at which the output achieves the open circuit condition and is not reference to output voltage levels.
- 11) In write cycles, the input data is latched at the earlier of R/W or  $\overline{CE}$  rising edge. Therefore the input data must be valid during set-up time ( $t_{DSW}$ ,  $t_{DSC}$ ) and hold time ( $t_{DHW}$ ,  $t_{DHC}$ ).
- 12) All address are latched at the falling edge of  $\overline{CE}$ . Therefore must be valid during  $t_{ASC}$  and  $t_{AHC}$ .
- 13) Two refresh operation - auto refresh and self refresh are determined by the  $\overline{OE}/\overline{RFSH}$  pulse width under the condition of  $\overline{CE}=V_{IH}$ .

Auto refresh:  $\overline{OE}/\overline{RFSH}$  pulse width  $\leq t_{FAP}(max.)$

Self refresh:  $\overline{OE}/\overline{RFSH}$  pulse width  $\leq t_{FAS}(min.)$

The following timing parameter must be kept before device proper operation is achieved after refresh.

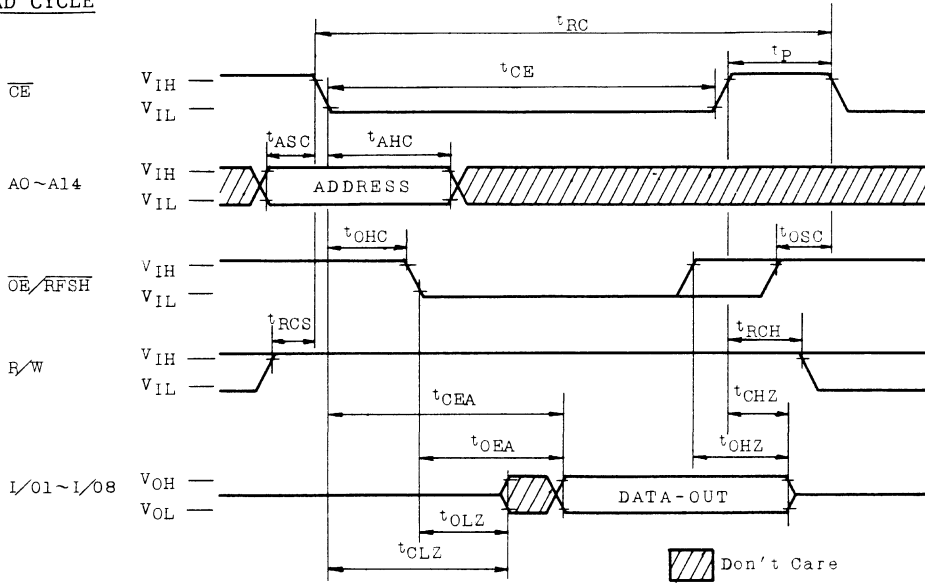
Auto refresh:  $t_{FCE}$  and  $t_{FSR}$

Self refresh:  $t_{FRS}$

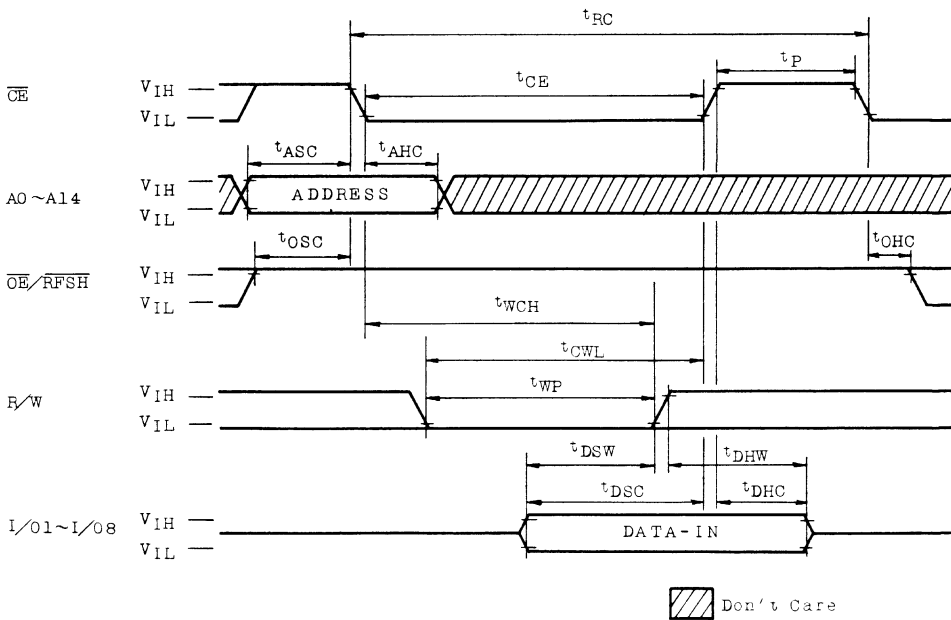
# TC51832PL-85, TC51832PL-10 TC51832PL-12

## TIMING CHART

### READ CYCLE

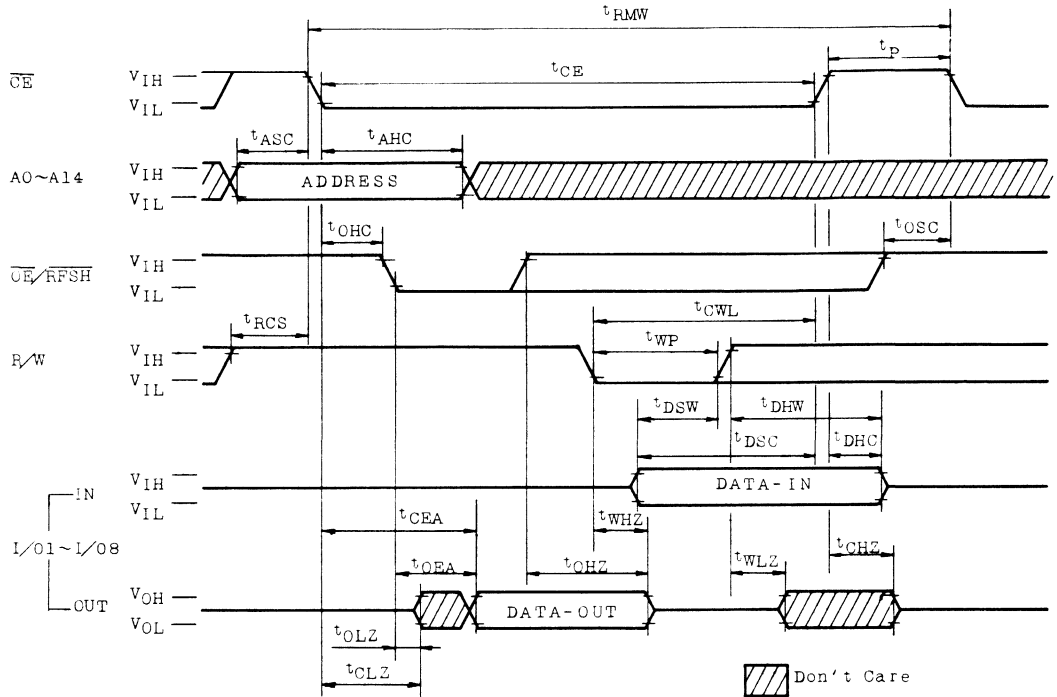


### WRITE CYCLE

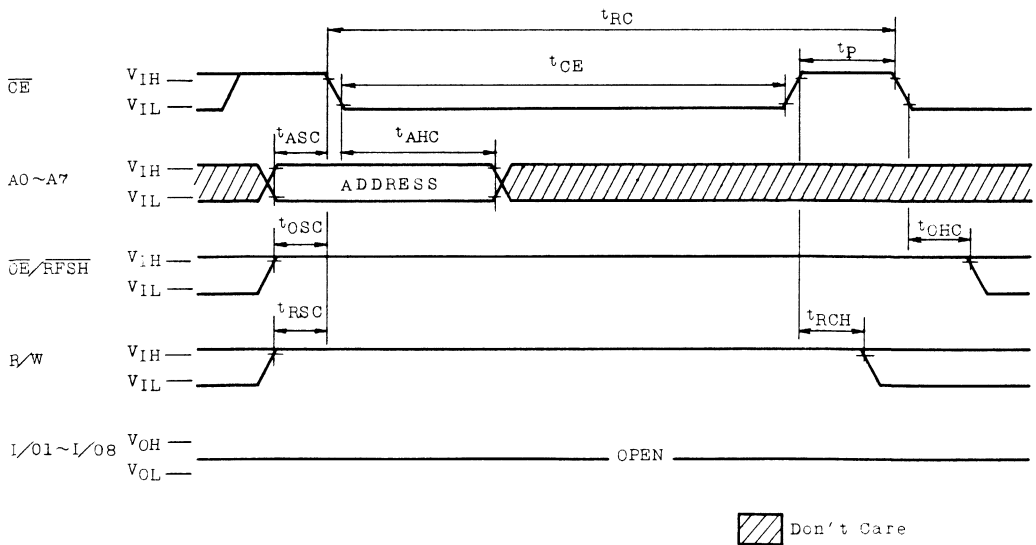


# TC51832PL-85, TC51832PL-10 TC51832PL-12

## READ WRITE CYCLE

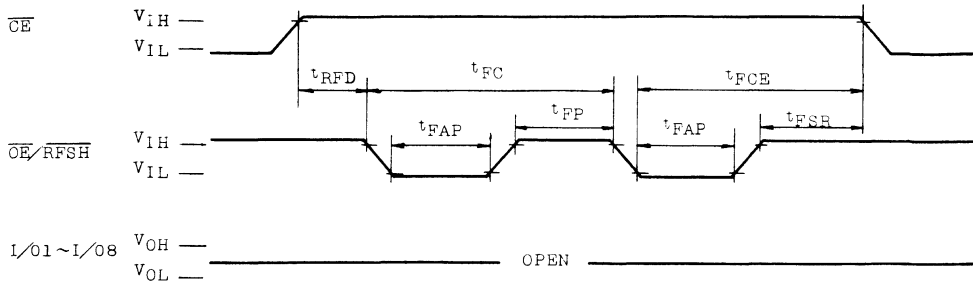


## $\overline{CE}$ ONLY REFRESH CYCLE



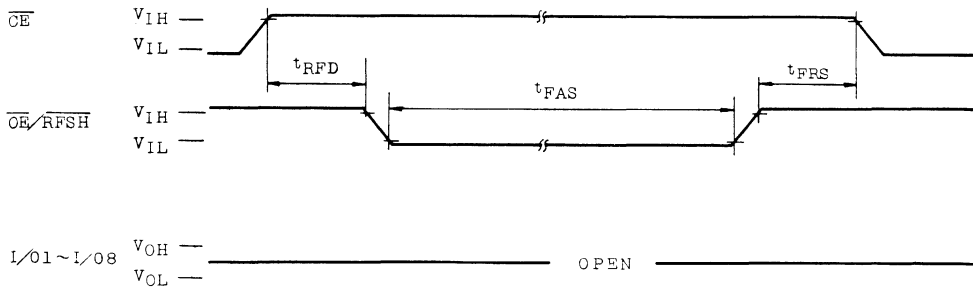
# TC51832PL-85, TC51832PL-10 TC51832PL-12

## AUTO REFRESH CYCLE



Note) A0~A14, R/W = Don't Care

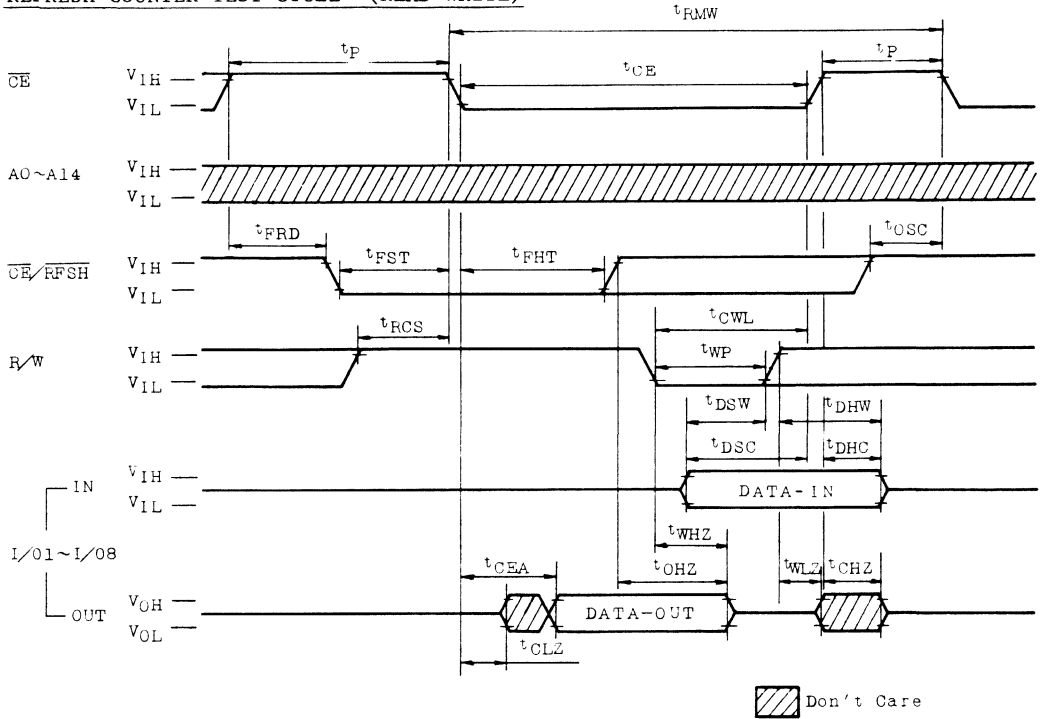
## SELF REFRESH CYCLE



Note) A0~A14, R/W = Don't Care

# TC51832PL-85, TC51832PL-10 TC51832PL-12

## REFRESH COUNTER TEST CYCLE (READ WRITE)



## REFRESH COUNTER TEST

The internal refresh operation of TC51832PL can be tested by REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and fixed zero as column address.

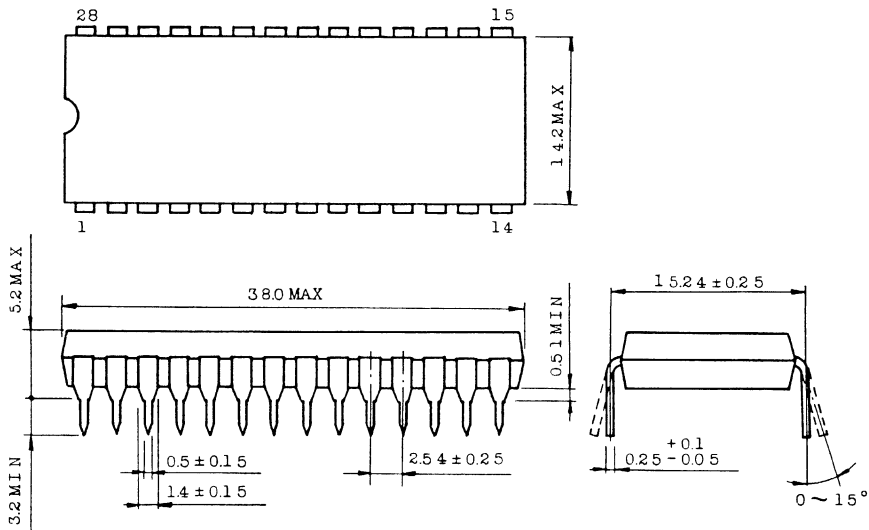
The test procedure is as follows.

- ① Write "0" into all the memory cells at normal write mode.
- ② Read "0" out and write "1" in each cell by performing REFRESH COUNTER TEST.  
Repeat this operation 256 times.
- ③ Check "1" out of 256 bits at normal read mode, which was written at ②.
- ④ Read "1" out and write "0" in each cell by performing REFRESH COUNTER TEST.  
Repeat this operation 256 times.
- ⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.
- ⑥ Perform the above ① to ⑤ the complement data.

**TC51832PL-85, TC51832PL-10  
TC51832PL-12**

OUTLINE DRAWINGS (6D28A-P)

Unit in mm



NOTES: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads. All dimensions are in millimeters.



# High Speed Static RAMs



# TOSHIBA MOS MEMORY PRODUCT

2,048 WORD × 8 BIT STATIC RAM  
 SILICON MONOLITHIC  
 N-CHANNEL SILICON GATE MOS PROCESS

**TMM2018AD-25, TMM2018AD-35**  
**TMM2018AD-45**

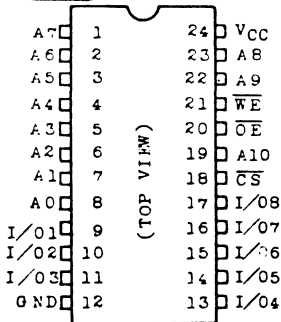
## DESCRIPTION

The TMM2018AD is a 16,384 bits high speed and low power static random access memory organized as 2,048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 25ns/35ns/45ns and maximum operating current of 150mA/135mA/135mA. When  $\overline{CS}$  goes high, the device is deselected and placed in a low power standby mode in which maximum standby current is 20mA. Thus the TMM2018AD is most suitable for use in cache memory and high speed storage. The TMM2018AD is offered in a 24 pin standard cerdip package with 0.3 inch width for high density assembly. The TMM2018AD is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

## FEATURES

- Fast access time
  - $t_{ACC}=25ns$ : TMM2018AD-25
  - $t_{ACC}=35ns$ : TMM2018AD-35
  - $t_{ACC}=45ns$ : TMM2018AD-45
- Low power dissipation
  - $I_{CC}=150mA$ : TMM2018AD-25
  - $I_{CC}=135mA$ : TMM2018AD-35
  - $I_{CC}=135mA$ : TMM2018AD-45
  - $I_{SB}=20mA$
- Single 5V power supply
- Fully static operation
- All inputs and outputs Directly TTL Compatible
- Power down feature:  $\overline{CS}=V_{IH}$
- Output buffer control:  $\overline{OE}$
- Three state outputs
- Inputs protected: All inputs protection against static charge.
- Package: 24 pins standard cerdip package, 0.3 inch width

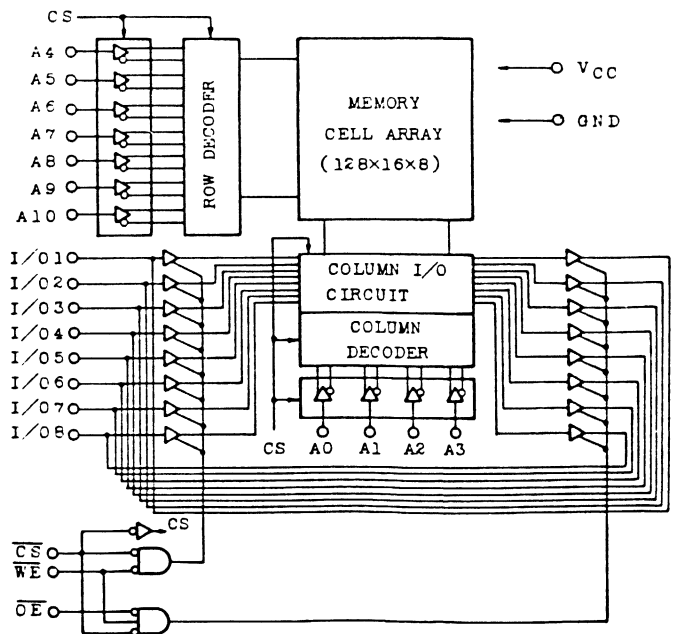
## PIN CONNECTION



## PIN NAMES

A <sub>0</sub> -A <sub>10</sub>	Address Inputs
I/O <sub>1</sub> -I/O <sub>8</sub>	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V <sub>CC</sub>	Power (+5V)
GND	Ground

## BLOCK DIAGRAM



# TMM2018AD-25, TMM2018AD-35 TMM2018AD-45

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
VCC	Power Supply Voltage	-3.5-7.0	V
VIN	Input Voltage	-3.5-7.0	V
VI/O	Input/Output Voltage	-3.5-7.0	V
Topr	Operating Temperature	0-70	°C
Tstg	Storage Temperature	-55-150	°C
Tsolder	Soldering Temperature · Time	260 · 10	°C·sec
Pd	Power Dissipation	0.9	W
IOUT	D.C. Output Current	20	mA

## D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.0	-	VCC+1.0	V
VIL	Input Low Voltage	-3.0*	-	0.8	V
VCC	Power Supply Voltage	4.5	5.0	5.5	V

\* Pulse Width: 10ns, DC: -0.5V(MIN.)

## D.C. CHARACTERISTICS (Ta=0-70°C, VCC=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT	
IIL	Input Current	VIN=0-VCC	-	±1.0	μA	
VOH	Output High Voltage	IOH=-4.0mA	2.4	-	V	
VOL	Output Low Voltage	IOL=8.0mA	-	0.4	V	
ILO	Output Leakage Current	VOUT=0-VCC, $\overline{CS}$ =VIH	-	±1.0	μA	
ICC	Operating Current	$\overline{CS}$ =VIL	-25	-	150	mA
			-35	-	135	
			-45	-	135	
ISB	Standby Current	$\overline{CS}$ =VIH	-	20	mA	
ISBP	Peak Power-on Current	$\overline{CS}$ =VCC, VCC=0-5.5V	-	40	mA	

## CAPACITANCE\* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
CIN	Input Capacitance	VIN=0V	5	PF
COUT	Output Capacitance	VOUT=0V	10	

\* Note: This parameter is periodically sampled and is not 100% tested.

# TMM2018AD-25, TMM2018AD-35 TMM2018AD-45

A.C. CHARACTERISTICS (Ta=0-70°C, VCC=5V±10%)

## READ CYCLE

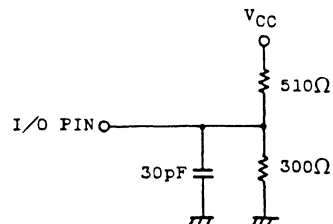
SYMBOL	PARAMETER	TMM2018AD-25		TMM2018AD-35		TMM2018AD-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	25	-	35	-	45	-	ns
t <sub>ACC</sub>	Address Access Time	-	25	-	35	-	45	
t <sub>CO</sub>	Chip Select Access Time	-	25	-	35	-	45	
t <sub>OE</sub>	Output Enable to Output Valid	-	15	-	20	-	20	
t <sub>CLZ</sub>	Chip Selection to Output in Low-Z	0	-	0	-	0	-	
t <sub>CHZ</sub>	Chip Deselection to Output in High-Z	-	15	-	20	-	20	
t <sub>OLZ</sub>	Output Enable to Output in Low-Z	0	-	0	-	0	-	
t <sub>OHZ</sub>	Output Disable to Output in High-Z	-	12	-	15	-	15	
t <sub>OH</sub>	Output Data Hold Time	5	-	5	-	5	-	
t <sub>PU</sub>	Chip Selection to Power Up Time	0	-	0	-	0	-	
t <sub>PD</sub>	Chip Deselection to Power Down Time	-	20	-	30	-	30	

## WRITE CYCLE

SYMBOL	PARAMETER	TMM2018AD-25		TMM2018AD-35		TMM2018AD-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	25	-	35	-	45	-	ns
t <sub>CW</sub>	Chip Selection to End of Write	20	-	30	-	40	-	
t <sub>AS</sub>	Address Set Up Time	0	-	0	-	0	-	
t <sub>WP</sub>	Write Pulse Width	20	-	30	-	35	-	
t <sub>WR</sub>	Write Recovery Time	0	-	0	-	0	-	
t <sub>WLZ</sub>	$\overline{WE}$ to Output in Low-Z	0	-	0	-	0	-	
t <sub>WHZ</sub>	$\overline{WE}$ to Output in High-Z	-	12	-	15	-	15	
t <sub>DS</sub>	Data Set Up Time	12	-	15	-	20	-	
t <sub>DH</sub>	Data Hold Time	0	-	0	-	0	-	

## A.C. TEST CONDITONS

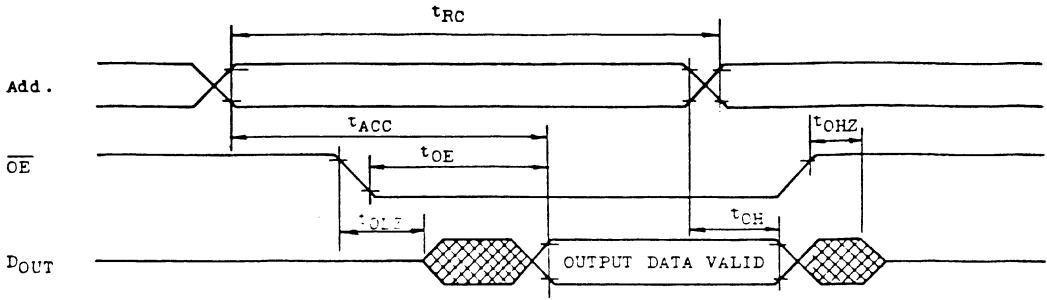
Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	2.0V/0.8V
Output Load	See Fig.1



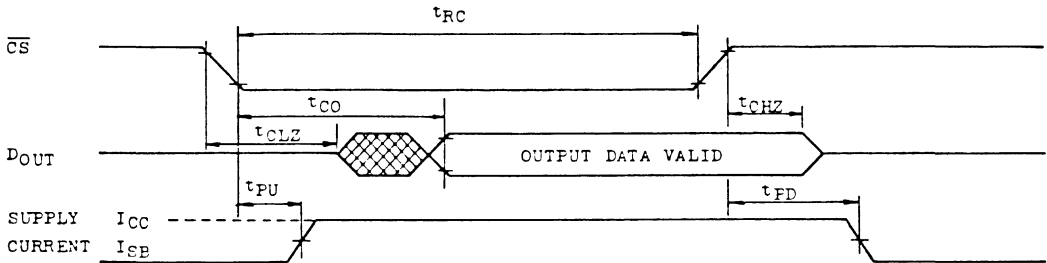
# TMM2018AD-25, TMM2018AD-35 TMM2018AD-45

## TIMING WAVEFORMS

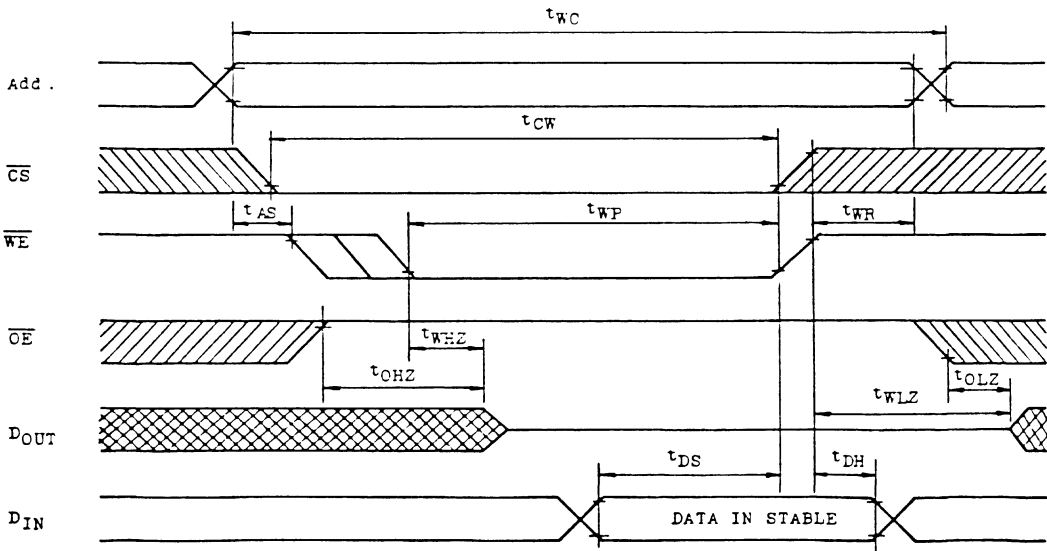
READ CYCLE 1. ( $\overline{WE}=V_{IH}, \overline{CS}=V_{IL}$ )



READ CYCLE 2. ( $\overline{WE}=V_{IH}, \overline{OE}=V_{IL}$ )

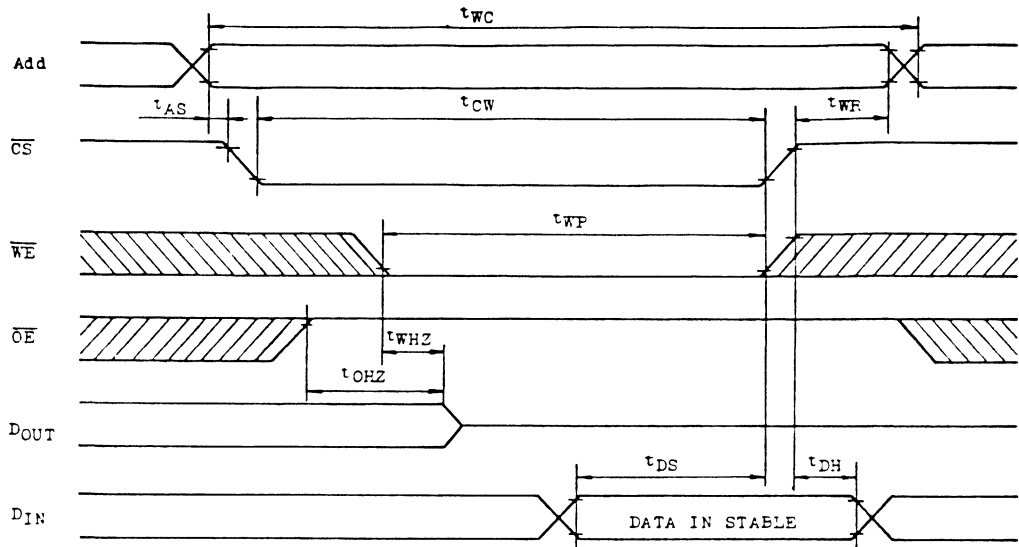


WRITE CYCLE 1.



# TMM2018AD-25, TMM2018AD-35 TMM2018AD-45

## WRITE CYCLE 2.



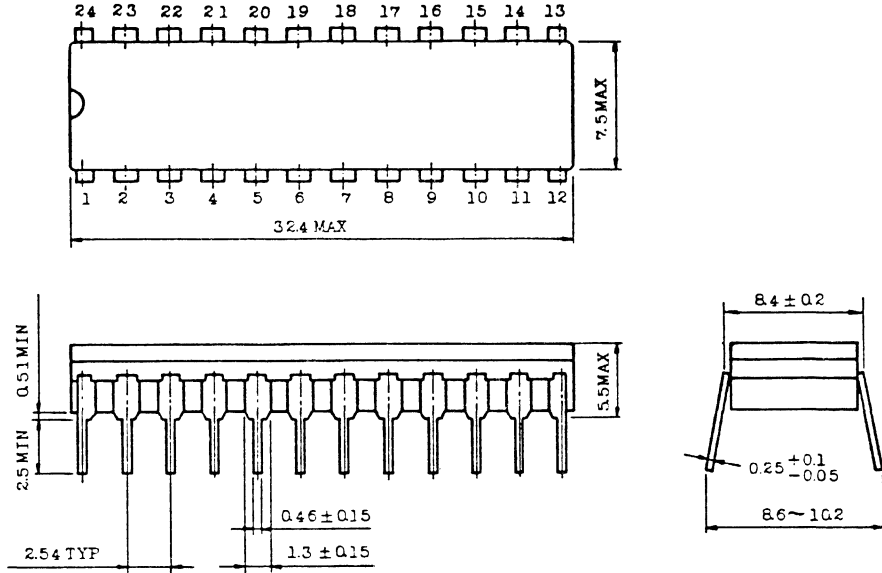
### Note:

1. In read cycle 2, all addresses are valid prior to or coincident with  $\overline{CS}$  transition low.
2. The operating temperature ( $T_a$ ) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

**TMM2018AD-25, TMM2018AD-35  
TMM2018AD-45**

OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.24 leads.



# TOSHIBA MOS MEMORY PRODUCT

2,048 WORD × 8 BIT STATIC RAM  
SILICON MONOLITHIC  
N-CHANNEL SILICON GATE MOS PROCESS

**TMM2018AP-25, TMM2018AP-35**  
**TMM2018AP-45**

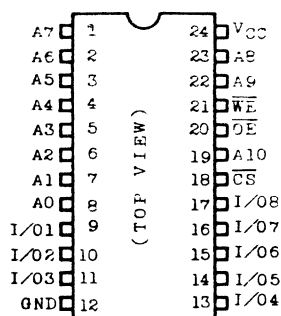
## DESCRIPTION

The TMM2018AP is a 16,384 bits high speed and low power static random access memory organized as 2,048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 25ns/35ns/45ns and maximum operating current of 150mA/135mA/135mA. When  $\overline{CS}$  goes high, the device is deselected and placed in a low power standby mode in which maximum standby current is 20mA. Thus the TMM2018AP is most suitable for use in cache memory and high speed storage. The TMM2018AP is offered in a 24 pin standard plastic package with 0.3 inch width for high density assembly. The TMM2018AP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

## FEATURES

- Fast access time
  - $t_{ACC}=25ns$ : TMM2018AP-25
  - $t_{ACC}=35ns$ : TMM2018AP-35
  - $t_{ACC}=45ns$ : TMM2018AP-45
- Low power dissipation
  - $I_{CC}=150mA$ : TMM2018AP-25
  - $I_{CC}=135mA$ : TMM2018AP-35
  - $I_{CC}=135mA$ : TMM2018AP-45
  - $I_{SB}=20mA$
- Single 5V power supply
- Fully static operation
- All inputs and outputs: Directly TTL compatible
- Power down feature:  $\overline{CS}=V_{IH}$
- Output buffer control:  $\overline{OE}$
- Three state outputs
- Inputs protected: All inputs protection against static charge.
- Package: 24 pin standard plastic package, 0.3 inch width.

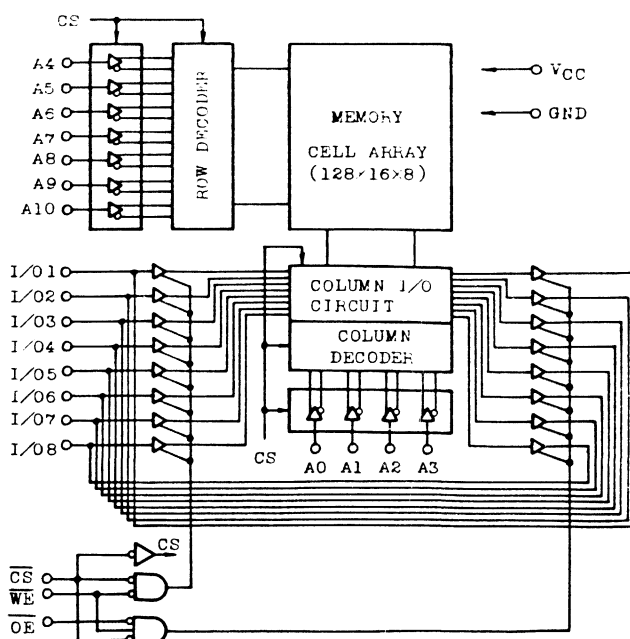
## PIN CONNECTION



## PIN NAMES

A0 ~ A10	Address Inputs
I/O1 ~ I/O8	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
VCC	Power (+5V)
GND	Ground

## BLOCK DIAGRAM



# TMM2018AP-25, TMM2018AP-35 TMM2018AP-45

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	Power Supply Voltage	-3.5 ~ 7.0	V
V <sub>IN</sub>	Input Voltage	-3.5 ~ 7.0	V
V <sub>I/O</sub>	Input/Output Voltage	-3.5 ~ 7.0	V
T <sub>opr</sub>	Operating Temperature	0 ~ 70	°C
T <sub>stg</sub>	Storage Temperature	-55 ~ 150	°C
T <sub>solder</sub>	Soldering Temperature • Time	260 • 10	°C • sec
P <sub>D</sub>	Power Dissipation	0.9	W
I <sub>OUT</sub>	D.C. Output Current	20	mA

## D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.0	-	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input Low Voltage	-3.0*	-	0.8	
V <sub>CC</sub>	Power Supply Voltage	4.5	5.0	5.5	

\* Pulse Width: 10ns, DC: -0.5V (MIN.)

## D.C. CHARACTERISTICS (Ta=0 ~ 70°C, V<sub>CC</sub>=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT	
I <sub>IL</sub>	Input Current	V <sub>IN</sub> =0 ~ V <sub>CC</sub>	-	±1.0	μA	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> =-4.0mA	2.4	-	V	
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> =8.0mA	-	0.4	V	
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> =0 ~ V <sub>CC</sub> , $\bar{CS}=V_{IH}$	-	±1.0	μA	
I <sub>CC</sub>	Operating Current	$\bar{CS}=V_{IL}$	-25	-	150	mA
			-35	-	135	
			-45	-	135	
I <sub>SB</sub>	Standby Current	$\bar{CS}=V_{IH}$	-	20	mA	
I <sub>SBP</sub>	Peak Power-on Current	$\bar{CS}=V_{CC}$ , V <sub>CC</sub> =0 ~ 5.5V	-	40		

## CAPACITANCE\* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =0V	5	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> =0V	10	

\* Note: This parameter is periodically sampled and is not 100% tested.

# TMM2018AP-25, TMM2018AP-35 TMM2018AP-45

A.C. CHARACTERISTICS (Ta=0 ~ 70°C, VCC=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TMM2018AP-25		TMM2018AP-35		TMM2018AP-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	25	-	35	-	45	-	ns
t <sub>ACC</sub>	Address Access Time	-	25	-	35	-	45	
t <sub>CO</sub>	Chip Select Access Time	-	25	-	35	-	45	
t <sub>OE</sub>	Output Enable to Output Valid	-	15	-	20	-	20	
t <sub>CLZ</sub>	Chip Selection to Output in Low-Z	0	-	0	-	0	-	
t <sub>CHZ</sub>	Chip Deselection to Output in High-Z	-	15	-	20	-	20	
t <sub>OLZ</sub>	Output Enable to Output in Low-Z	0	-	0	-	0	-	
t <sub>OHZ</sub>	Output Disable to Output in High-Z	-	12	-	15	-	15	
t <sub>OH</sub>	Output Data Hold Time	5	-	5	-	5	-	
t <sub>PU</sub>	Chip Selection to Power Up Time	0	-	0	-	0	-	
t <sub>PD</sub>	Chip Deselection to Power Down Time	-	20	-	30	-	30	

Write Cycle

SYMBOL	PARAMETER	TMM2018AP-25		TMM2018AP-35		TMM2018AP-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	25	-	35	-	45	-	ns
t <sub>CW</sub>	Chip Selection to End of Write	20	-	30	-	40	-	
t <sub>AS</sub>	Address Set Up Time	0	-	0	-	0	-	
t <sub>WP</sub>	Write Pulse Width	20	-	30	-	35	-	
t <sub>WR</sub>	Write Recovery Time	0	-	0	-	0	-	
t <sub>WLZ</sub>	$\overline{WE}$ to Output in Low-Z	0	-	0	-	0	-	
t <sub>WHZ</sub>	$\overline{WE}$ to Output in High-Z	-	12	-	15	-	15	
t <sub>DS</sub>	Data Set Up Time	12	-	15	-	20	-	
t <sub>DH</sub>	Data Hold Time	0	-	0	-	0	-	

A.C. TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	2.0V/0.8V
Output Load	See Fig.1

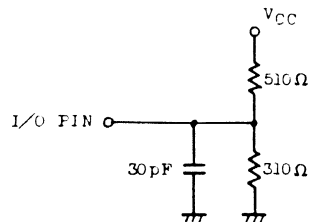
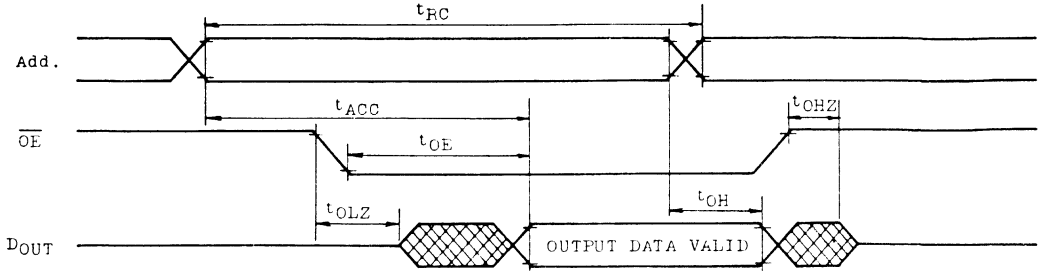


Fig.1 OUTPUT LOAD

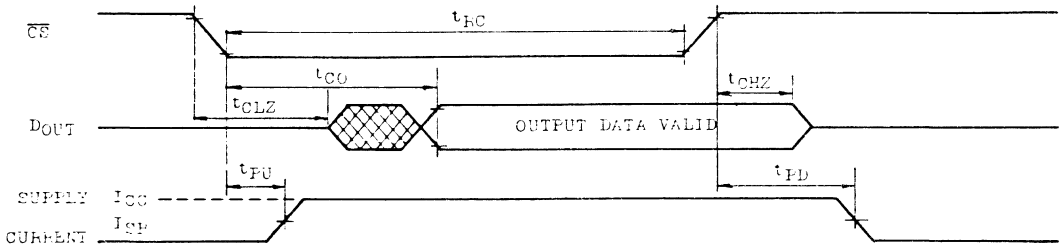
# TMM2018AP-25, TMM2018AP-35 TMM2018AP-45

## TIMING WAVEFORMS

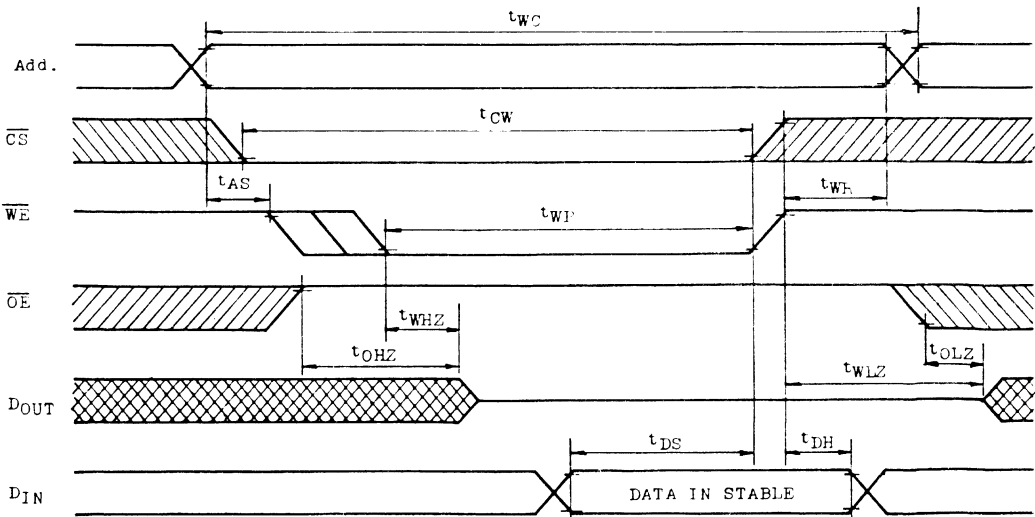
READ CYCLE 1. ( $\overline{WE}=V_{IH}$ ,  $\overline{CS}=V_{IL}$ )



READ CYCLE 2. ( $\overline{WE}=V_{IH}$ ,  $\overline{OE}=V_{IL}$ )

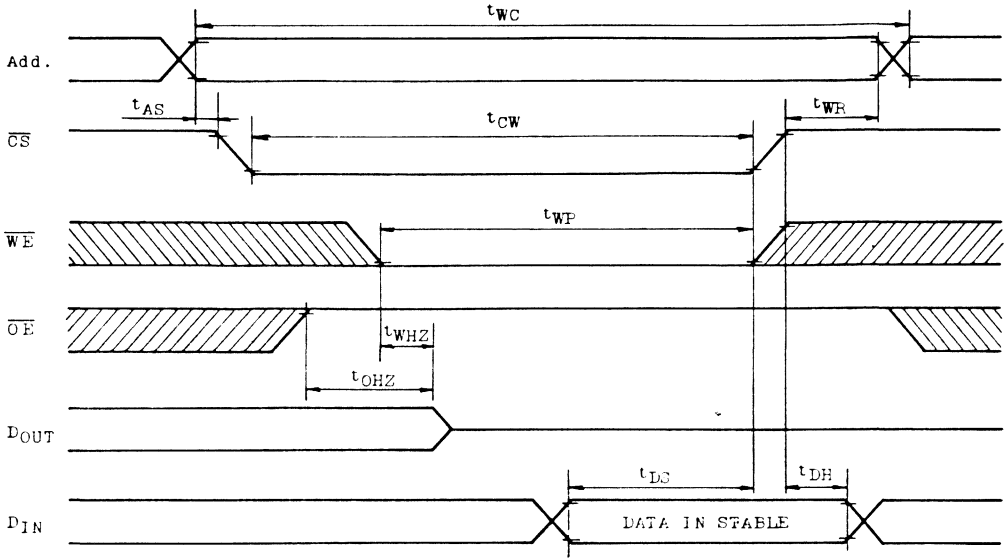


WRITE CYCLE 1.



**TMM2018AP-25, TMM2018AP-35  
TMM2018AP-45**

WRITE CYCLE 2.



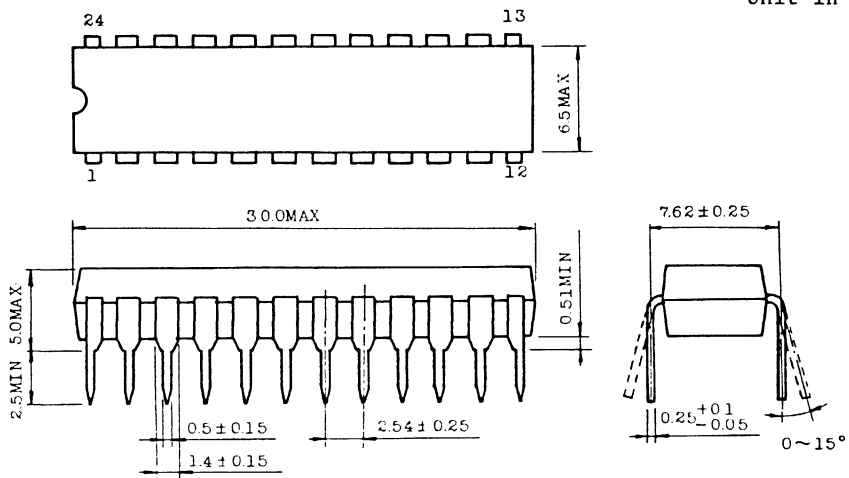
Note: 1. In read cycle 2, all addresses are valid prior to or coincident with  $\overline{CS}$  transition low.

2. The operating temperature ( $T_a$ ) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

**TMM2018AP-25, TMM2018AP-35  
TMM2018AP-45**

OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54mm.

All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.24 leads.

# TOSHIBA MOS MEMORY PRODUCT

**4,096 WORD × 4 BIT STATIC RAM**  
 SILICON MONOLITHIC  
 N-CHANNEL SILICON GATE MOS PROCESS

**TMM2068AD-25, TMM2068AD-35**  
**TMM2068AD-45**

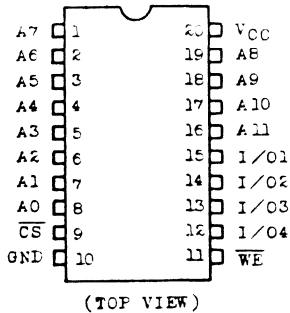
## DESCRIPTION

The TMM2068AD is a 16,384 bits high speed and low power static random access memory organized as 4,096 words by 4 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power, features with a maximum access time of 25ns/35ns/45ns and maximum operating current of 135/120/120mA. When  $\overline{CS}$  goes high, the device is deselected and placed in a low power standby mode in which maximum standby current is 20mA. Thus the TMM2068AD is most suitable for us in cache memory and high speed storage. The TMM2068AD is offered in a 20 pin standard cerdip package with 0.3 inch width for high density assembly. The TMM2068AD is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

## FEATURES

- . Fast access time
  - t<sub>ACC</sub>=25ns: TMM2068AD-25
  - t<sub>ACC</sub>=35ns: TMM2068AD-35
  - t<sub>ACC</sub>=45ns: TMM2068AD-45
- . Low power dissipation
  - I<sub>CC</sub>=135mA: TMM2068AD-25
  - I<sub>CC</sub>=120mA: TMM2068AD-35
  - I<sub>CC</sub>=120mA: TMM2068AD-45
  - I<sub>SB</sub>=20mA
- . Single 5V power supply
- . Fully static operation
- . All inputs and outputs: Directly TTL compatible
- . Power down feature :  $\overline{CS}=V_{IH}$
- . Three state outputs
- . Inputs protected: All inputs protection against static charge.
- . Package: 20 pins standard cerdip package, 0.3 inch width.

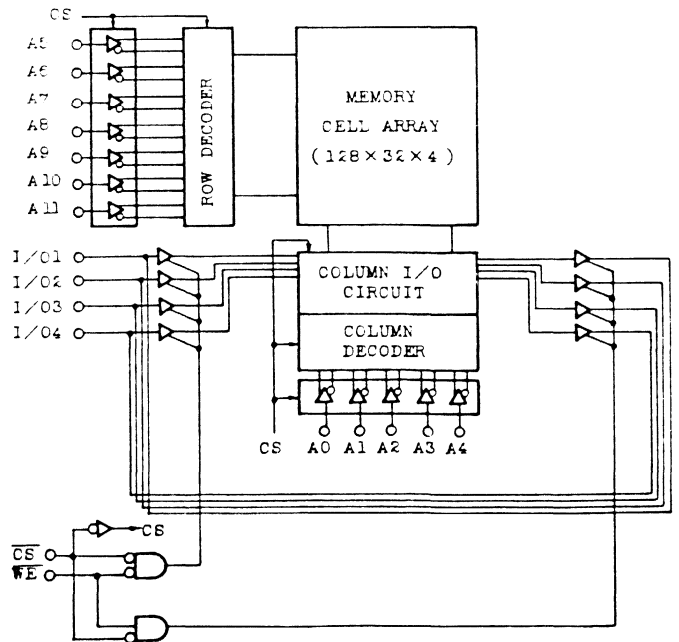
## PIN CONNECTION



## PIN NAMES

A0-A11	Address Inputs
I/O <sub>1</sub> -I/O <sub>4</sub>	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
VCC	Power (+5V)
GND	Ground

## BLOCK DIAGRAM



# TMM2068AD-25, TMM2068AD-35 TMM2068AD-45

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	Power Supply Voltage	-3.5~7.0	V
V <sub>IN</sub>	Input Voltage	-3.5~7.0	V
V <sub>I/O</sub>	Input/Output Voltage	-3.5~7.0	V
T <sub>opr</sub>	Operating Temperature	0~70	°C
T <sub>stg</sub>	Storage Temperature	-55~150	°C
T <sub>solder</sub>	Soldering Temperature·Time	260·10	°C·sec
P <sub>D</sub>	Power Dissipation	1.0	W
I <sub>OUT</sub>	D.C. Output Current	20	mA

## D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.0	-	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input Low Voltage	-3.0*	-	0.8	V
V <sub>CC</sub>	Power Supply Voltage	4.5	5.0	5.5	V

\* Pulse Width: 10ns, DC: -0.5V (Min.)

## D.C. CHARACTERISTICS (T<sub>a</sub>=0~70°C, V<sub>CC</sub>=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT	
I <sub>IL</sub>	Input Current	V <sub>IN</sub> =0~V <sub>CC</sub>	-	±1.0	μA	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> =-4.0mA	2.4	-	V	
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> =8.0mA	-	0.4	V	
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> =0~V <sub>CC</sub> , $\overline{CS}$ =V <sub>IH</sub>	-	±1.0	μA	
I <sub>CC</sub>	Operating Current	$\overline{CS}$ =V <sub>IL</sub>	-25	-	135	mA
			-35	-	120	
			-45	-	120	
I <sub>SB</sub>	Standby Current	$\overline{CS}$ =V <sub>IH</sub>	-	20	mA	
I <sub>SBP</sub>	Peak Power-on Current	$\overline{CS}$ =V <sub>CC</sub> , V <sub>CC</sub> =0~5.5V	-	40	mA	

## CAPACITANCE\* (T<sub>a</sub>=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =0V	8	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> =0V	8	

\* Note: This parameter is periodically sampled and is not 100% tested.



# TMM2068AD-25, TMM2068AD-35 TMM2068AD-45

## A.C. CHARACTERISTICS (Ta=0-70°C, VCC=5V±10%)

### Read Cycle

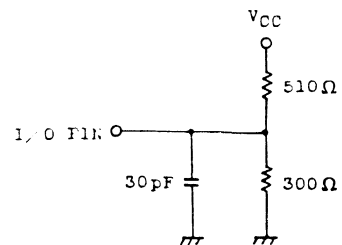
SYMBOL	PARAMETER	TMM2068AD-25		TMM2068AD-35		TMM2068AD-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	25	-	35	-	45	-	ns
t <sub>ACC</sub>	Address Access Time	-	25	-	35	-	45	
t <sub>CO</sub>	Chip Select Access Time	-	25	-	35	-	45	
t <sub>CLZ</sub>	Chip Selection to Output in Low-Z	5	-	5	-	5	-	
t <sub>CHZ</sub>	Chip Deselection to Output in High-Z	0	15	0	20	0	20	
t <sub>OH</sub>	Output Data Hold Time	5	-	5	-	5	-	
t <sub>PU</sub>	Chip Selection to Power Up Time	0	-	0	-	0	-	
t <sub>PD</sub>	Chip Deselection to Power Down Time	-	20	-	30	-	30	

### Write Cycle

SYMBOL	PARAMETER	TMM2068AD-25		TMM2068AD-35		TMM2068AD-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	25	-	35	-	45	-	ns
t <sub>CW</sub>	Chip Selection to End of Write	20	-	30	-	40	-	
t <sub>AS</sub>	Address Set Up Time	0	-	0	-	0	-	
t <sub>WP</sub>	Write Pulse Width	20	-	30	-	35	-	
t <sub>WR</sub>	Write Recovery Time	0	-	0	-	0	-	
t <sub>WLZ</sub>	$\overline{WE}$ to Output in Low-Z	0	-	0	-	0	-	
t <sub>WHZ</sub>	$\overline{WE}$ to Output in High-Z	0	10	0	15	0	15	
t <sub>DS</sub>	Data Set Up Time	10	-	15	-	20	-	
t <sub>DH</sub>	Data Hold Time	0	-	0	-	0	-	

### A.C. TEST CONDITIONS

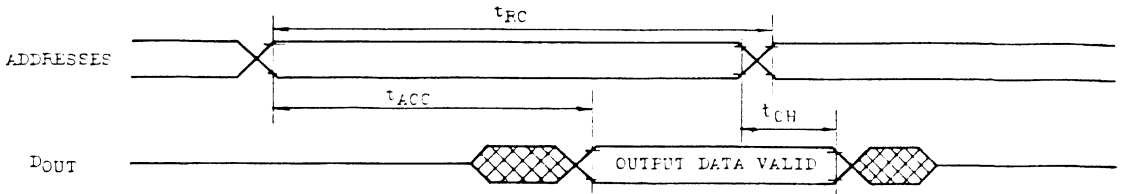
Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	2.0V/0.8V
Output Load	See Fig.1



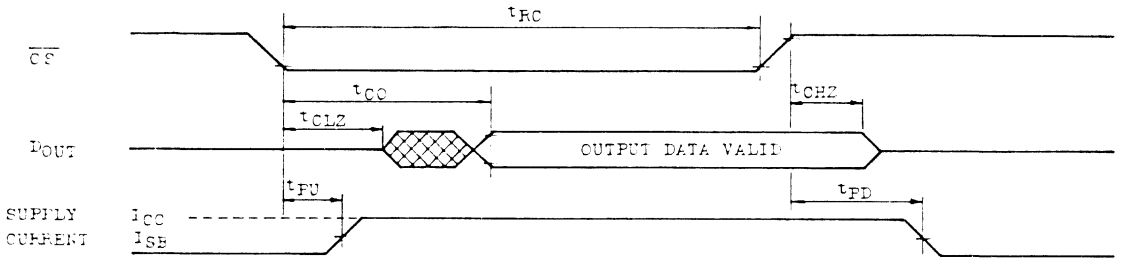
# TMM2068AD-25, TMM2068AD-35 TMM2068AD-45

## TIMING WAVEFORMS

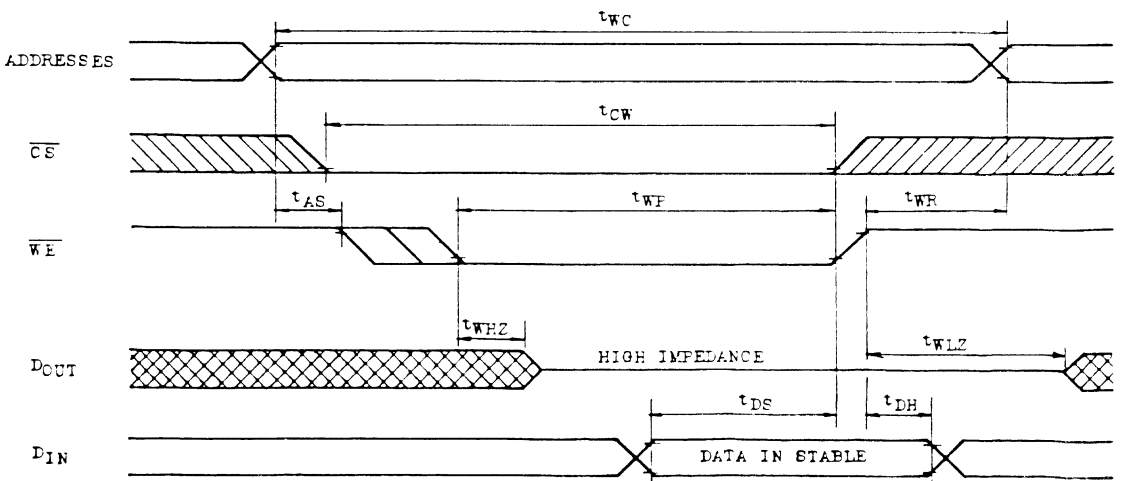
READ CYCLE 1. ( $\overline{WE}=V_{IH}$ ,  $\overline{CS}=V_{IL}$ )



READ CYCLE 2. ( $\overline{WE}=V_{IH}$ )

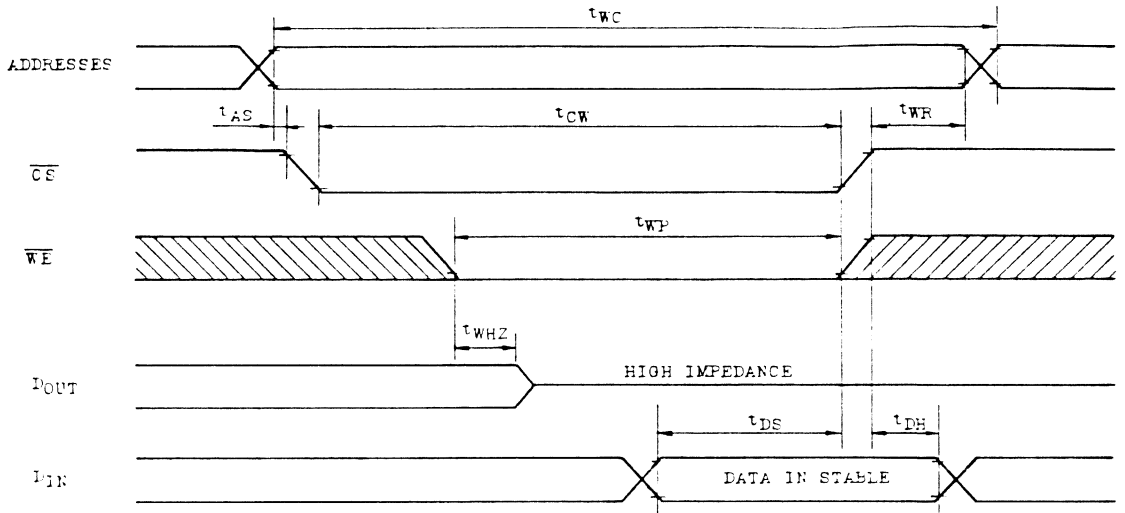


WRITE CYCLE 1.



**TMM2068AD-25, TMM2068AD-35  
TMM2068AD-45**

WRITE CYCLE 2.

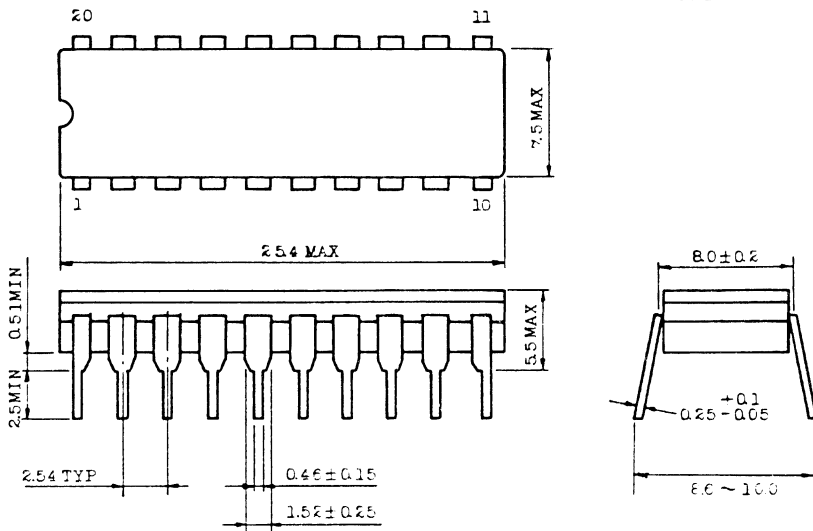


- Note 1. In read cycle 2, all addresses are valid prior to or coincident with  $\overline{CS}$  transition low.
2. The operating temperature ( $T_a$ ) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

**TMM2068AD-25, TMM2068AD-35  
TMM2068AD-45**

OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54mm.

All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.20 lead.

# TOSHIBA MOS MEMORY PRODUCT

**4,096 WORD × 4 BIT STATIC RAM**  
 SILICON MONOLITHIC  
 N-CHANNEL SILICON GATE MOS PROCESS

**TMM2068AP-25, TMM2068AP-35**  
**TMM2068AP-45**

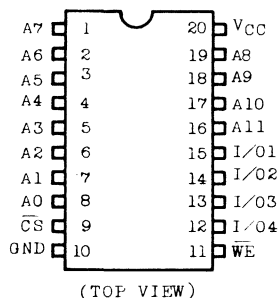
## DESCRIPTION

The TMM2068AP is a 16,384 bits high speed and low power static random access memory organized as 4,096 words by 4 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 25ns/35ns/45ns and maximum operating current of 135/120/120mA. When  $\overline{CS}$  goes high, the device is deselected and placed in a low power standby mode in which maximum standby current is 20mA. Thus the TMM2068AP is most suitable for us in cache memory and high speed storage. The TMM2068AP is offered in a 20 pin standard plastic package with 0.3 inch width for high density assembly. The TMM2068AP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

## FEATURES

- Fast access time
  - $t_{ACC}=25ns$ : TMM2068AP-25
  - $t_{ACC}=35ns$ : TMM2068AP-35
  - $t_{ACC}=45ns$ : TMM2068AP-45
- Low power dissipation
  - $I_{CC}=135mA$ : TMM2068AP-25
  - $I_{CC}=120mA$ : TMM2068AP-35
  - $I_{CC}=120mA$ : TMM2068AP-45
  - $I_{SB}=20mA$
- Single 5V power supply
- Fully static operation
- All inputs and outputs: Directly TTL compatible
- Power down feature :  $\overline{CS}=V_{IH}$
- Three state outputs
- Inputs protected: All inputs protection against static charge.
- Package: 20 pins standard plastic package, 0.3 inch width.

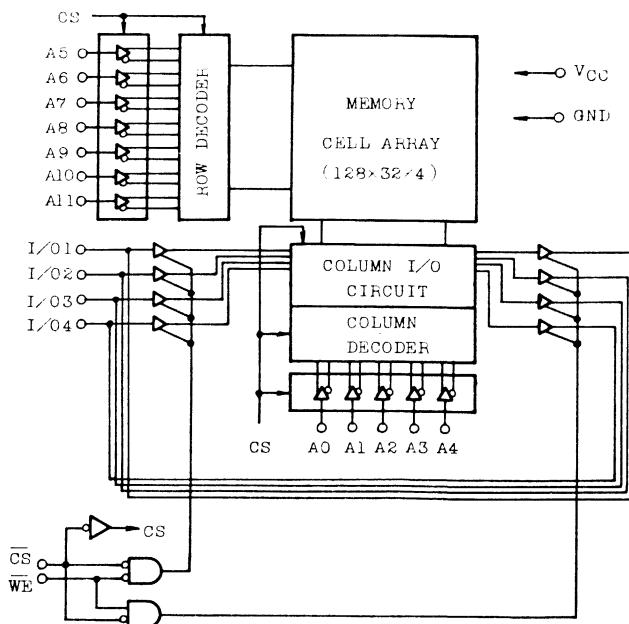
## PIN CONNECTION



## PIN NAMES

A0 ~ A11	Address Inputs
I/O1 ~ I/O4	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
VCC	Power (+5V)
GND	Ground

## BLOCK DIAGRAM



# TMM2068AP-25, TMM2068AP-35 TMM2068AP-45

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	Power Supply Voltage	-3.5 ~ 7.0	V
V <sub>IN</sub>	Input Voltage	-3.5 ~ 7.0	V
V <sub>I/O</sub>	Input/Output Voltage	-3.5 ~ 7.0	V
T <sub>opr</sub>	Operating Temperature	0 ~ 70	°C
T <sub>stg</sub>	Storage Temperature	-55 ~ 150	°C
T <sub>solder</sub>	Soldering Temperature • Time	260 • 10	°C • sec
P <sub>D</sub>	Power Dissipation	1.0	W
I <sub>OUT</sub>	D.C. Output Current	20	mA

## D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.0	-	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input Low Voltage	-3.0*	-	0.8	V
V <sub>CC</sub>	Power Supply Voltage	4.5	5.0	5.5	V

\* Pulse Width: 10ns, DC: -0.5V (Min.)

## D.C. CHARACTERISTICS (Ta=0 ~ 70°C, V<sub>CC</sub>=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT	
I <sub>IL</sub>	Input Current	V <sub>IN</sub> =0 ~ V <sub>CC</sub>	-	±1.0	μA	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> =-4.0mA	2.4	-	V	
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> =8.0mA	-	0.4	V	
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> =0 ~ V <sub>CC</sub> , $\overline{CS}$ =V <sub>IH</sub>	-	±1.0	μA	
I <sub>CC</sub>	Operating Current	$\overline{CS}$ =V <sub>IL</sub>	-25	-	135	mA
			-35	-	120	
			-45	-	120	
I <sub>SB</sub>	Standby Current	$\overline{CS}$ =V <sub>IH</sub>	-	20	mA	
I <sub>SBP</sub>	Peak Power-on Current	$\overline{CS}$ =V <sub>CC</sub> , V <sub>CC</sub> =0 ~ 5.5V	-	40	mA	

## CAPACITANCE\* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =0V	8	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> =0V	8	

\* Note: This parameter is periodically sampled and is not 100% tested.

# TMM2068AP-25, TMM2068AP-35 TMM2068AP-45

A.C. CHARACTERISTICS (Ta=0 ~ 70°C, VCC=5V±10%)

### Read Cycle

SYMBOL	PARAMETER	TMM2068AP-25		TMM2068AP-35		TMM2068AP-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	25	-	35	-	45	-	ns
t <sub>ACC</sub>	Address Access Time	-	25	-	35	-	45	
t <sub>CO</sub>	Chip Select Access Time	-	25	-	35	-	45	
t <sub>CLZ</sub>	Chip Selection to Output in Low-Z	5	-	5	-	5	-	
t <sub>CHZ</sub>	Chip Deselection to Output in High-Z	0	15	0	20	-	20	
t <sub>OH</sub>	Output Data Hold Time	5	-	5	-	5	-	
t <sub>PU</sub>	Chip Selection to Power Up Time	0	-	0	-	0	-	
t <sub>PD</sub>	Chip Deselection to Power Down Time	-	20	-	30	-	30	

### Write Cycle

SYMBOL	PARAMETER	TMM2068AP-25		TMM2068AP-35		TMM2068AP-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	25	-	35	-	45	-	ns
t <sub>CW</sub>	Chip Selection to End of Write	20	-	30	-	40	-	
t <sub>AS</sub>	Address Set Up Time	0	-	0	-	0	-	
t <sub>WP</sub>	Write Pulse Width	20	-	30	-	35	-	
t <sub>WR</sub>	Write Recovery Time	0	-	0	-	0	-	
t <sub>WLZ</sub>	$\overline{WE}$ to Output in Low-Z	0	-	0	-	0	-	
t <sub>WHZ</sub>	$\overline{WE}$ to Output in High-Z	0	10	0	15	0	15	
t <sub>DS</sub>	Data Set Up Time	10	-	15	-	20	-	
t <sub>DH</sub>	Data Hold Time	0	-	0	-	0	-	

### A.C. TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	2.0V/0.8V
Output Load	See Fig.1

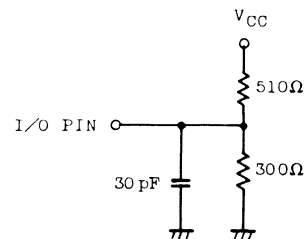
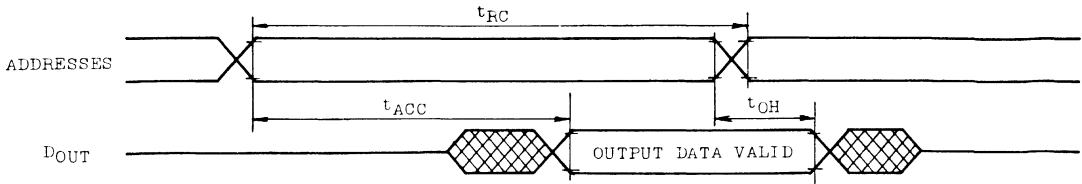


Fig.1 OUTPUT LOAD

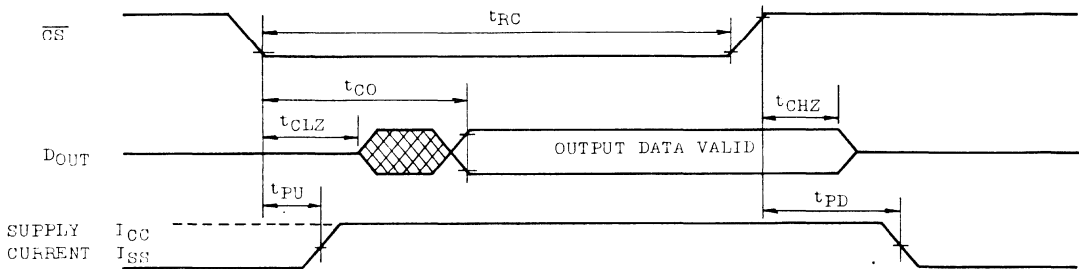
# TMM2068AP-25, TMM2068AP-35 TMM2068AP-45

## TIMING WAVEFORMS

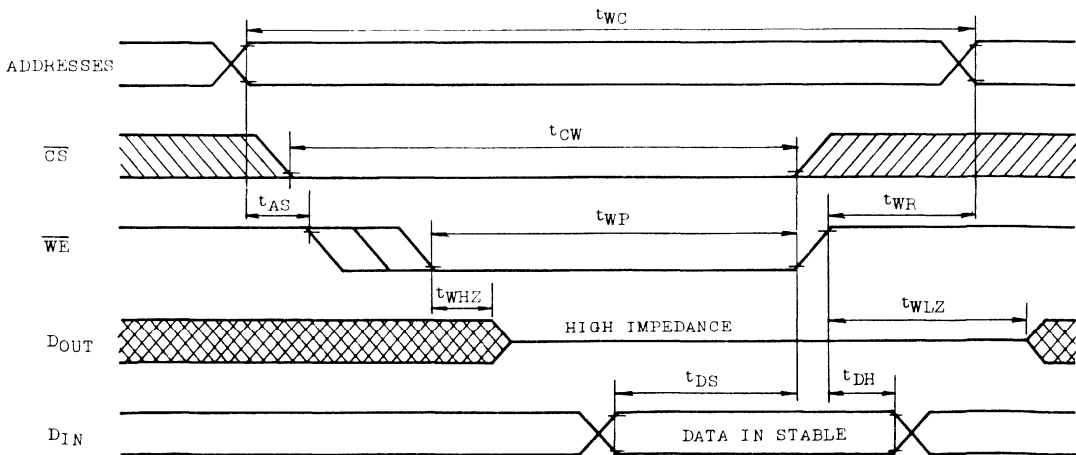
READ CYCLE 1. ( $\overline{WE}=V_{IH}$ ,  $\overline{CS}=V_{IL}$ )



READ CYCLE 2. ( $\overline{WE}=V_{IH}$ )



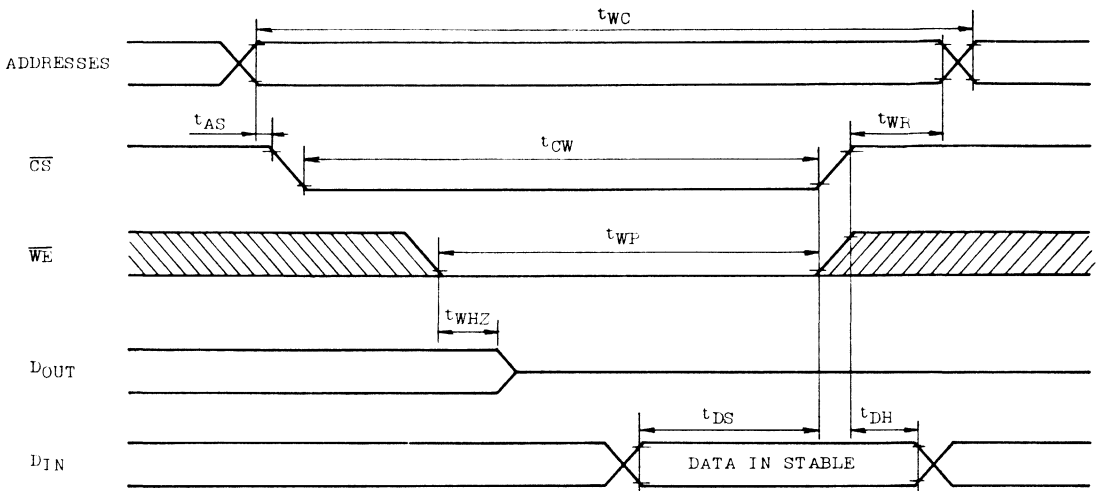
WRITE CYCLE 1.





# TMM2068AP-25, TMM2068AP-35 TMM2068AP-45

WRITE CYCLE 2.



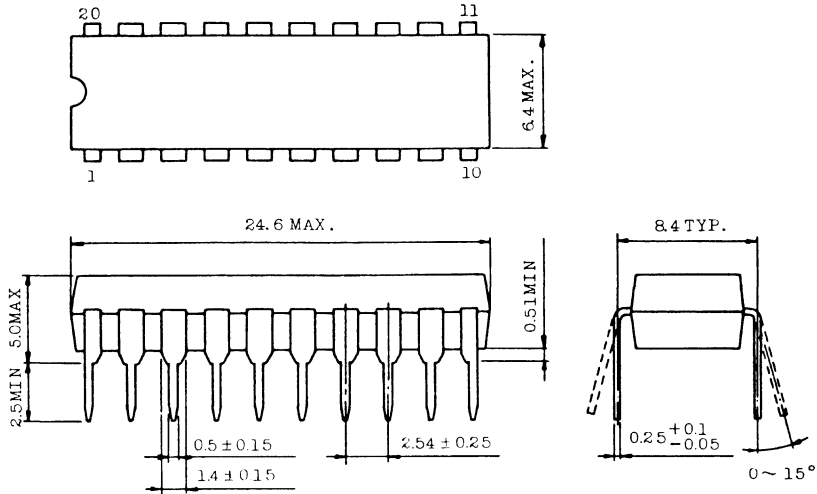
Note 1. In read cycle 2, all addresses are valid prior to or coincident with  $\overline{CS}$  transition low.

2. The operating temperature ( $T_a$ ) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

**TMM2068AP-25, TMM2068AP-35  
TMM2068AP-45**

OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54mm.

All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.20 leads.

# TOSHIBA MOS MEMORY PRODUCT

4,096 WORD × 4 BIT STATIC RAM  
 SILICON MONOLITHIC  
 N-CHANNEL SILICON GATE MOS PROCESS

**TMM2078AD-25, TMM2078AD-35  
 TMM2078AD-45**

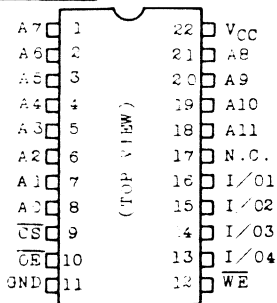
## DESCRIPTION

The TMM2078AD is a 16,384 bits high speed and low power static random access memory organized as 4,096 words by 4 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 25ns/35ns/45ns and maximum operating current of 135mA/120mA/120mA. When  $\overline{CS}$  goes high, the device is deselected and placed in a low power standby mode in which maximum standby current is 20mA. Thus the TMM2078AD is most suitable for use in cache memory and high speed storage. The TMM2078AD is offered in a 22 pin standard cerdip package with 0.3 inch width for high density assembly. The TMM2078AD is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

## FEATURES

- Fast access time
  - $t_{ACC}=25ns$ : TMM2078AD-25
  - $t_{ACC}=35ns$ : TMM2078AD-35
  - $t_{ACC}=45ns$ : TMM2078AD-45
- Low power dissipation
  - $ICC=135mA$ : TMM2078AD-25
  - $ICC=120mA$ : TMM2078AD-35
  - $ICC=120mA$ : TMM2078AD-45
  - $ISB=20mA$
- Single 5V power supply
- Fully static operation
- All inputs and outputs Directly TTL Compatible
- Power down feature:  $\overline{CS}=V_{IH}$
- Output buffer control:  $\overline{OE}$
- Three state outputs
- Inputs protected: All inputs protection against static charge.
- Package: 22 pins standard cerdip package, 0.3 inch width

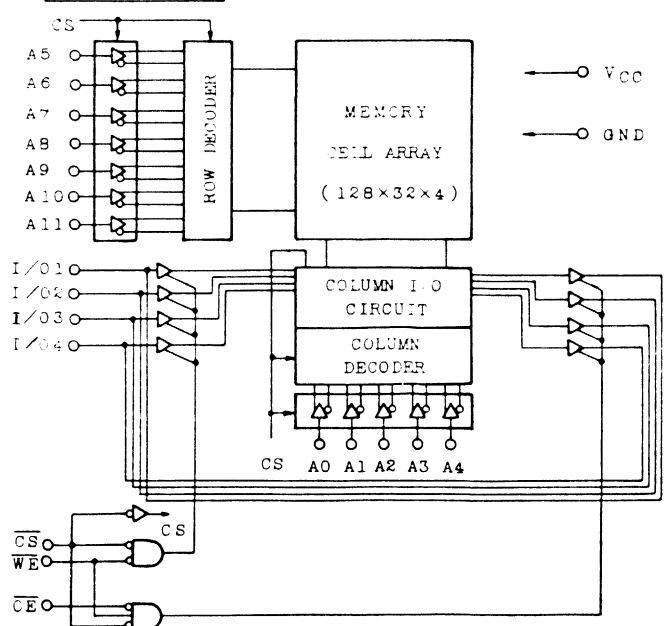
## PIN CONNECTION



## PIN NAMES

A <sub>0</sub> -A <sub>11</sub>	Address Inputs
I/O <sub>1</sub> -I/O <sub>4</sub>	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
VCC	Power (+5V)
GND	Ground
N.C.	No Connection

## BLOCK DIAGRAM



# TMM2078AD-25, TMM2078AD-35 TMM2078AD-45

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
VCC	Power Supply Voltage	-3.5-7.0	V
VIN	Input Voltage	-3.5-7.0	V
VI/O	Input/Output Voltage	-3.5-7.0	V
Topr	Operating Temperature	0-70	°C
Tstg	Storage Temperature	-55-150	°C
Tsolder	Soldering Temperature · Time	260 · 10	°C·sec
PD	Power Dissipation	0.9	W
IOUT	D.C. Output Current	20	mA

## D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	2.0	-	VCC+1.0	V
VIL	Input Low Voltage	-3.0*	-	0.8	V
VCC	Power Supply Voltage	4.5	5.0	5.5	V

\* Pulse Width: 10ns, DC: -0.5V(MIN.)

## D.C. CHARACTERISTICS (Ta=0-70°C, VCC=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT	
IIL	Input Current	VIN=0-VCC	-	±1.0	µA	
VOH	Output High Voltage	IOH=-4.0mA	2.4	-	V	
VOL	Output Low Voltage	IOL=8.0mA	-	0.4	V	
ILO	Output Leakage Current	VOU=0-VCC, $\overline{CS}=V_{IH}$	-	±1.0	µA	
ICC	Operating Current	$\overline{CS}=V_{IL}$	-25	-	135	mA
			-35	-	120	
			-45	-	120	
ISB	Standby Current	$\overline{CS}=V_{IH}$	-	20	mA	
ISBP	Peak Power-on Current	$\overline{CS}=V_{CC}$ , VCC=0-5.5V	-	40	mA	

## CAPACITANCE\* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
CIN	Input Capacitance	VIN=0V	8	PF
COU	Output Capacitance	VOU=0V	8	

\* Note: This parameter is periodically sampled and is not 100% tested.

# TMM2078AD-25, TMM2078AD-35 TMM2078AD-45

A.C. CHARACTERISTICS (Ta=0-70°C, VCC=5V±10%)

## READ CYCLE

SYMBOL	PARAMETER	TMM2078AD-25		TMM2078AD-35		TMM2078AD-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	25	-	35	-	45	-	ns
t <sub>ACC</sub>	Address Access Time	-	25	-	35	-	45	
t <sub>CO</sub>	Chip Select Access Time	-	25	-	35	-	45	
t <sub>OE</sub>	Output Enable to Output Valid	-	15	-	20	-	20	
t <sub>CLZ</sub>	Chip Selection to Output in Low-Z	0	-	0	-	5	-	
t <sub>CHZ</sub>	Chip Deselection to Output in High-Z	-	15	-	20	-	20	
t <sub>OLZ</sub>	Output Enable to Output in Low-Z	0	-	0	-	0	-	
t <sub>OHZ</sub>	Output Disable to Output in High-Z	-	10	-	15	-	15	
t <sub>OH</sub>	Output Data Hold Time	5	-	5	-	5	-	
t <sub>PU</sub>	Chip Selection to Power Up Time	0	-	0	-	0	-	
t <sub>PD</sub>	Chip Deselection to Power Down Time	-	20	-	30	-	30	

## WRITE CYCLE

SYMBOL	PARAMETER	TMM2078AD-25		TMM2078AD-35		TMM2078AD-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	25	-	35	-	45	-	ns
t <sub>CW</sub>	Chip Selection to End of Write	20	-	30	-	40	-	
t <sub>AS</sub>	Address Set Up Time	0	-	0	-	0	-	
t <sub>WP</sub>	Write Pulse Width	20	-	30	-	35	-	
t <sub>WR</sub>	Write Recovery Time	0	-	0	-	0	-	
t <sub>WLZ</sub>	$\overline{WE}$ to Output in Low-Z	0	-	0	-	0	-	
t <sub>WHZ</sub>	$\overline{WE}$ to Output in High-Z	-	10	-	15	-	15	
t <sub>DS</sub>	Data Set Up Time	10	-	15	-	20	-	
t <sub>DH</sub>	Data Hold Time	0	-	0	-	0	-	

## A.C. TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	2.0V/0.8V
Output Load	See Fig.1

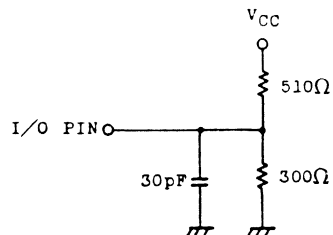
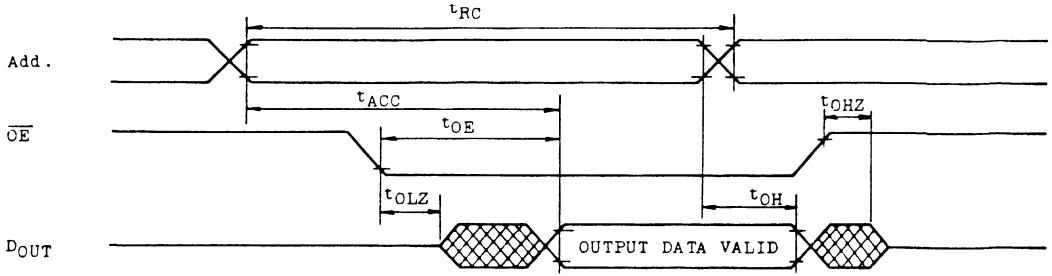


Fig.1 Output Load

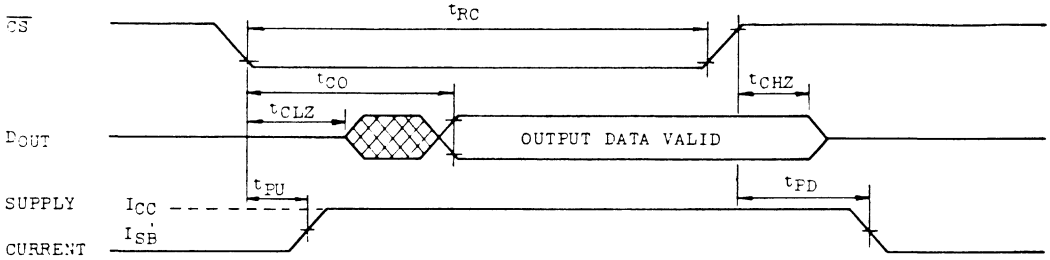
# TMM2078AD-25, TMM2078AD-35 TMM2078AD-45

## TIMING WAVEFORMS

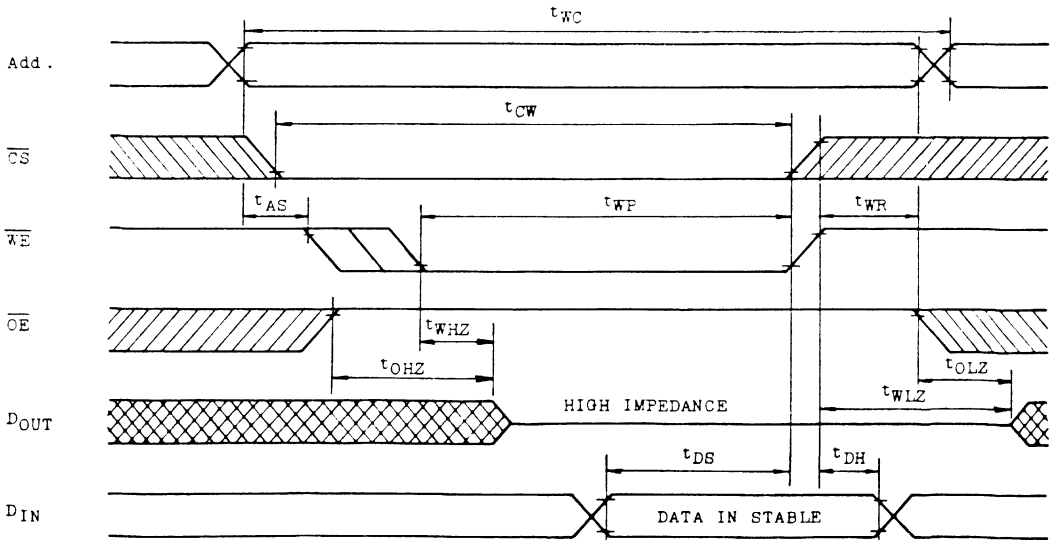
READ CYCLE 1. ( $\overline{WE}=V_{IH}$ ,  $\overline{CS}=V_{IL}$ )



READ CYCLE 2. ( $\overline{WE}=V_{IH}$ ,  $\overline{OE}=V_{IL}$ )

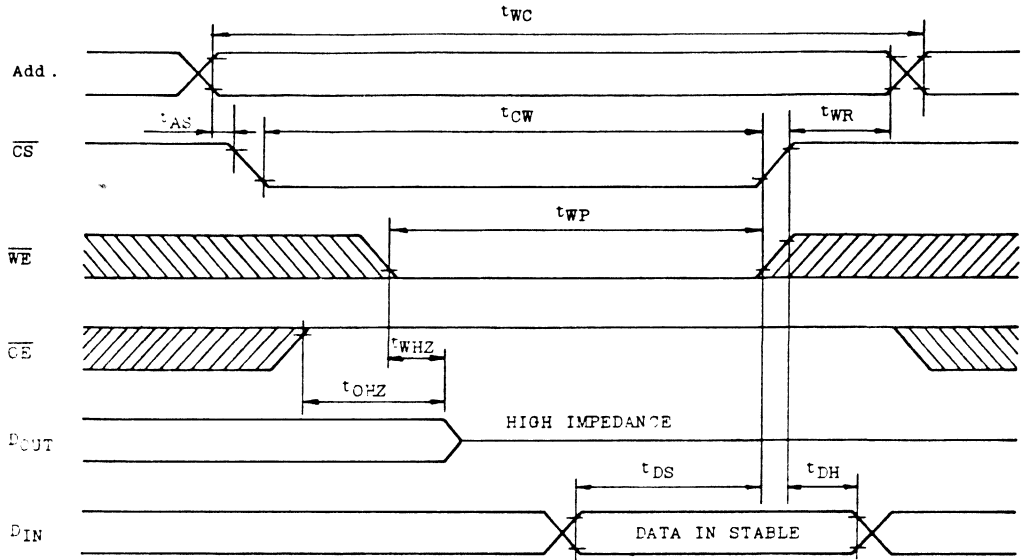


WRITE CYCLE 1.



**TMM2078AD-25, TMM2078AD-35  
TMM2078AD-45**

WRITE CYCLE 2.



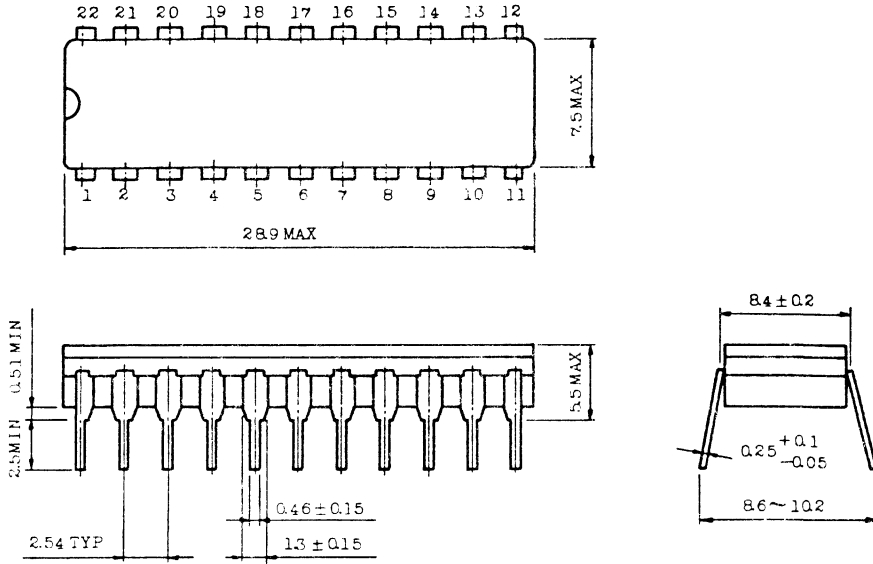
Note:

1. In read cycle 2, all addresses are valid prior to or coincident with  $\overline{CS}$  transition low.
2. The operating temperature ( $T_a$ ) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

**TMM2078AD-25, TMM2078AD-35  
TMM2078AD-45**

OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.22 leads.



# TOSHIBA MOS MEMORY PRODUCT

8,192 WORD × 8 BIT STATIC RAM  
N-CHANNEL SILICON GATE MOS

**TMM2088P-35, TMM2088P-45**  
**TMM2088P-55**

## DESCRIPTION

The TMM2088P is a 65,536 bits high speed N-channel silicon gate MOS static random access memory organized as 8,192 words by 8 bits and operates from a single 5-volt supply. The TMM2088P is features an automatic stand-by mode when deselected by  $\overline{CS1}$  signal. Thus the TMM2088P is suitable for use in cache memory and high speed storage. The TMM2088P is offered in a 28 pin standard plastic dual in-line package with 0.3 inch width for high density assembly.

## FEATURES

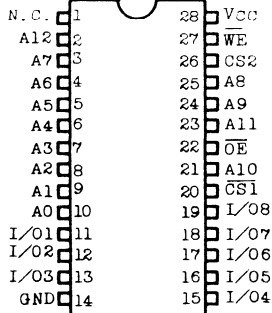
- Access Time and Current

Parameter Part Number	Access Time (MAX.)	Operating Current (MAX.)	Standby Current (MAX.)
TMM2088P-35	35ns	135mA	15mA
TMM2088P-45	45ns	135mA	15mA
TMM2088P-55	55ns	135mA	15mA

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature: ( $\overline{CS1}$ )
- Output Buffer Control: ( $\overline{OE}$ )
- Three State Outputs
- All Inputs and Outputs: (Directly TTL Compatible)

- Inputs Protected: (All inputs have Protection against static charge.)

## PIN CONNECTION



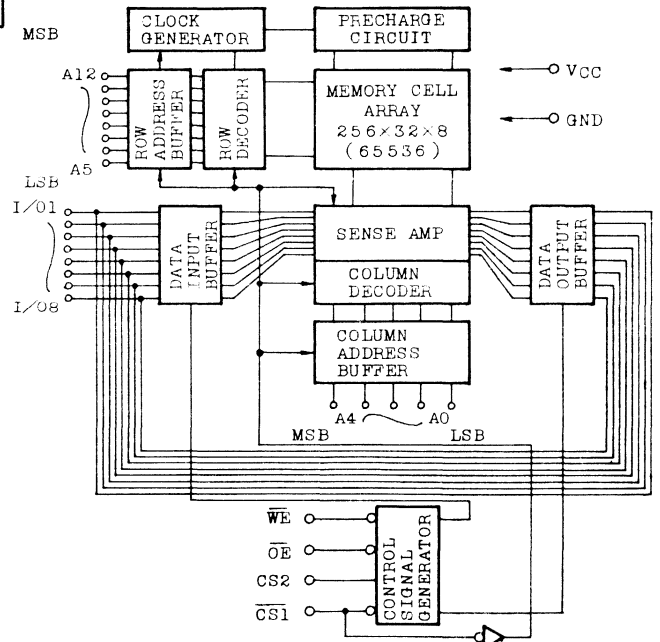
## PIN NAMES

A0 ~ A12	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{CS1}$ , CS2	Chip Select Inputs
I/O1 ~ I/O8	Data Input/Output
VCC	Power (+5V)
GND	Ground
N.C.	No Connection

## OPERATION MODE

MODE	CS1	CS2	OE	$\overline{WE}$	I/O1 ~ 8	Power
Write	L	H	*	L	In	Active
Read	L	H	L	H	Out	Active
Standby	H	*	*	*	High-Z	Standby
Standby	L	L	*	*	High-Z	Active
Output Buffer Disable	L	H	H	H	High-Z	Active

## BLOCK DIAGRAM



# TMM2088P-35, TMM2088P-45 TMM2088P-55

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	Power Supply Voltage	-3.5 ~ 7.0	V
V <sub>IN</sub> , V <sub>OUT</sub>	Input Output Voltage	-3.5 ~ 7.0	V
T <sub>opr.</sub>	Operating Temperature	0 ~ 70	°C
T <sub>stg.</sub>	Storage Temperature	-55 ~ 150	°C
T <sub>solder</sub>	Soldering Temperature • Time	260 • 10	°C•sec
P <sub>D</sub>	Power Dissipation (Ta=70°C)	1.0	W

## D.C. RECOMMENDED OPERATING CONDITIONS (Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input Low Voltage	-3.0*	-	0.8	V
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V

\* Pulse Width: 10ns, DC: -0.5V (Min.)

## D.C. CHARACTERISTICS (Ta=0 ~ 70°C, V<sub>CC</sub>=5.0V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I <sub>IIL</sub>	Input Leakage Current	V <sub>IN</sub> =0V ~ 5.5V	-1.0	1.0	μA
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> =2.4V	-4.0	-	mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> =0.4V	8.0	-	mA
I <sub>LO</sub>	Output Leakage Current	$\overline{CS1}=V_{IH}$ or CS2=V <sub>IL</sub> or $\overline{WE}=V_{IL}$ or $\overline{OE}=V_{IH}$ , V <sub>OUT</sub> =0V~5.5V	-1.0	1.0	μA
I <sub>SBP</sub>	Peak Power-on Current	$\overline{CS1}=V_{CC}$ , CS2=0V, I <sub>OUT</sub> =0mA	-	30	mA
I <sub>SB</sub>	Standby Current	$\overline{CS1}=V_{IH}$ , I <sub>OUT</sub> =0mA	-	15	mA
I <sub>CC</sub>	Operating Current	$\overline{CS1}=V_{IL}$ , I <sub>OUT</sub> =0mA	-	135	mA

## CAPACITANCE\* (Ta=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =0V	8	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>IN</sub> =0V	10	pF

\* Note: This parameter is periodically sampled and is not 100% tested.

# TMM2088P-35, TMM2088P-45 TMM2088P-55

## A.C. CHARACTERISTICS (Ta=0 ~ 70°C, VCC=5V±10%)

### READ CYCLE

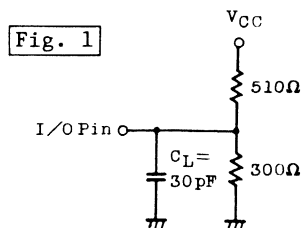
SYMBOL	PARAMETER	TMM2088P-35		TMM2088P-45		TMM2088P-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	35	-	45	-	55	-	ns
t <sub>ACC</sub>	Address Access Time	-	35	-	45	-	55	
t <sub>CO1</sub>	CS1 Access Time	-	35	-	45	-	45	
t <sub>CO2</sub>	CS2 Access Time	-	25	-	25	-	30	
t <sub>OE</sub>	OE Access Time	-	20	-	20	-	25	
t <sub>OH</sub>	Output Data Hold Time from Address Change	5	-	5	-	5	-	
t <sub>CLZ</sub>	Output Enable Time from CS1 or CS2	0	-	5	-	5	-	
t <sub>CHZ</sub>	Output Disable Time from CS1 or CS2	-	20	-	20	-	20	
t <sub>OLZ</sub>	Output Enable Time from OE	0	-	0	-	0	-	
t <sub>OHZ</sub>	Output Disable Time from OE	-	15	-	15	-	20	
t <sub>PU</sub>	Chip Selection to Power Up Time	0	-	0	-	0	-	
t <sub>PD</sub>	Chip Deselection to Power Down Time	-	30	-	30	-	30	

### WRITE CYCLE

SYMBOL	PARAMETER	TMM2088P-35		TMM2088P-45		TMM2088P-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	35	-	45	-	55	-	ns
t <sub>CW</sub>	Chip Selection to End of Write	30	-	40	-	50	-	
t <sub>AS</sub>	Address Set Up Time	0	-	0	-	0	-	
t <sub>WP</sub>	Write Pulse Width	25	-	35	-	45	-	
t <sub>WR</sub>	Write Recovery Time	0	-	0	-	0	-	
t <sub>DS</sub>	Data Set Up Time	15	-	20	-	20	-	
t <sub>DH</sub>	Data Hold Time	0	-	0	-	0	-	
t <sub>WLZ</sub>	Output Enable Time from WE	0	-	0	-	0	-	
t <sub>WHZ</sub>	Output Disable Time from WE	-	15	-	15	-	20	

### A.C. TEST CONDITIONS

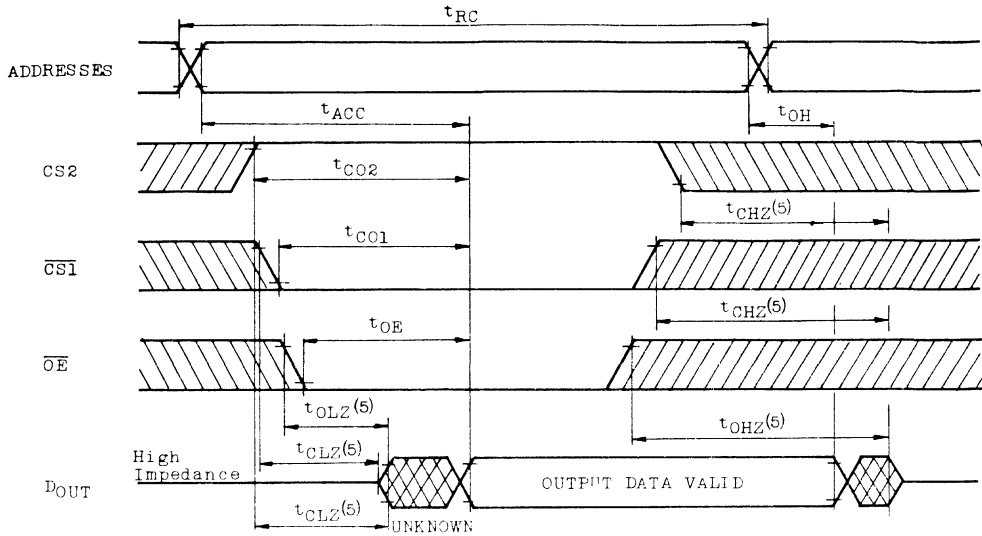
Input Pulse Levels	0.0 ~ 3.0V
Input Rise and Fall Time	5ns
Input and Output Reference Levels	2.0V/0.8V
Output Load	Fig. 1



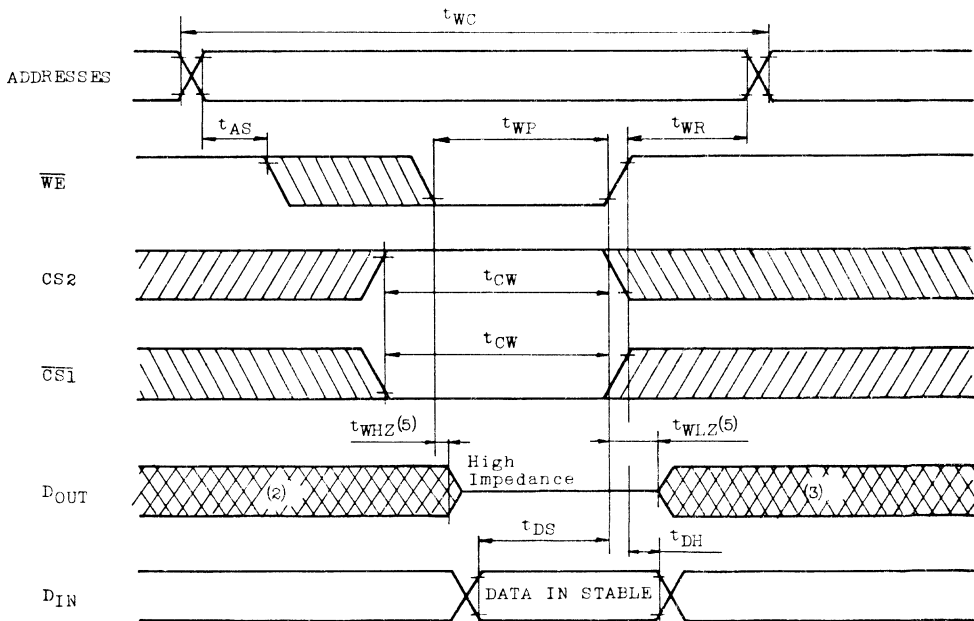
# TMM2088P-35, TMM2088P-45 TMM2088P-55

## TIMING WAVEFORMS

### READ CYCLE (1)

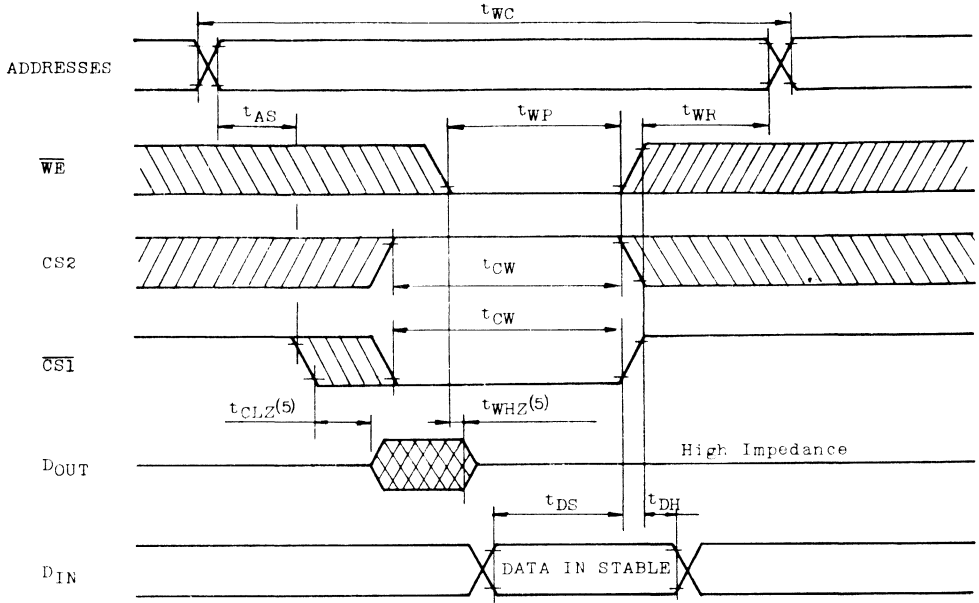


### WRITE CYCLE 1 (4) ( $\overline{WE}$ Controlled Write)

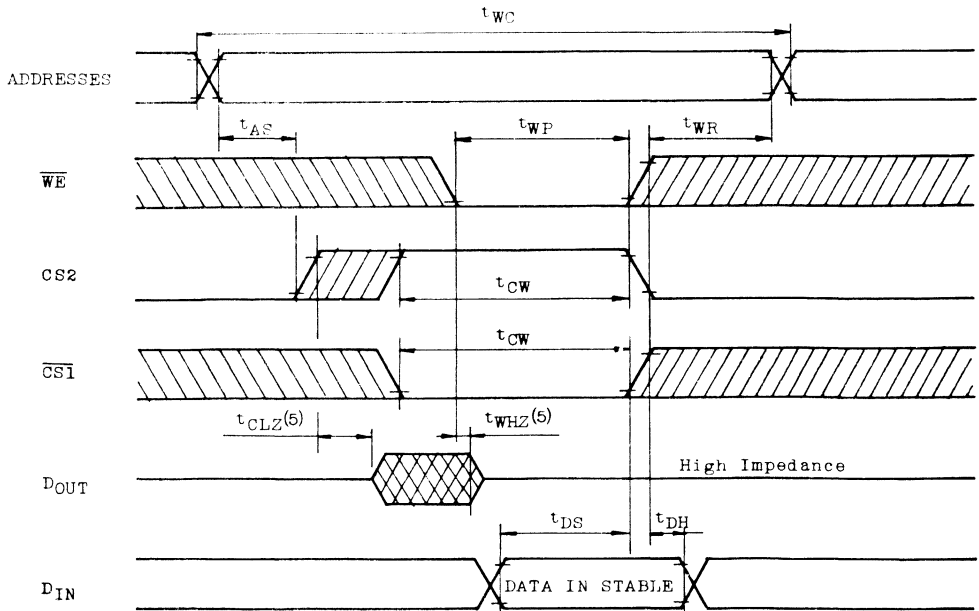


# TMM2088P-35, TMM2088P-45 TMM2088P-55

WRITE CYCLE 2 (4) ( $\overline{\text{CS1}}$  Controlled Write)



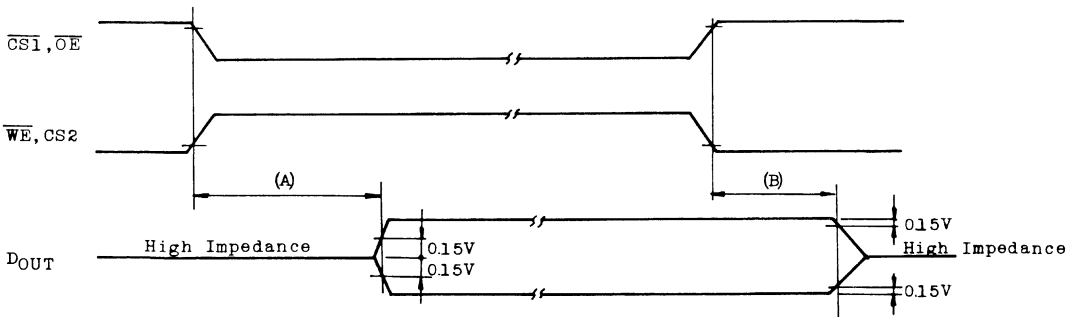
WRITE CYCLE 3 (4) ( $\text{CS2}$  Controlled Write)



# TMM2088P-35, TMM2088P-45 TMM2088P-55

- Note: 1.  $\overline{WE}$  is High for Read Cycle.
2. Assuming that  $\overline{CS1}$  Low transition or CS2 High transition occurs coincident with or after  $\overline{WE}$  Low transition, Outputs remain in a high impedance state.
  3. Assuming that  $\overline{CS1}$  High transition or CS2 Low transition occurs coincident with or prior to  $\overline{WE}$  High transition, Outputs remain in a high impedance state.
  4. Assuming that  $\overline{OE}$  is High for Write Cycle, Outputs are in high impedance state during this period.
  5. These parameters are specified as follows and measured by using the load shown in Fig. 1.

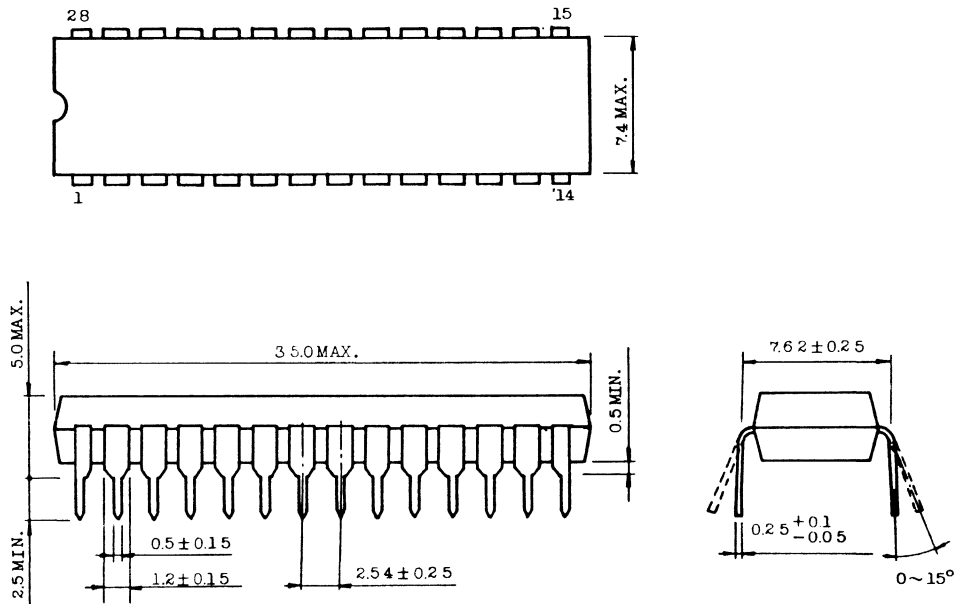
- (A)  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{WLZ}$  ..... Output Enable Time  
 (B)  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$  ..... Output Disable Time



**TMM2088P-35, TMM2088P-45  
TMM2088P-55**

DIP 28 PIN OUTLINE DRAWING

Unit in mm



Note: Lead pitch is 2.54 and tolerance is  $\pm 0.25$  against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.





# TOSHIBA MOS MEMORY PRODUCT

8,192 WORD × 9 BIT STATIC RAM  
N-CHANNEL SILICON GATE MOS

**TMM2089C-35**  
**TMM2089C-45**  
**TMM2089C-55**

PRELIMINARY

## DESCRIPTION

The TMM2089C is a 73,728 bits high speed N-channel silicon gate MOS static random access memory organized as 8,192 words by 9 bits and operates from a single 5-volt supply. The TMM2089C is features an automatic stand-by mode when deselected by  $\overline{CS1}$  signal. Thus the TMM2089C

is suitable for use in cache memory and high speed storage. The TMM2089C has nine I/O terminals, therefore it is most suitable for MEMORY SYSTEM with Parity bit. The TMM2089C is offered in a 28 pin standard ceramic dual in-line package with 0.3 inch width for high density assembly.

## FEATURES

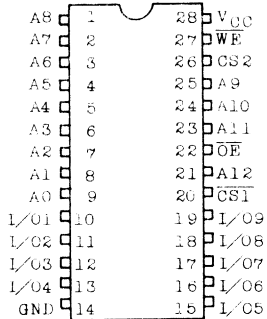
- Access Time and Current

Part Number	Parameter	Access Time (MAX.)	Operating Current (MAX.)	Standby Current (MAX.)
TMM2089C-35		35ns	135mA	15mA
TMM2089C-45		45ns	135mA	15mA
TMM2089C-55		55ns	135mA	15mA

- Single 5V Power Supply
- Fully static Operation
- Power Down Feature : ( $\overline{CS1}$ )
- Output Buffer Control : ( $\overline{OE}$ )
- Three State Outputs

- All Inputs and Outputs: (Directly TTL Compatible)
- Inputs Protected: (All inputs have protection against static charge.)

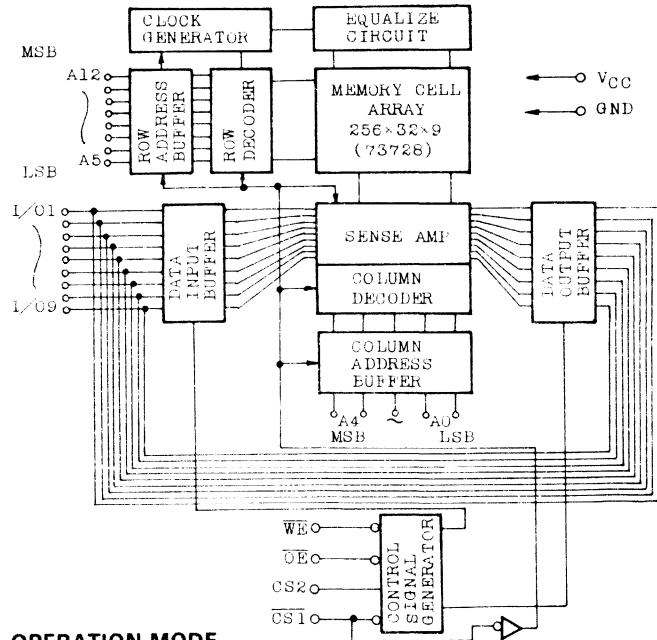
## PIN CONNECTION (TOP VIEW)



## PIN NAMES

$A_0 - A_{12}$	Address Inputs
$\overline{CS1}, \overline{CS2}$	Chip Select Inputs
$\overline{WE}$	Write Enable Input
I/O1 ~ I/O9	Data Input Output
$\overline{OE}$	Output Enable input
$V_{CC}$	Power (+5V)
GND	Ground

## BLOCK DIAGRAM



## OPERATION MODE

MODE	$\overline{CS1}$	$\overline{CS2}$	$\overline{OE}$	$\overline{WE}$	I/O1-9	Power
Write	L	H	*	L	In	Active
Read	L	H	L	H	Out	Active
Standby	H	*	*	*	High-Z	Standby
Standby	L	L	*	*	High-Z	Active
Output Buffer Disable	L	H	H	H	High-Z	Active

# TMM2089C-35, TMM2089C-45 TMM2089C-55

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	Power Supply Voltage	-3.5 ~ 7.0	V
V <sub>IN</sub> , V <sub>OUT</sub>	Input Output Voltage	-3.5 ~ 7.0	V
T <sub>opr.</sub>	Operating Temperature	0 ~ 70	°C
T <sub>stg.</sub>	Storage Temperature	-55 ~ 150	°C
T <sub>solder</sub>	Soldering Temperature · Time	260 · 10	°C · sec
P <sub>D</sub>	Power Dissipation (Ta = 70°C)	1.0	W

## D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V <sub>IH</sub>	Input High Voltage	2.0	—	V <sub>CC</sub> + 1.0	V
V <sub>IL</sub>	Input Low Voltage	-3.0	—	0.8	V
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	4.50	5.00	5.50	V

\* Pulse width : 10ns, DC : -0.5V (Min.)

## D. C. CHARACTERISTICS (Ta = 0 ~ 70°C, V<sub>CC</sub> = 5.0V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0V ~ 5.5V	-1.0	1.0	μA
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4V	-4.0	—	mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4V	8.0	—	mA
I <sub>IO</sub>	Output Leakage Current	CS1 = V <sub>IH</sub> or CS2 = V <sub>IL</sub> or WE = V <sub>IL</sub> or OE = V <sub>IH</sub> , V <sub>OUT</sub> = 0V ~ 5.5V	-1.0	1.0	μA
I <sub>SBP</sub>	Peak Power-on Current	CS1 = V <sub>CC</sub> , CS2 = 0V, I <sub>OUT</sub> = 0mA	—	30	mA
I <sub>SB</sub>	Standby Current	CS1 = V <sub>IH</sub> , I <sub>OUT</sub> = 0mA	—	15	mA
I <sub>CC</sub>	Operating Current	CS1 = V <sub>IL</sub> , I <sub>OUT</sub> = 0mA	—	135	mA

## CAPACITANCE \* (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	8	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>IN</sub> = 0V	10	pF

\* Note : This parameter is periodically sampled and is not 100% tested.

# TMM2089C-35, TMM2089C-45 TMM2089C-55

## A. C. CHARACTERISTICS (Ta = 0 ~ 70 °C, Vcc = 5V ± 10%)

### READ CYCLE

SYMBOL	PARAMETER	TMM2089C-35		TMM2089C-45		TMM2089C-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	35	—	45	—	55	—	ns
t <sub>ACC</sub>	Address Access Time	—	35	—	45	—	55	
t <sub>CO1</sub>	CS1 Access Time	—	35	—	45	—	45	
t <sub>CO2</sub>	CS2 Access Time	—	25	—	25	—	30	
t <sub>OE</sub>	OE Access Time	—	20	—	20	—	25	
t <sub>OH</sub>	Output Data Hold Time from Address Change	5	—	5	—	5	—	
t <sub>CLZ</sub>	Output Enable Time from CS1 or CS2	0	—	5	—	5	—	
t <sub>CHZ</sub>	Output Disable Time from CS1 or CS2	—	20	—	20	—	20	
t <sub>OLZ</sub>	Output Enable Time from OE	0	—	0	—	0	—	
t <sub>OHZ</sub>	Output Disable Time from OE	—	10	—	10	—	15	
t <sub>PU</sub>	Chip Selection to Power Up Time	0	—	0	—	0	—	
t <sub>PD</sub>	Chip Deselection to Power Down Time	—	30	—	30	—	30	

### WRITE CYCLE

SYMBOL	PARAMETER	TMM2089C-35		TMM2089C-45		TMM2089C-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	35	—	45	—	55	—	ns
t <sub>CW</sub>	Chip Selection to End of Write	30	—	40	—	50	—	
t <sub>AS</sub>	Address Set Up Time	0	—	0	—	0	—	
t <sub>WP</sub>	Write Pulse Width	25	—	35	—	45	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	
t <sub>DS</sub>	Data Set UP Time	15	—	20	—	20	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	
t <sub>WLZ</sub>	Output Enable Time from WE	0	—	0	—	0	—	
t <sub>WHZ</sub>	Output Disable Time from WE	—	10	—	10	—	15	

## A. C. TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Time	5ns
Input and Output Reference Levels	2.0V/0.8V
Output Load	Fig. 1

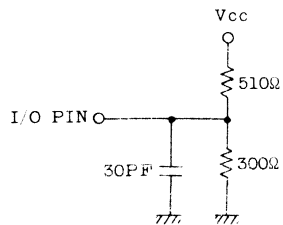
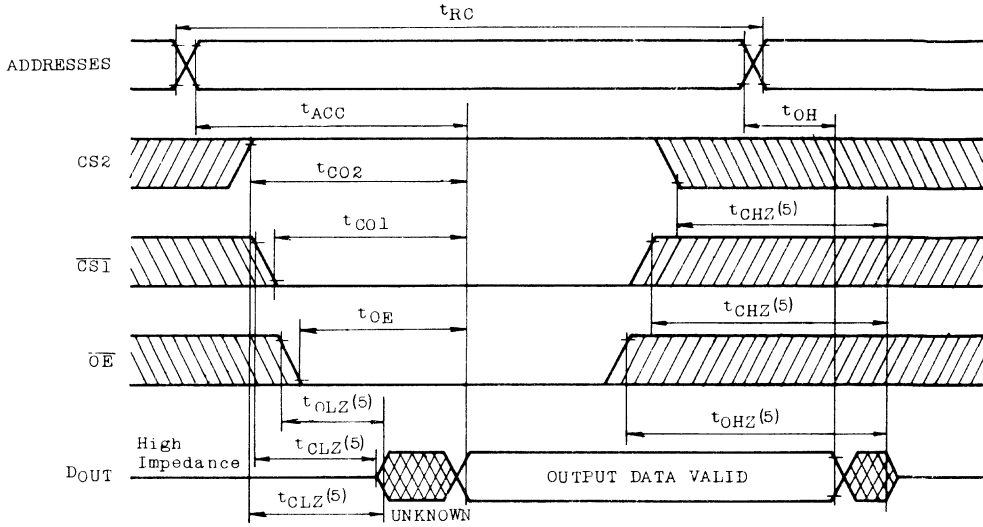


Fig. 1 Output Load

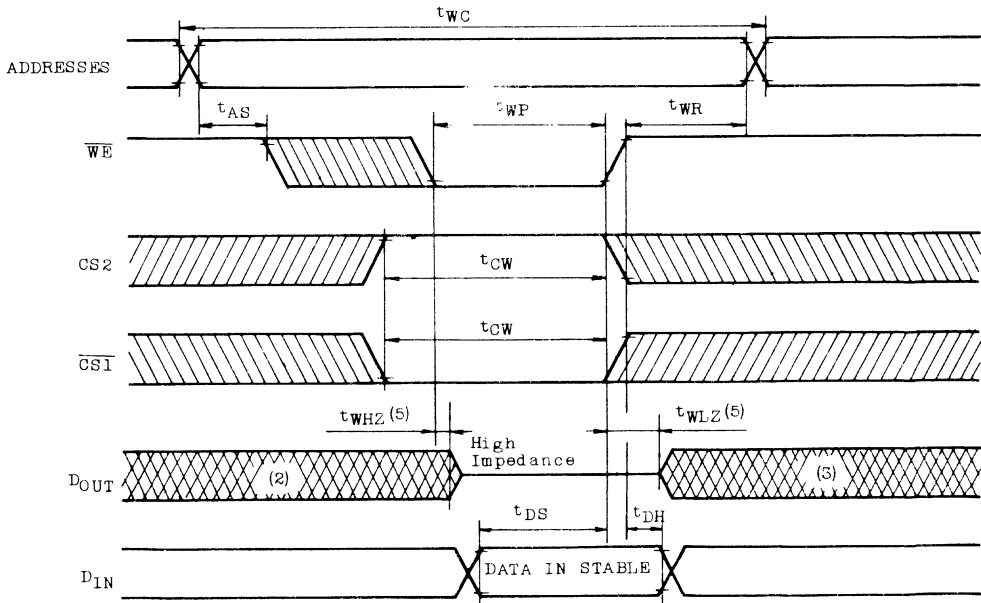
# TMM2089C-35, TMM2089C-45 TMM2089C-55

## TIMING WAVEFORMS

### ● READ CYCLE (1)

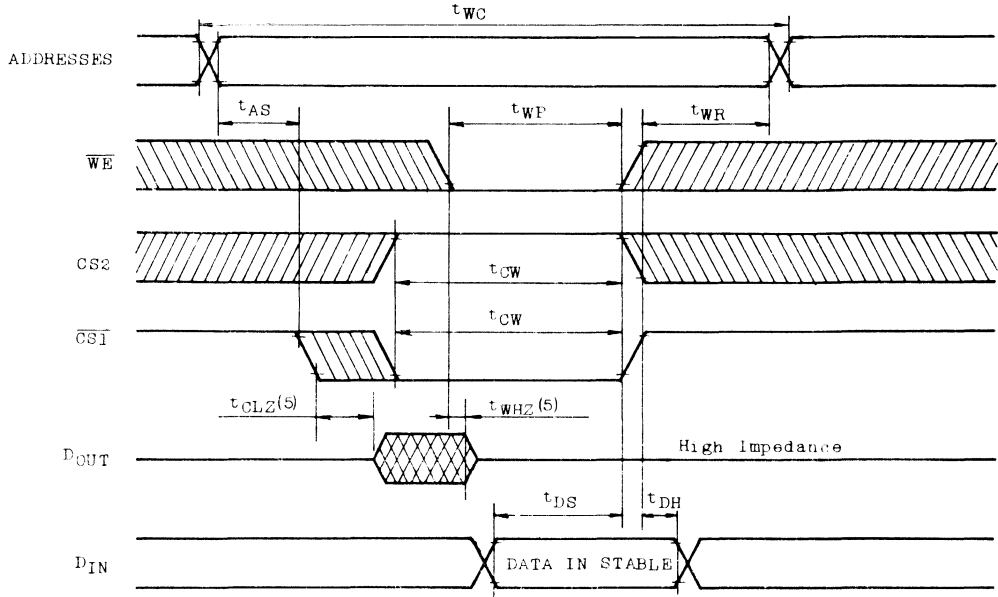


### ● WRITE CYCLE 1 (4) ( $\overline{WE}$ Controlled Write)

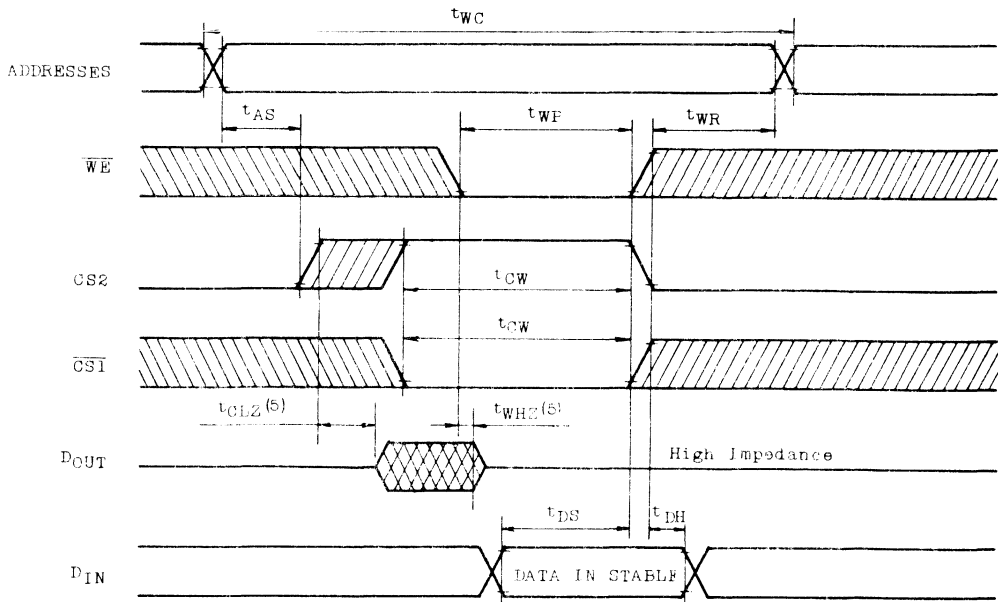


# TMM2089C-35, TMM2089C-45 TMM2089C-55

## ● WRITE CYCLE 2 (4) (CS1 Controlled Write)



## ● WRITE CYCLE 3 (4) (CS2 Controlled Write)



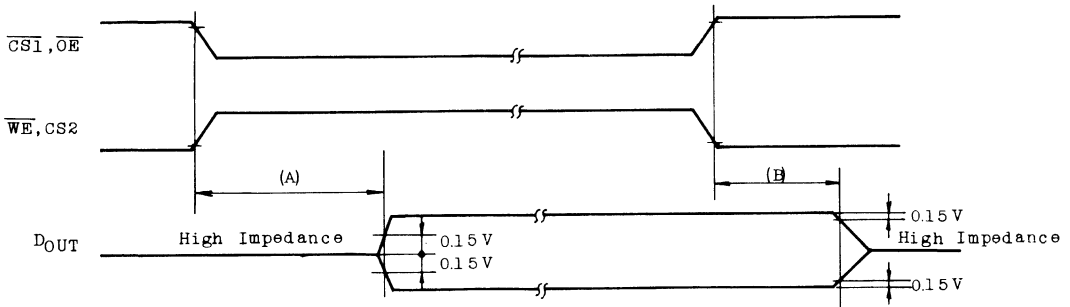
# TMM2089C-35, TMM2089C-45 TMM2089C-55

NOTE :

1.  $\overline{WE}$  is High for Read Cycle.
2. Assuming that  $\overline{CS1}$  Low transition or  $CS2$  High transition occurs coincident with or after  $\overline{WE}$  Low transition, Outputs remain in a high impedance state.
3. Assuming that  $\overline{CS1}$  High transition or  $CS2$  Low transition occurs coincident with or prior to  $\overline{WE}$  High transition, Outputs remain in a high impedance state.
4. Assuming that  $\overline{OE}$  is High for Write Cycle, Outputs are in high impedance state during this period.
5. These parameters are specified as follows and measured by using the load in Fig. 1.

(A)  $t_{CLZ}, t_{OLZ}, t_{WLZ}$ .....Output Enable Time

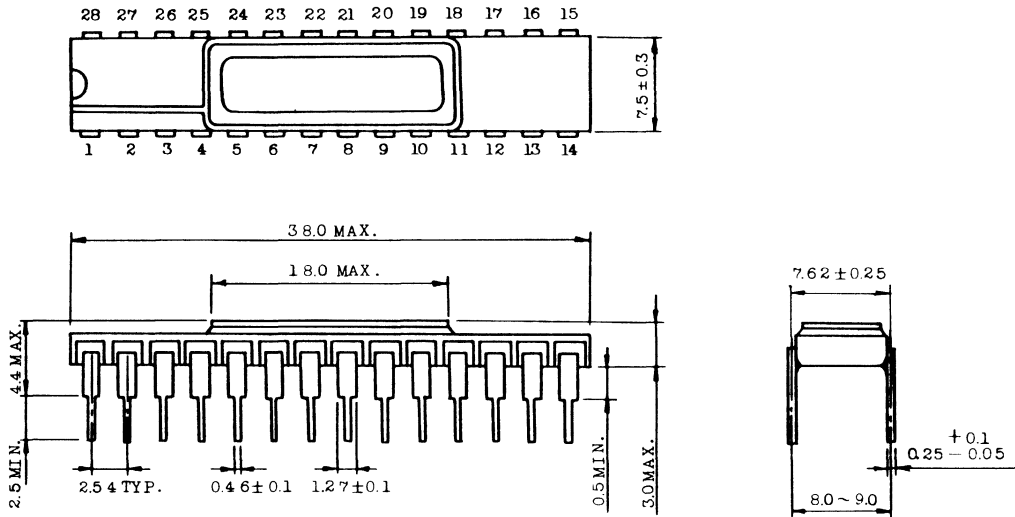
(B)  $t_{CHZ}, t_{OHZ}, t_{WHZ}$ .....Output Disable Time



# TMM2089C-35, TMM2089C-45 TMM2089C-55

## OUTLINE DRAWINGS

Unit: mm



Note : Each lead pitch is 2.54mm.

All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.28 leads.

**TMM2089C-35, TMM2089C-45  
TMM2089C-55**

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.  
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# TOSHIBA MOS MEMORY PRODUCT

8,192 WORD × 9 BIT STATIC RAM  
N-CHANNEL SILICON GATE MOS

**TMM2089P-35, TMM2089P-45**  
**TMM2089P-55**

## DESCRIPTION

The TMM2089P is a 73,728 bits high speed N-channel silicon gate MOS static random access memory organized as 8,192 words by 9 bits and operates from a single 5-volt supply. The TMM2089P features an automatic stand-by mode when deselected by  $\overline{CS1}$  signal. Thus the TMM2089P is suitable for use in cache memory and high speed storage. The TMM2089P has nine I/O terminals, therefore it is most suitable for MEMORY SYSTEM with Parity bit. The TMM2089P is offered in a 28 pin standard plastic dual in-line package with 0.3 inch width for high density assembly.

## FEATURES

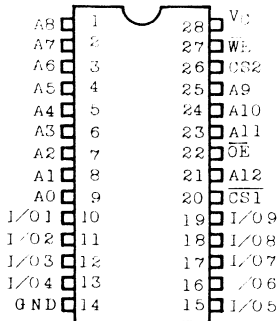
### • Access Time and Current

Parameter Part Number	Access Time (MAX.)	Operating Current (MAX.)	Standby Current (MAX.)
TMM2089P-35	35ns	135mA	15mA
TMM2089P-45	45ns	135mA	15mA
TMM2089P-55	55ns	135mA	15mA

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature: ( $\overline{CS1}$ )
- Output Buffer Control: ( $\overline{OE}$ )
- Three State Outputs
- All Inputs and Outputs: (Directly TTL Compatible)

- Inputs Protected: (All inputs have protection against static charge.)

## PIN CONNECTION



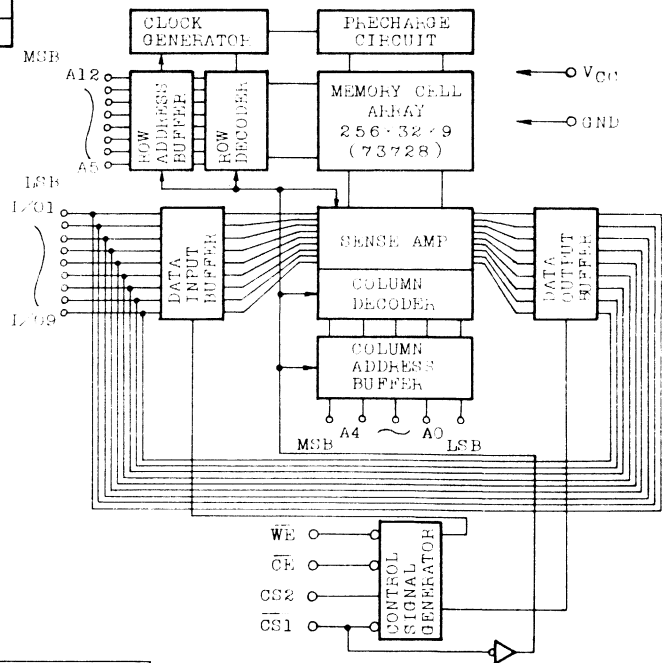
## PIN NAMES

A0 ~ A12	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{CS1}$ , CS2	Chip Select Inputs
I/O1 ~ I/O9	Data Input/Output
VCC	Power (+5V)
GND	Ground

## OPERATION MODE

MODE	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	I/O1 ~ 9	Power
Write	L	H	*	L	In	Active
Read	L	H	L	H	Out	Active
Standby	H	*	*	*	High-Z	Standby
Standby	L	L	*	*	High-Z	Active
Output Buffer Disable	L	H	H	H	High-Z	Active

## BLOCK DIAGRAM



# TMM2089P-35, TMM2089P-45 TMM2089P-55

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	Power Supply Voltage	-3.5 ~ 7.0	V
V <sub>IN</sub> , V <sub>OUT</sub>	Input Output Voltage	-3.5 ~ 7.0	V
T <sub>opr.</sub>	Operating Temperature	0 ~ 70	°C
T <sub>stg.</sub>	Storage Temperature	-55 ~ 150	°C
T <sub>solder</sub>	Soldering Temperature · Time	260 · 10	°C·sec
P <sub>D</sub>	Power Dissipation (Ta=70°C)	1.0	W

## D.C. RECOMMENDED OPERATING CONDITIONS (Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input Low Voltage	-3.0*	-	0.8	V
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V

\* Pulse Width: 10ns, DC: -0.5V(Min.)

## D.C. CHARACTERISTICS (Ta=0 ~ 70°C, V<sub>CC</sub>=5.0V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> =0V ~ 5.5V	-1.0	1.0	μA
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> =2.4V	-4.0	-	mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> =0.4V	8.0	-	mA
I <sub>LO</sub>	Output Leakage Current	$\overline{CS1}=V_{IH}$ or $CS2=V_{IL}$ or $\overline{WE}=V_{IL}$ or $\overline{OE}=V_{IH}$ , V <sub>OUT</sub> =0V ~ 5.5V	-1.0	1.0	μA
I <sub>SBP</sub>	Peak Power-on Current	$\overline{CS1}=V_{CC}$ , CS2=0V, I <sub>OUT</sub> =0mA	-	30	mA
I <sub>SB</sub>	Standby Current	$\overline{CS1}=V_{IH}$ , I <sub>OUT</sub> =0mA	-	15	mA
I <sub>CC</sub>	Operating Current	$\overline{CS1}=V_{IL}$ , I <sub>OUT</sub> =0mA	-	135	mA

## CAPACITANCE\* (Ta=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =0V	8	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>IN</sub> =0V	10	

\* Note: This parameter is periodically sampled and is not 100% tested.

# TMM2089P-35, TMM2089P-45 TMM2089P-55

## A.C. CHARACTERISTICS (Ta=0 ~ 70°C, VCC=5V±10%)

### READ CYCLE

SYMBOL	PARAMETER	TMM2080P-35		TMM2089P-45		TMM2089P-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	35	-	45	-	55	-	ns
t <sub>ACC</sub>	Address Access Time	-	35	-	45	-	55	
t <sub>CO1</sub>	CS1 Access Time	-	35	-	45	-	45	
t <sub>CO2</sub>	CS2 Access Time	-	25	-	25	-	30	
t <sub>OE</sub>	$\overline{OE}$ Access Time	-	20	-	20	-	25	
t <sub>OH</sub>	Output Data Hold Time from Address Change	5	-	5	-	5	-	
t <sub>CLZ</sub>	Output Enable Time from $\overline{CS1}$ or CS2	0	-	5	-	5	-	
t <sub>CHZ</sub>	Output Disable Time from $\overline{CS1}$ or CS2	-	20	-	20	-	20	
t <sub>OLZ</sub>	Output Enable Time from $\overline{OE}$	0	-	0	-	0	-	
t <sub>OHZ</sub>	Output Disable Time from $\overline{OE}$	-	15	-	15	-	20	
t <sub>PU</sub>	Chip Selection to Power Up Time	0	-	0	-	0	-	
t <sub>PD</sub>	Chip Deselection to Power Down Time	-	30	-	30	-	30	

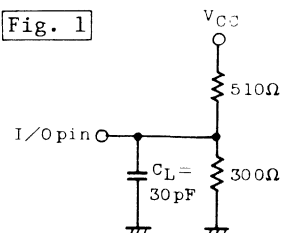
### WRITE CYCLE

SYMBOL	PARAMETER	TMM2089P-35		TMM2089P-45		TMM2089P-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	35	-	45	-	55	-	ns
t <sub>CS</sub>	Chip Selection to End of Write	30	-	40	-	50	-	
t <sub>AS</sub>	Address Set Up Time	0	-	0	-	0	-	
t <sub>WP</sub>	Write Pulse Width	25	-	35	-	45	-	
t <sub>WR</sub>	Write Recovery Time	0	-	0	-	0	-	
t <sub>Ds</sub>	Data Set Up Time	15	-	20	-	20	-	
t <sub>DH</sub>	Data Hold Time	0	-	0	-	0	-	
t <sub>WLZ</sub>	Output Enable Time from $\overline{WE}$	0	-	0	-	0	-	
t <sub>WHZ</sub>	Output Disable Time from $\overline{WE}$	-	15	-	15	-	20	

## A.C. TEST CONDITIONS

Input Pulse Levels	0.0V/3.0V
Input Rise and Fall Time	5ns
Input and Output Reference Levels	2.0V/0.8V
Output Load	Fig. 1

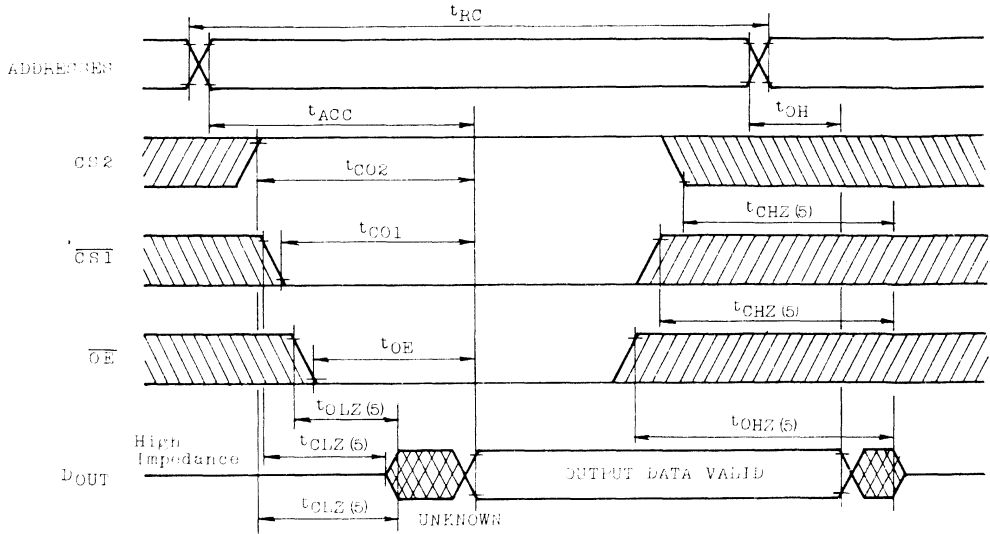
Fig. 1



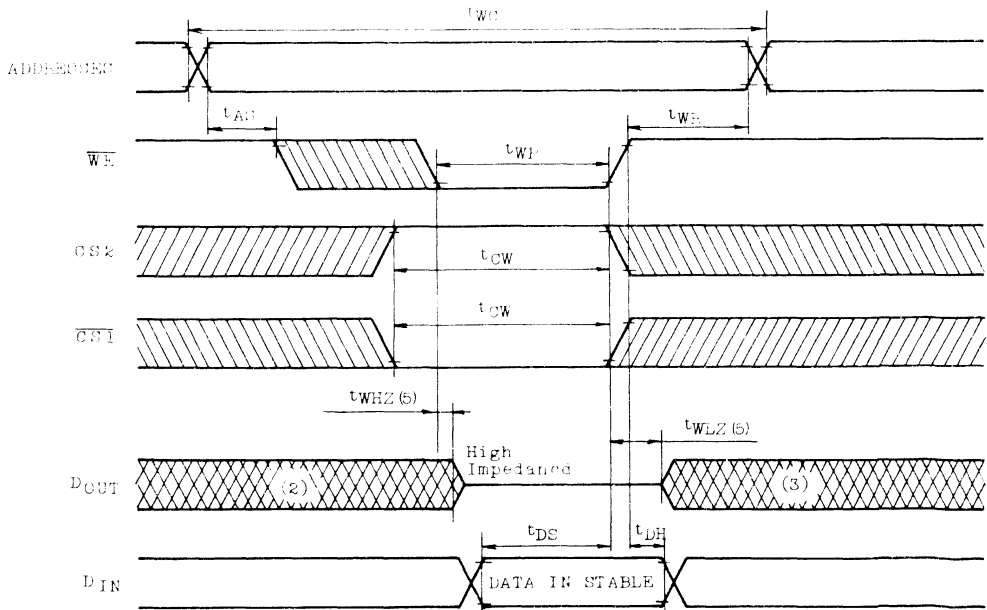
# TMM2089P-35, TMM2089P-45 TMM2089P-55

## TIMING WAVEFORMS

### READ CYCLE (1)

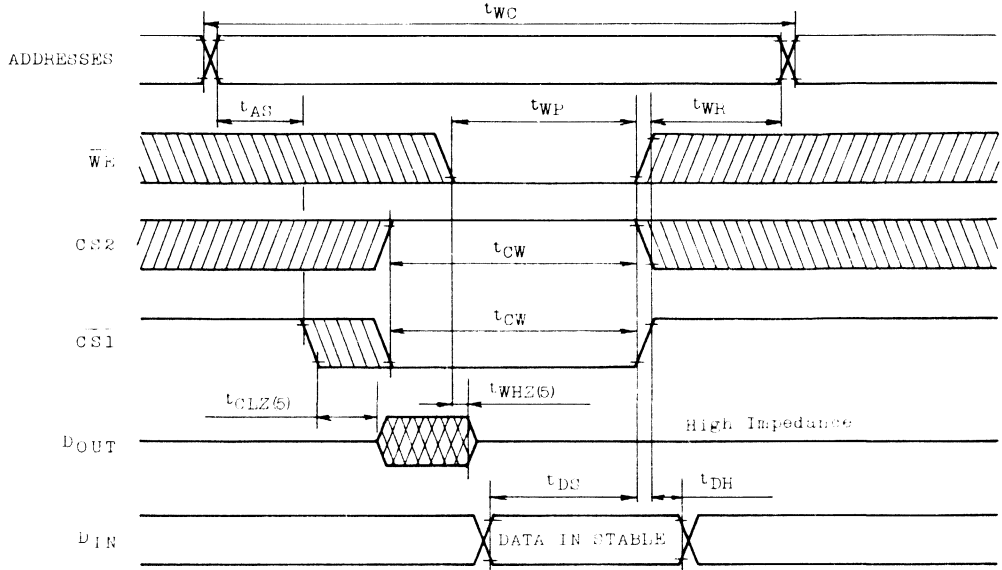


### WRITE CYCLE 1 (4) ( $\overline{WE}$ Controlled Write)

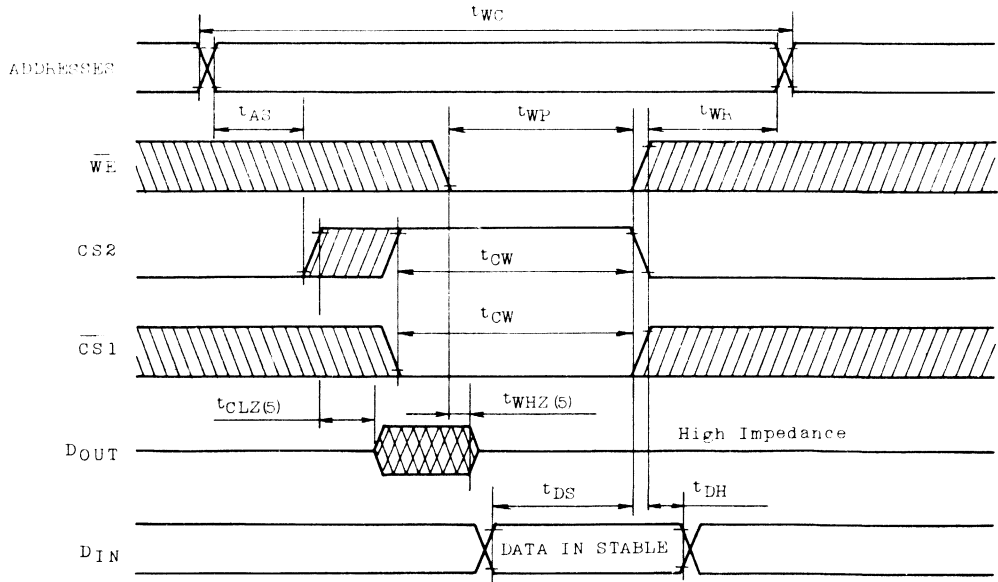


# TMM2089P-35, TMM2089P-45 TMM2089P-55

WRITE CYCLE 2 (4) ( $\overline{CS1}$  Controlled Write)



WRITE CYCLE 3 (4) ( $CS2$  Controlled Write)

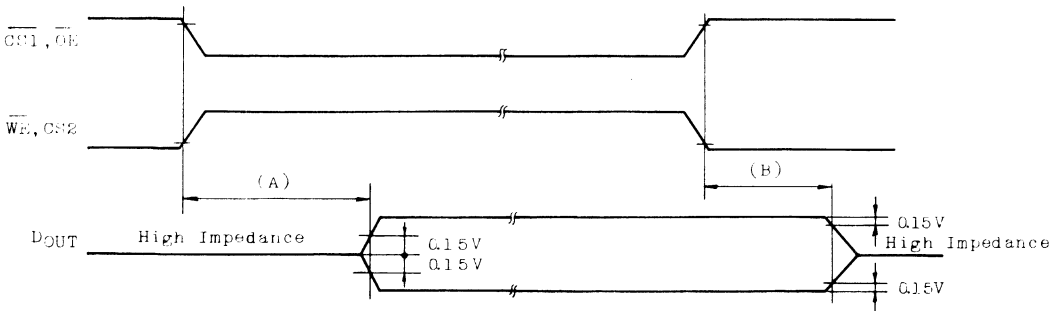


# TMM2089P-35, TMM2089P-45 TMM2089P-55

- Note: 1.  $\overline{WE}$  is High for Read Cycle.
2. Assuming that  $\overline{CS1}$  Low transition or CS2 High transition occurs coincident with or after  $\overline{WE}$  Low transition, Outputs remain in a high impedance state.
  3. Assuming that  $\overline{CS1}$  High transition or CS2 Low transition occurs coincident with or prior to  $\overline{WE}$  High transition, Outputs remain in a high impedance state.
  4. Assuming that  $\overline{OE}$  is High for Write Cycle, Outputs are in high impedance state during this period.
  5. These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A)  $t_{CLZ}, t_{OLZ}, t_{WLZ}$  ..... Output Enable Time

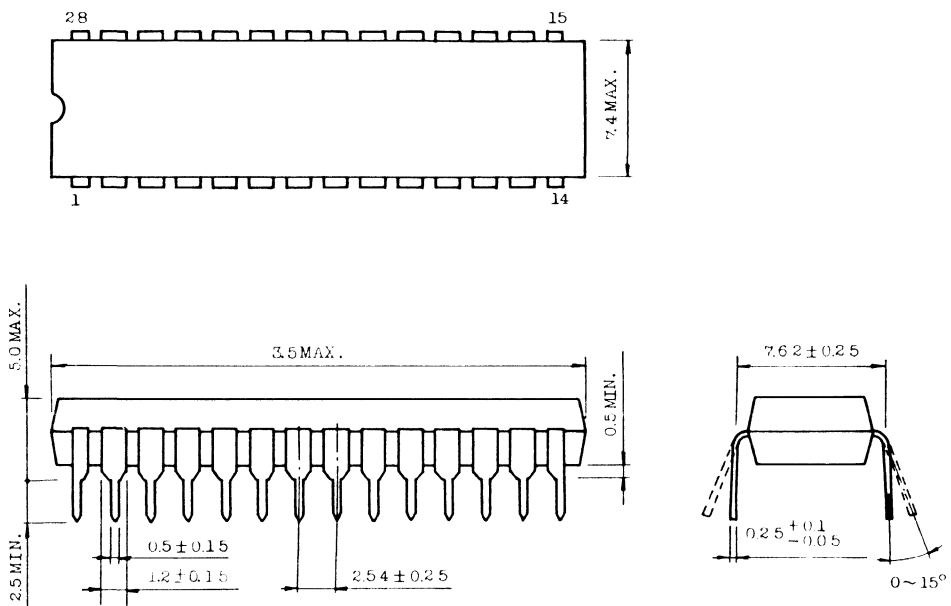
(B)  $t_{CHZ}, t_{OHZ}, t_{WHZ}$  ..... Output Disable Time



# TMM2089P-35, TMM2089P-45 TMM2089P-55

DIP 28 PIN OUTLINE DRAWING

Unit in mm



Note) Lead pitch is 2.54 and tolerance is  $\pm 0.25$  against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.





# TOSHIBA MOS MEMORY PRODUCT

**65,536 WORD × 1 BIT CMOS STATIC RAM**  
SILICON GATE CMOS

**TC5561P-55**  
**TC5561P-70**

## DESCRIPTION

The TC5561P is a 65,536 bit high speed static random access memory organized as 65,536 words by 1 bit using CMOS technology, and Operated from a single 5-volt supply.

Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 55ns/70ns and maximum operating current of 100mA at minimum cycle time.

The TC5561P also features an automatic stand-by mode. When deselected by Chip Enable (CE), the

operating current is reduced from 100mA to 100 $\mu$ A.

The TC5561P is suitable for use in main memory of high speed computer and pattern memory, where high speed/low power/high density are required.

The TC5561P is moulded in a 22 pin standard plastic package with 0.3 inch width for high density assembly.

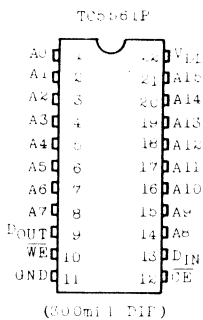
The TC5561P is fabricated with ion implanted COMS silicon gate MOS technology for high performance and high reliability.

## FEATURES

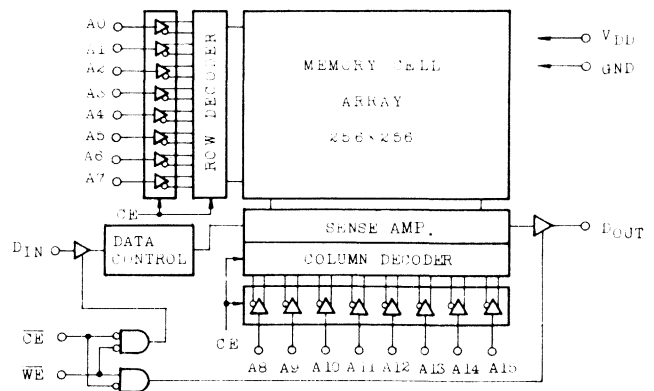
- Fast access time : TC5561P-55 55ns(MAX.)  
TC5561P-70 70ns(MAX.)
- Low power dissipation : Operation 100mA(MAX.)  
Standby 100 $\mu$ A(MAX.)
- 5V single power supply

- Fully static operation
- Directly TTL compatible : All Input and Output
- I/O separate
- Package : 22 pin standard plastic package, 300mil width

## PIN CONNECTION (TOP VIEW)



## BLOCK DIAGRAM



## PIN NAMES

A <sub>0</sub> ~A <sub>15</sub>	Address Inputs
D <sub>IN</sub>	Data Input
D <sub>OUT</sub>	Data Output
CE	Chip Enable Input
WE	Write Enable Input
V <sub>DD</sub>	Power (+ 5V)
GND	Ground

# TC5561P-55

# TC5561P-70

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.3~7.0	V
V <sub>IN</sub>	Input Voltage	-2.0~7.0	V
V <sub>OUT</sub>	Output Voltage	-0.5~V <sub>DD</sub> +0.5	V
P <sub>D</sub>	Power Dissipation	650	mW
T <sub>SOLDER</sub>	Soldering Temperature	260 · 10	°C·sec
T <sub>STG</sub>	Storage Temperature	-65~150	°C
T <sub>OPR</sub>	Operating Temperature	0~70	°C

## D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-3.0	—	0.8	V
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	—	5.5	V

## D. C. and OPERATING CHARACTERISTICS (T<sub>a</sub> = 0~70°C, V<sub>DD</sub> = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0~V <sub>DD</sub>	—	—	±1.0	μA
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4V	-8	—	—	mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4V	8	—	—	mA
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V <sub>OUT</sub> = 0~V <sub>DD</sub>	—	—	±1.0	μA
I <sub>DDO</sub>	Operating Current	V <sub>DD</sub> = 5.5V, t <sub>cycle</sub> = Min cycle, $\overline{CE} = V_{IL}$ Other Input = V <sub>IH</sub> /V <sub>IL</sub>	—	—	100	mA
I <sub>DDs1</sub>	Standby Current	$\overline{CE} = V_{IH}$	—	—	2	mA
I <sub>DDs2</sub>		$\overline{CE} = V_{DD} - 0.2V$	—	—	100	μA

## CAPACITANCE (T<sub>a</sub> = 25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = GND	10	pF

Note : This parameter periodically sampled is not 100% tested.

# TC5561P-55 TC5561P-70

## A. C. CHARACTERISTICS (Ta = 0~70°C, VDD = 5V ± 10%)

### Read Cycle

SYMBOL	PARAMETER	TC5561P-55		TC5561P-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	55	—	70	—	ns
t <sub>ACC</sub>	Address Access Time	—	55	—	70	
t <sub>CO</sub>	Chip Enable Access Time	—	55	—	70	
t <sub>COE</sub>	Chip Enable to Output in Low-Z	5	—	5	—	
t <sub>COD</sub>	Chip Disable to Output in High-Z	—	30	—	30	
t <sub>OH</sub>	Output Data Hold Time	5	—	5	—	

### Write Cycle

SYMBOL	PARAMETER	TC5561P-55		TC5561P-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	55	—	70	—	ns
t <sub>WP</sub>	Write Pulse Width	35	—	35	—	
t <sub>OW</sub>	Chip Enable to End of Write	35	—	35	—	
t <sub>AS</sub>	Address Set up Time	0	—	0	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	
t <sub>OE<sub>W</sub></sub>	WE to Output Low-Z	0	—	0	—	
t <sub>OD<sub>W</sub></sub>	WE to Output High-Z	—	30	—	30	
t <sub>DS</sub>	Data Set up Time	35	—	35	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	

## A. C. TEST CONDITIONS

Input Pulse Levels	2.4V/0.6V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

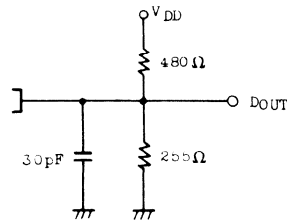
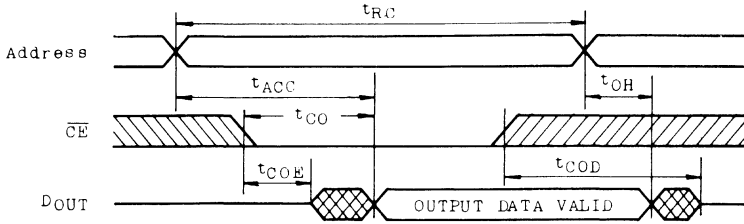


Fig.1 Output Load

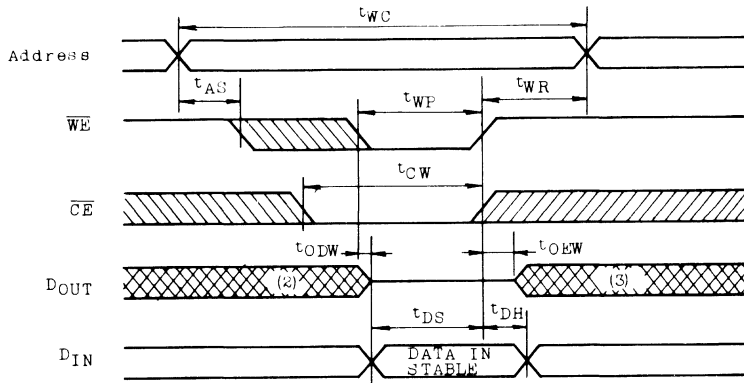
# TC5561P-55 TC5561P-70

## TIMING WAVEFORMS

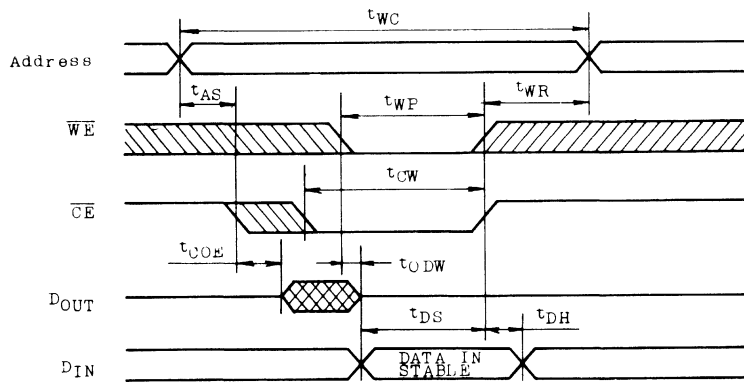
### ● READ CYCLE (1)



### ● WRITE CYCLE 1 ( $\overline{WE}$ Controlled Write)



### ● WRITE CYCLE 2 ( $\overline{CE}$ Controlled Write)



Note :

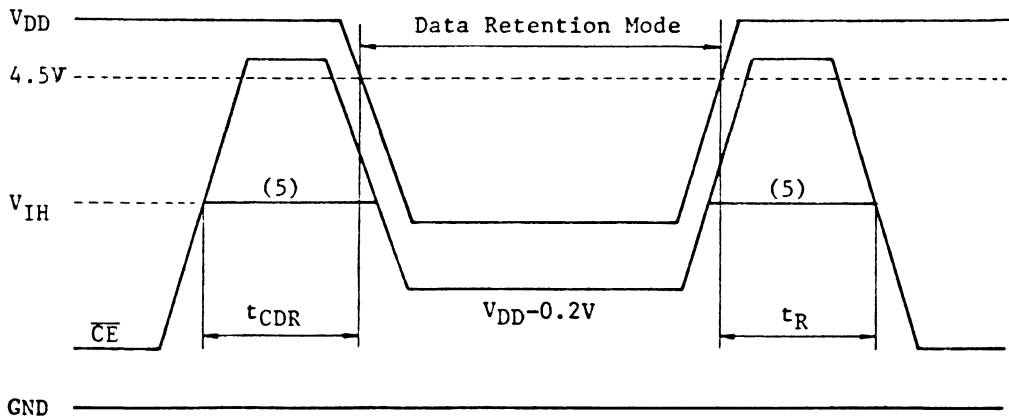
1.  $\overline{WE}$  is High for Read Cycle.
2. Assuming that  $\overline{CE}$  Low transition occurs coincident with or after  $\overline{WE}$  Low transition, Outputs remain in a high impedance state.
3. Assuming that  $\overline{CE}$  High transition occurs coincident with or prior to  $\overline{WE}$  High transition, Outputs remain in a high impedance state.
4. The operating temperature ( $T_a$ ) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

# TC5561P-55 TC5561P-70

## DATA RETENTION CHARACTERISTICS

(Ta: -40~50°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{DH}$	Data Retention Supply Voltage	2.0	—	5.5	V
$I_{DDS2}$	Standby Supply Current	$V_{DD}=3.0V$	—	50	$\mu A$
		$V_{DD}=5.5V$	—	100	$\mu A$
$t_{CDH}$	Chip Deselection to Data Retention Mode	0	—	—	$\mu S$
$t_R$	Recovery Time	$t_{RC}(1)$	—	—	$\mu S$

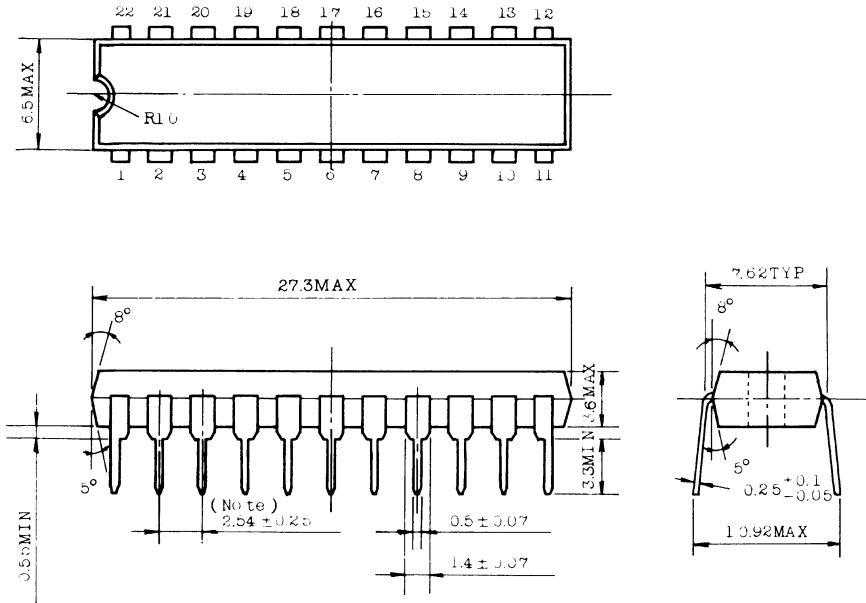


5. If the  $v_{IH}$  of  $\overline{CE}_1$  is 2.2V in operation,  $I_{DDS1}$  current flows the period that  $v_{DD}$  voltage is going down from 4.5V to 2.5V.

# TC5561P-55 TC5561P-70

## OUTLINE DRAWINGS

Unit in mm



Note : Each lead pitch is 2.54mm.

All leads are located within 0.25mm of the true longitudinal position with respect to No.1 and No.22 leads.

Note Toshiba does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry

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# TOSHIBA MOS MEMORY PRODUCT

**65,536 WORD × 1 BIT CMOS STATIC RAM**  
SILICON GATE CMOS

## TC5562P-45

## TC5562P-55

### DESCRIPTION

The TC5562P is a 65,536 bit high speed static random access memory organized as 65,536 words by 1 bit using CMOS technology, and operated from a single 5-volt supply.

Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 45ns/55ns and maximum operating current of 100mA at minimum cycle time.

The TC5562P also features and automatic stand-

by mode. When deselected by chip Enable ( $\overline{CE}$ ), the operating current is reduced from 100mA to 20mA.

The TC5562P is suitable for use in main memory of high speed/high density are required.

The TC5562P is moulded in a 22 pin standard plastic package with 0.3 inch width for high density assembly.

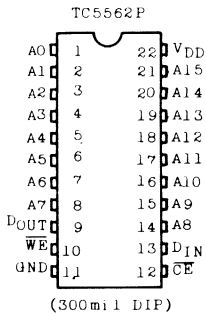
The TC5562P is fabricated with ion implanted COMS silicon gate MOS technology for high performance and high reliability.

### FEATURES

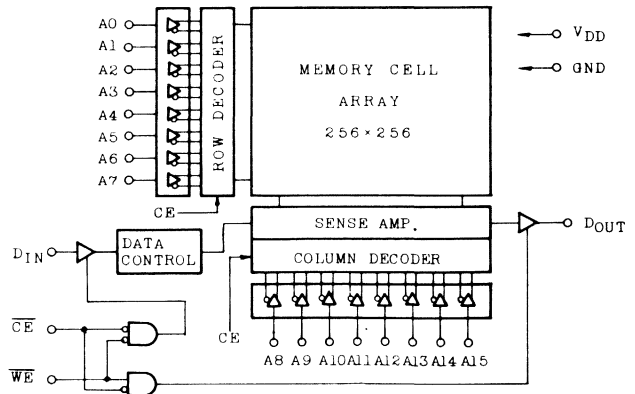
- Fast access time : TC5562P-45 45ns(MAX.)  
TC5562P-55 55ns(MAX.)
- Low power dissipation : Operation 100mA(MAX.)  
Standby 20mA(MAX.)
- 5V single power supply

- Fully Static operation
- Directly TTL compatible : All Input and Output
- I/O separate
- Package : 22 pin standard plastic package,  
300mil width

### PIN CONNECTION (TOP VIEW)



### BLOCK DIAGRAM



### PIN NAMES

A <sub>0</sub> ~A <sub>15</sub>	Address Inputs
D <sub>IN</sub>	Data Input
D <sub>OUT</sub>	Data Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V <sub>DD</sub>	Power (+5V)
GND	Ground

# TC5562P-45

# TC5562P-55

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.3~7.0	V
V <sub>IN</sub>	Input Voltage	-2.0~7.0	V
V <sub>OUT</sub>	Output Voltage	-0.5~V <sub>DD</sub> +0.5	V
P <sub>D</sub>	Power Dissipation	650	mW
T <sub>SOLDER</sub>	Soldering Temperature	260 · 10	°C·sec
T <sub>STG</sub>	Storage Temperature	-65~150	°C
T <sub>OPR</sub>	Operating Temperature	0~70	°C

## D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	3.0	—	0.8	V

## D. C and OPERATING CHARACTERISTICS (T<sub>a</sub>=0~70°C, V<sub>DD</sub>=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> =0~V <sub>DD</sub>	—	—	±1.0	μA
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> =2.4V	-8	—	—	mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> =0.4V	8	—	—	mA
I <sub>LO</sub>	Output Leakage Current	CE = V <sub>IH</sub> or WE = V <sub>IL</sub> V <sub>OUT</sub> =0~V <sub>DD</sub>	—	—	±1.0	μA
I <sub>DDO</sub>	Operating Current	V <sub>DD</sub> =5.5V, t <sub>cycle</sub> =Min cycle, CE = V <sub>IL</sub> Other Input = V <sub>IH</sub> /V <sub>IL</sub>	—	—	100	mA
I <sub>DDs1</sub>	Standby Current	CE = V <sub>IH</sub>	—	—	20	mA
I <sub>DDs2</sub>		CE = V <sub>DD</sub> -0.2V Other Input = V <sub>DD</sub> -0.2V or 0.2V	—	—	2	

## CAPACITANCE (T<sub>a</sub>=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> =GND	10	pF

Note : This parameter periodically sampled is not 100% tested.



# TC5562P-45 TC5562P-55

## A. C. CHARACTERISTICS (Ta = 0 ~ 70°C, VDD = 5V ± 10%)

### Read Cycle

SYMBOL	PARAMETER	TC5562P-45		TC5562P-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	45	—	55	—	ns
t <sub>ACC</sub>	Address Access Time	—	45	—	55	
t <sub>CO</sub>	Chip Enable Access Time	—	45	—	55	
t <sub>COE</sub>	Chip Enable to Output in Low-Z	5	—	5	—	
t <sub>COD</sub>	Chip Disable to Output in High-Z	—	25	—	30	
t <sub>OH</sub>	Output Data Hold Time	5	—	5	—	

### Write Cycle

SYMBOL	PARAMETER	TC5562P-45		TC5562P-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	45	—	55	—	ns
t <sub>WP</sub>	Write Pulse Width	30	—	35	—	
t <sub>CW</sub>	Chip Enable to End of Write	30	—	35	—	
t <sub>AS</sub>	Address Set up Time	0	—	0	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	
t <sub>OE<sub>W</sub></sub>	$\overline{WE}$ to Output Low-Z	0	—	0	—	
t <sub>OD<sub>W</sub></sub>	$\overline{WE}$ to Output High-Z	—	25	—	30	
t <sub>DS</sub>	Data Set up Time	30	—	35	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	

## A. C. TEST CONDITIONS

Input Pulse Levels	2.4V/0.6V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

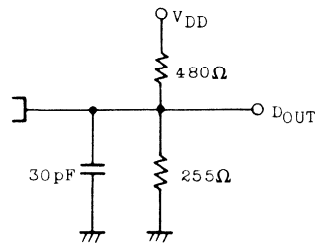


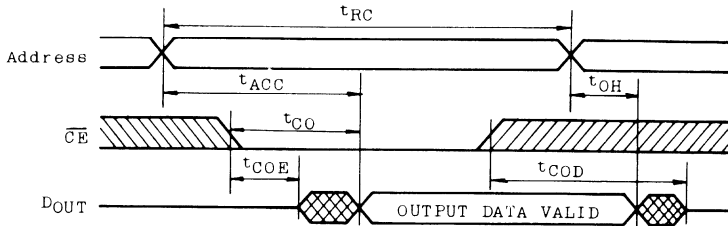
Fig.1 Output Load

# TC5562P-45

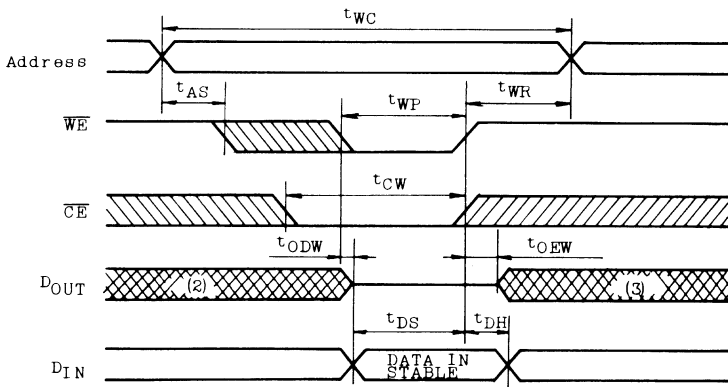
# TC5562P-55

## TIMING WAVEFORMS

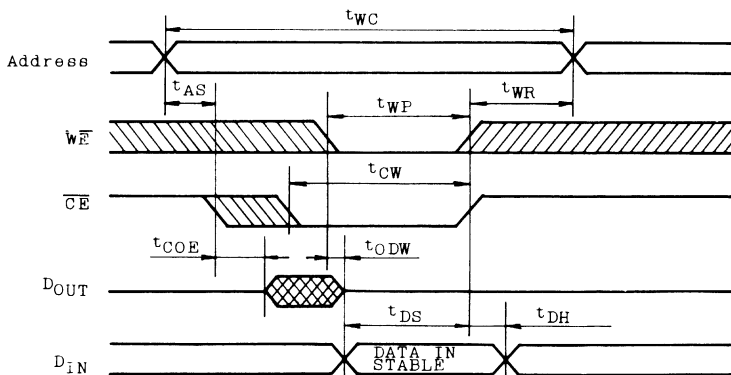
### ● READ CYCLE (1)



### ● WRITE CYCLE 1 ( $\overline{WE}$ Controlled Write)



### ● WRITE CYCLE 2 ( $\overline{CE}$ Controlled Write)



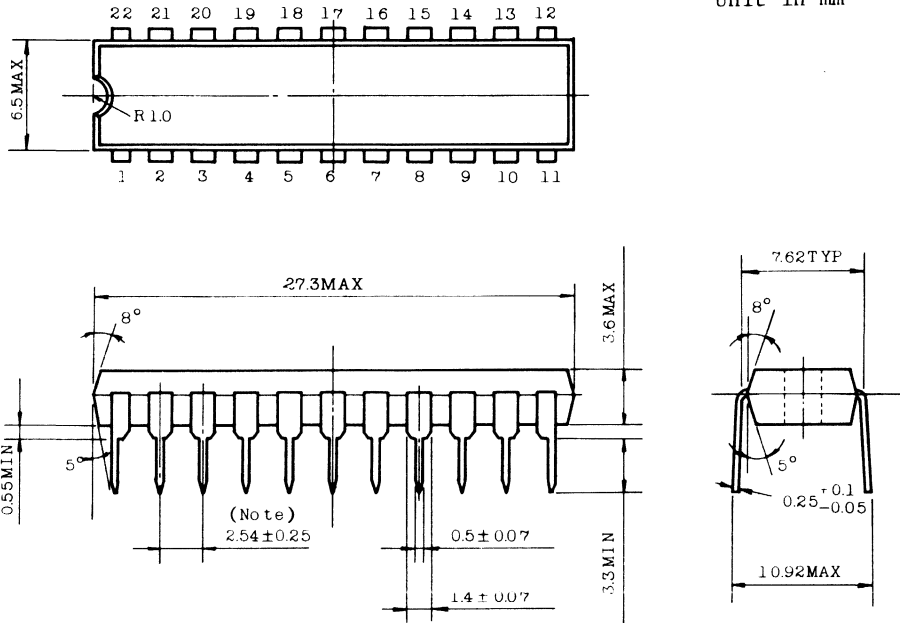
Note :

1.  $\overline{WE}$  is High for Read Cycle.
2. Assuming that  $\overline{CE}$  Low transition occurs coincident with or after  $\overline{WE}$  Low transition, Outputs remain in a high impedance state.
3. Assuming that  $\overline{CE}$  High transition occurs coincident with or prior  $\overline{WE}$  High transition, Outputs remain in a high impedance state.
4. The operating temperature ( $T_a$ ) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

**TC5562P-45**  
**TC5562P-55**

**OUTLINE DRAWINGS**

Unit in mm



Note : Each lead pitch is 2.54mm.  
 All leads are located within 0.25mm of the true longitudinal position with respect to No. 1 and No. 22 leads.

# **TC5562P-45**

# **TC5562P-55**

Note: Toshiba does not assume any responsibility for use of any cirtry described, no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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# TOSHIBA MOS MEMORY PRODUCT

16,384 WORD × 4 BIT CMOS STATIC RAM  
SILICON GATE CMOS

**TC55416P-35**  
**TC55416P-45**

## DESCRIPTION

The TC55416P is a 65,536 bit high speed static random access memory organized as 16,384 words by 4 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 35ns/45ns and maximum operating current of 80mA/60mA at minimum cycle time.

The TC55416P also features an automatic stand-by mode. When deselected by Chip Enable ( $\overline{CE}$ ), the operating current is reduced to 10mA.

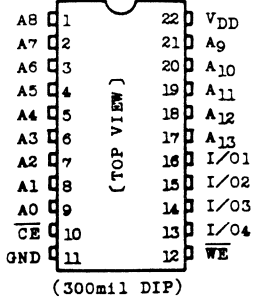
The TC55416P is suitable for use in cache memory and high speed storage, where high speed/high density are required.

The TC55416P is molded in a 22 pin standard plastic package with 0.3 inch width for high density assembly. The TC55416P is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

## FEATURES

- . Fast access time : TC55416P-35 35ns (Max.)  
TC55416P-45 45ns (Max.)
- . Low power dissipation : Operation TC55416P-35 80mA (Max.)  
TC55416P-45 60mA (Max.)  
Standby 10mA (Max.)
- . 5V single power supply
- . Fully static operation
- . Directly TTL compatible : All Input and Output
- . Package : 22 pins standard plastic package, 300 mil width.

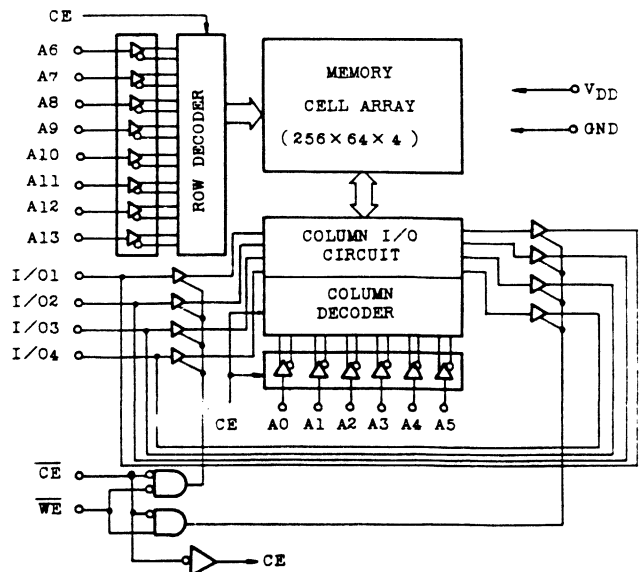
## PIN CONNECTION



## PIN NAMES

A0-A13	Address Inputs
I/O1-I/O4	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V <sub>DD</sub>	Power (+5V)
GND	Ground

## BLOCK DIAGRAM



# TC55416P-35

# TC55416P-45

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.3~7.0	V
V <sub>IN</sub>	Input Voltage	-2.0~7.0	.V
V <sub>OUT</sub>	Output Voltage	-0.5~V <sub>DD</sub> +0.5	V
P <sub>D</sub>	Power Dissipation	650	mW
T <sub>solder</sub>	Soldering Temperature	260·10	°C·sec
T <sub>stg</sub>	Storage Temperature	-65~150	°C
T <sub>opr</sub>	Operating Temperature	0~70	°C

## D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	-	0.8	V

## D.C. and OPERATING CHARACTERISTICS (T<sub>a</sub>=0~70°C, V<sub>DD</sub>=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> =0~V <sub>DD</sub>	-	-	±1.0	μA	
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> =2.4V	-4	-	-	mA	
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> =0.4V	8	-	-	mA	
I <sub>LO</sub>	Output Leakage Current	$\overline{CE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V <sub>OUT</sub> =0~V <sub>DD</sub>	-	-	±1.0	μA	
I <sub>DD0</sub>	Operating Current	V <sub>DD</sub> =5.5V t <sub>cycle</sub> =Min cycle $\overline{CE}=V_{IL}$ Other Input=V <sub>IH</sub> /V <sub>IL</sub>	-35	-	-	80	mA
			-45	-	-	60	
I <sub>DDs1</sub>	Standby Current	V <sub>DD</sub> =5.5V, t <sub>cycle</sub> =Min cycle $\overline{CE}=V_{IH}$ , Other Input=V <sub>IH</sub> /V <sub>IL</sub>	-	-	-	20	mA
I <sub>DDs2</sub>		$\overline{CE}=V_{DD}-0.2V$ Other Input=V <sub>DD</sub> -0.2V or 0.2V	-	-	-	1	

## CAPACITANCE (T<sub>a</sub>=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> =GND	10	pF

Note: This parameter periodically sampled is not 100% tested.

# TC55416P-35

# TC55416P-45

A.C. CHARACTERISTICS (Ta=0-70°C, VDD=5V±10%)

### Read Cycle

SYMBOL	PARAMETER	TC55416P-35		TC55416P-45		UNIT
		MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	35	-	45	-	ns
t <sub>ACC</sub>	Address Access Time	-	35	-	45	ns
t <sub>CO</sub>	Chip Enable Access Time	-	35	-	45	ns
t <sub>COE</sub>	Chip Enable to Output in Low-Z	0	-	0	-	ns
t <sub>COD</sub>	Chip Enable to Output in High-Z	-	15	-	20	ns
t <sub>OH</sub>	Output Data Hold Time	5	-	5	-	ns

### Write Cycle

SYMBOL	PARAMETER	TC55416P-35		TC55416P-45		UNIT
		MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	35	-	45	-	ns
t <sub>WP</sub>	Write Pulse Width	30	-	35	-	ns
t <sub>CW</sub>	Chip Enable to End of Write	30	-	35	-	ns
t <sub>AS</sub>	Address Set Up Time	0	-	0	-	ns
t <sub>WR</sub>	Write Recovery Time	0	-	0	-	ns
t <sub>ODW</sub>	$\overline{WE}$ to Output High-Z	-	15	-	15	ns
t <sub>OEW</sub>	$\overline{WE}$ to Output Low-Z	0	-	0	-	ns
t <sub>DS</sub>	Data Set Up Time	15	-	20	-	ns
t <sub>DH</sub>	Data Hold Time	0	-	0	-	ns

### A.C. TEST CONDITIONS

Input Pulse Levels	0.6V, 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.8V, 2.0V
Output Load	See Fig.1

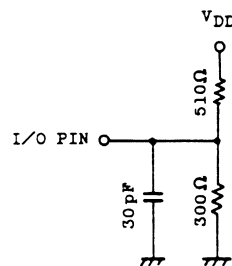


Fig.1 OUTPUT LOAD

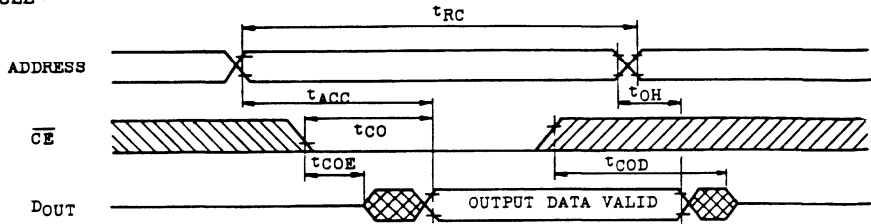
Note: In all condition, t<sub>COD</sub> max is less than t<sub>COE</sub> min both for a given device and from device to device.

# TC55416P-35

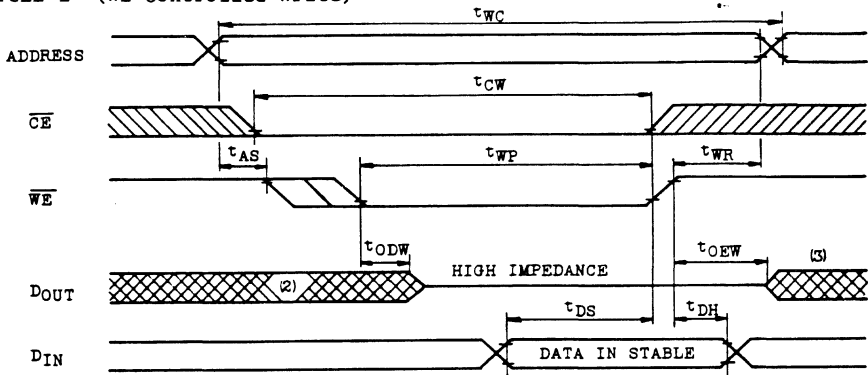
# TC55416P-45

## TIMING WAVEFORMS

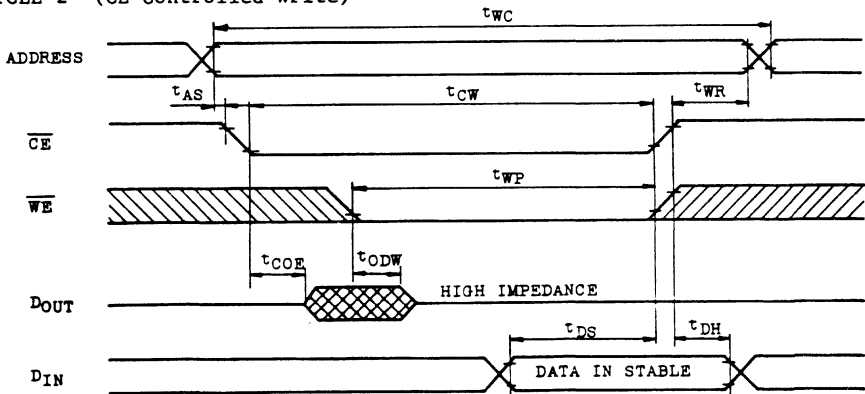
### READ CYCLE (1)



### WRITE CYCLE 1 ( $\overline{WE}$ Controlled Write)



### WRITE CYCLE 2 ( $\overline{CE}$ Controlled Write)



Note: 1.  $\overline{WE}$  is High for Read Cycle.

2. Assuming that  $\overline{CE}$  Low transition occurs coincident with or after  $\overline{WE}$  Low transition, Outputs remain in a high impedance state.

3. Assuming that  $\overline{CE}$  High transition occurs coincident with or prior to  $\overline{WE}$  High transition, Outputs remain in a high impedance state.

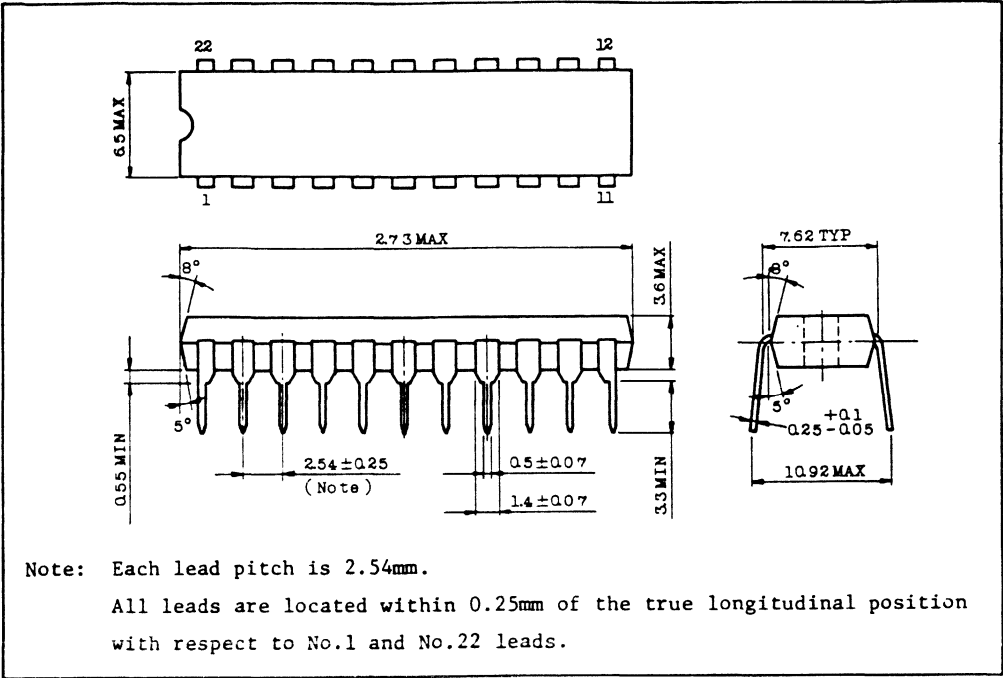
4. The Operating temperature ( $T_a$ ) is guaranteed with transverse air flow exceeding 400 linear feet per minute.



# TC55416P-35 TC55416P-45

OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54mm.  
All leads are located within 0.25mm of the true longitudinal position with respect to No.1 and No.22 leads.



# TOSHIBA MOS MEMORY PRODUCT

16,384 WORD × 4 BIT CMOS STATIC RAM  
SILICON GATE CMOS

TC55417P-35  
TC55417P-45

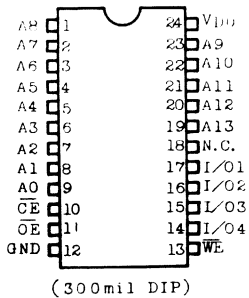
## DESCRIPTION

The TC55417P is a 65,536 bit high speed static random access memory organized as 16,384 words by 4 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 35ns/45ns and maximum operating current of 80mA/60mA at minimum cycle time. The TC55417P also features an automatic stand-by mode. When deselected by Chip Enable ( $\overline{CE}$ ), the operating current is reduced to 10mA. The TC55417P is suitable for use in cache memory and high speed storage, where high speed/high density are required. The TC55417P is molded in a 24 pin standard plastic package with 0.3 inch width for high density assembly. The TC55417P is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

## FEATURES

- Fast access time : TC55417P-35 35ns (Max.)  
TC55417P-45 45ns (Max.)
- Low power dissipation: Operation TC55417P-35 80mA (Max.)  
TC55417P-45 60mA (Max.)  
Standby 10mA (Max.)
- 5V single power supply
- Fully static operation
- Directly TTL compatible: All Input and Output
- Output buffer control :  $\overline{OE}$
- Package : 24 pins standard plastic package, 300 mil width.

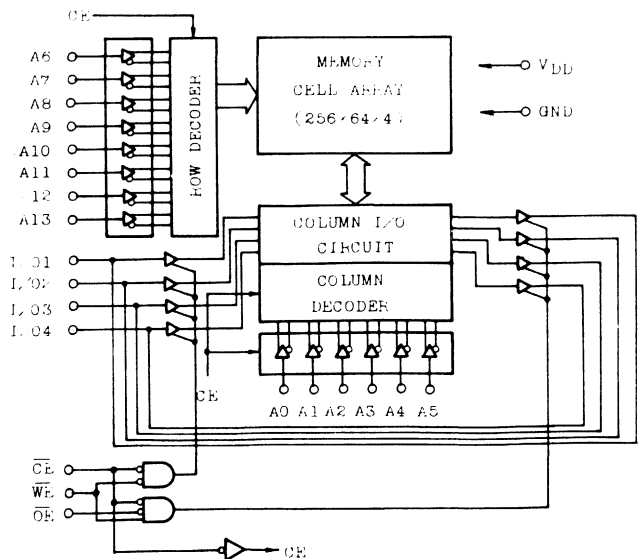
## PIN CONNECTION



## PIN NAMES

A0 ~ A13	Address Inputs
I/O1 ~ I/O4	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V <sub>DD</sub>	Power (+5V)
GND	Ground
N.C.	No Connection

## BLOCK DIAGRAM



# TC55417P-35

# TC55417P-45

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.3 ~ 7.0	V
V <sub>IN</sub>	Input Voltage	-2.0 ~ 7.0	V
V <sub>OUT</sub>	Output Voltage	-0.5 ~ V <sub>DD</sub> +0.5	V
P <sub>D</sub>	Power Dissipation	650	mW
T <sub>solder</sub>	Soldering Temperature · Time	260 · 10	°C·sec
T <sub>stg</sub>	Storage Temperature	-65 ~ 150	°C
T <sub>opr</sub>	Operating Temperature	0 ~ 70	°C

## D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	-	0.8	V

## D.C. and OPERATING CHARACTERISTICS (Ta=0 ~ 70°C, V<sub>DD</sub>=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> =0 ~ V <sub>DD</sub>	-	-	±1.0	μA	
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> =2.4V	-4	-	-	mA	
I <sub>OL</sub>	Output low Current	V <sub>OL</sub> =0.4V	8	-	-	mA	
I <sub>LO</sub>	Output Leakage Current	$\overline{CE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V <sub>OUT</sub> =0 ~ V <sub>DD</sub>	-	-	±1.0	μA	
I <sub>DD0</sub>	Operating Current	V <sub>DD</sub> =5.5V t <sub>cycle</sub> =Min cycle $\overline{CE}=V_{IL}$ Other Input=V <sub>IH</sub> /V <sub>IL</sub>	-35	-	-	80	mA
			-45	-	-	60	
I <sub>DDs1</sub>	Standby Current	V <sub>DD</sub> =5.5V, t <sub>cycle</sub> =Min cycle $\overline{CE}=V_{IH}$ , Other Input=V <sub>IH</sub> /V <sub>IL</sub>	-	-	-	20	mA
I <sub>DDs2</sub>		$\overline{CE}=V_{DD}-0.2V$ Other Input=V <sub>DD</sub> -0.2V or 0.2V	-	-	-	1	

## CAPACITANCE (Ta=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> =GND	10	pF

Note: This parameter periodically sampled is not 100% tested.

# TC55417P-35

# TC55417P-45

A.C. CHARACTERISTICS (Ta=0 ~ 70°C, V<sub>DD</sub>=5V±10%)

## Read Cycle

SYMBOL	PARAMETER	TC55417P-35		TC55417P-45		UNIT
		MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	35	-	45	-	ns
t <sub>ACC</sub>	Address Access Time	-	35	-	45	ns
t <sub>CO</sub>	Chip Enable Access Time	-	35	-	45	ns
t <sub>OE</sub>	Output Enable to Output Valid	-	20	-	20	ns
t <sub>COE</sub>	Chip Enable to Output in Low-Z	0	-	0	-	ns
t <sub>COD</sub>	Chip Enable to Output in High-Z	-	15	-	20	ns
t <sub>OEE</sub>	Output Enable to Output in Low-Z	0	-	0	-	ns
t <sub>ODO</sub>	Output Disable to Output in High-Z	-	15	-	15	ns
t <sub>OH</sub>	Output Data Hold Time	5	-	5	-	ns

## Write Cycle

SYMBOL	PARAMETER	TC55417P-35		TC55417P-45		UNIT
		MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	35	-	45	-	ns
t <sub>WP</sub>	Write Pulse Width	30	-	35	-	ns
t <sub>CW</sub>	Chip Enable to End of Write	30	-	35	-	ns
t <sub>AS</sub>	Address Set Up Time	0	-	0	-	ns
t <sub>WR</sub>	Write Recovery Time	0	-	0	-	ns
t <sub>ODW</sub>	$\overline{WE}$ to Output High-Z	-	15	-	15	ns
t <sub>OEW</sub>	$\overline{WE}$ to Output Low-Z	0	-	0	-	ns
t <sub>Ds</sub>	Data Set Up Time	15	-	20	-	ns
t <sub>DH</sub>	Data Hold Time	0	-	0	-	ns

## A.C. TEST CONDITIONS

Input Pulse Levels	0.6V, 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.8V, 2.0V
Output Load	See Fig. 1

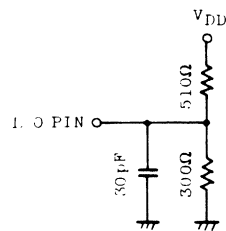


Fig. 1 OUTPUT LOAD

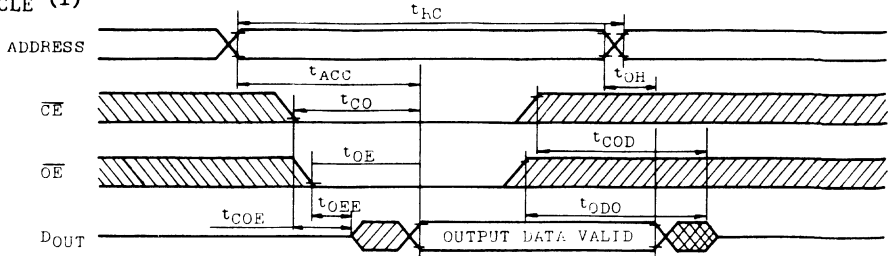
Note: In all condition, t<sub>COD</sub> max is less than t<sub>COE</sub> min both for a given device and from device to device.

# TC55417P-35

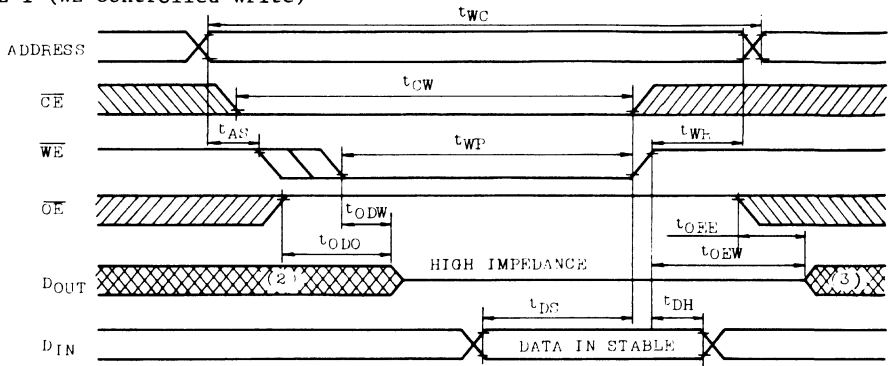
# TC55417P-45

## TIMING WAVEFORMS

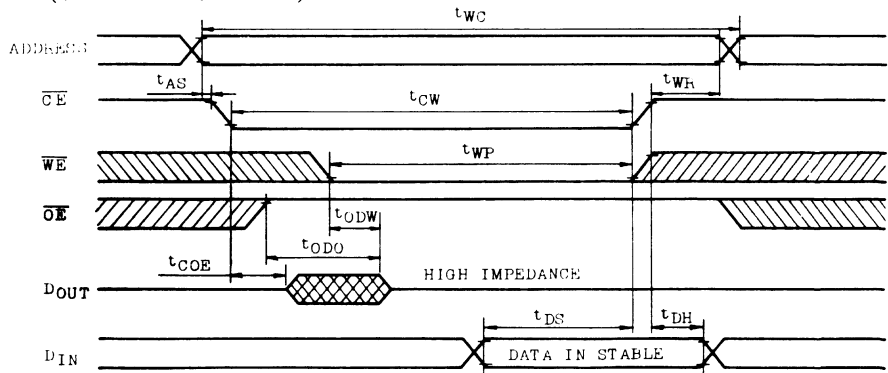
### READ CYCLE (1)



### WRITE CYCLE 1 ( $\overline{WE}$ Controlled Write)



### WRITE CYCLE 2 ( $\overline{CE}$ Controlled Write)



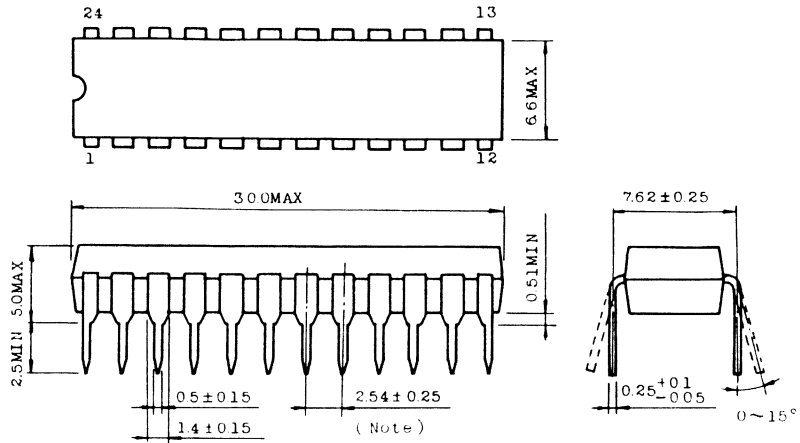
- Note: 1.  $\overline{WE}$  is High for Read cycle.  
 2. Assuming that  $\overline{CE}$  Low transition occurs coincident with or after  $\overline{WE}$  Low transition, Outputs remain in a high impedance state.  
 3. Assuming that  $\overline{CE}$  High transition occurs coincident with or prior to  $\overline{WE}$  High transition, Outputs remain in a high impedance state.  
 4. The Operating temperature ( $T_a$ ) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

# TC55417P-35

# TC55417P-45

## OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54mm.

All leads are located within 0.25mm of the true longitudinal position with respect to No.1 and No.24 leads.





**Erasable/Programmable Read Only Memories**



## HIGH SPEED PROGRAMMING MODE

### FEATURES

The High Speed Programming I or High Speed Programming II Algorithms may be used to program 64K through 512K devices. The 1MEGABIT devices may be programmed using the High Speed Programming II Algorithm.

The High Speed Programming I Algorithm uses 1ms programming pulse and the flow chart is shown in Figure 1.

The High Speed Programming II Algorithm uses 0.1ms programming pulse and the flow chart is shown in Figure 2.

### APPLICABLE DEVICES

Device Name		Theoretical Programming Time	
EPROM	One Time PROM	I	II
TMM2764AD/ADI	TMM2464AP/AF	33 sec	0.8 sec
TMM27128AD/ADI	TMM24128AP/AF	66 sec	1.7 sec
TMM27256AD/ADI	TMM24256AP/AF	131 sec	3.3 sec
TC57256AD	TC54256AP/AF	131 sec	3.3 sec
TMM27512D/DI	TMM24512P	262 sec	7.0 sec
TC571000D	TC541000P	N/A	14 sec
TC571001D	TC541001P	N/A	14 sec

### IDENTIFICATION MODE

The identification mode allows the reading of an electrical signature from the device that will identify the manufacturer and device type. The identification mode is activated using the following conditions:

- For the Manufacturer Code:  
Set  $A_9=12V\pm 0.5V$ ,  $A_\phi=ViL$ , Other Addresses= $ViL$   
Note: The manufacturer code is consistent with the E.I.A. standard.
- For the Device Code:  
Set  $A_9=12V\pm 0.5V$ ,  $A_\phi=ViH$ , Other Addresses= $ViL$ .  
Note: The Device Code is manufacturer dependent.

The following table shows the Electrical Signatures of Toshiba devices.

### ELECTRICAL DEVICES

Device Name		Signature	
EPROM	One Time PROM	Manufacture Code	Device Code
TMM2764AD/ADI	TMM2464AP/AF	98	52
TMM27128AD/ADI	TMM24128AP/AF	98	D3
TMM27256AD/ADI	TMM24256AP/AF	98	54
TC57256AD	TC54256AP/AF	98	C4
TMM27512D/DI	TMM24512P	98	15
TC571000D	TC541000P	98	86
TC571001D	TC541001P	98	07

# TOSHIBA

Figure 1

## HIGH SPEED PROGRAM I FLOW CHART

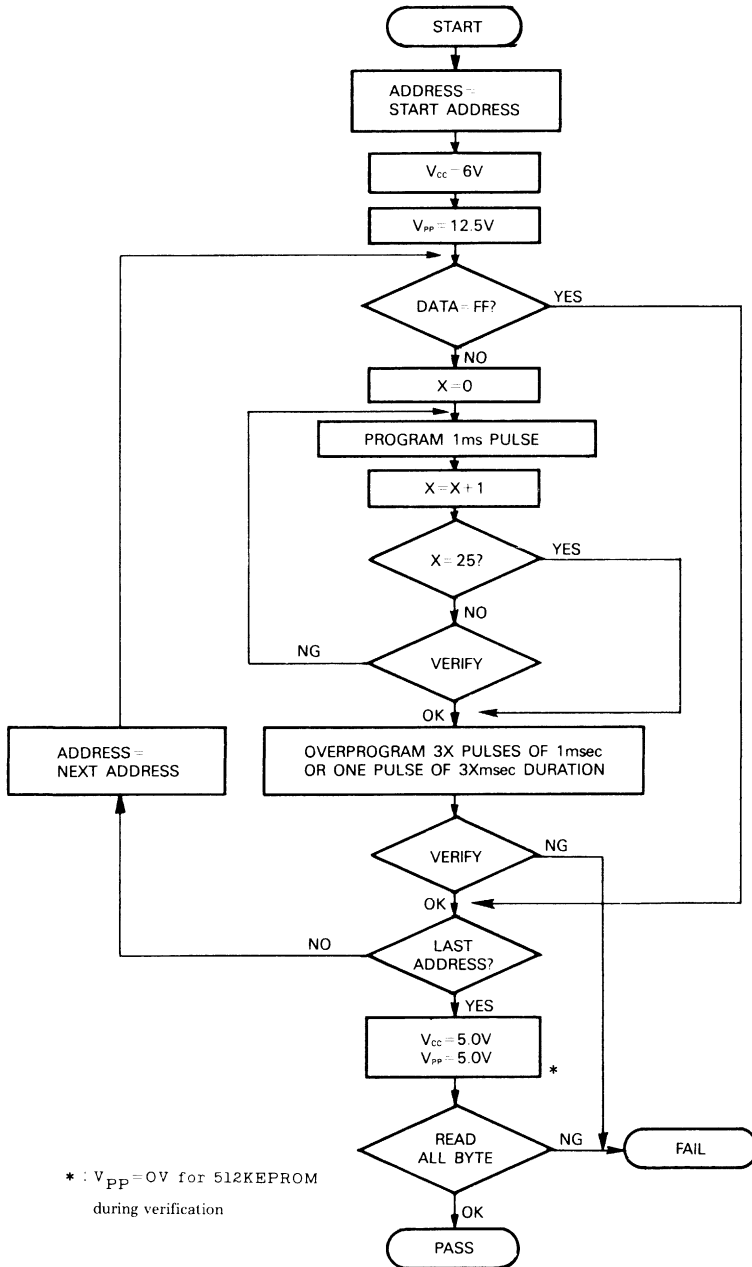
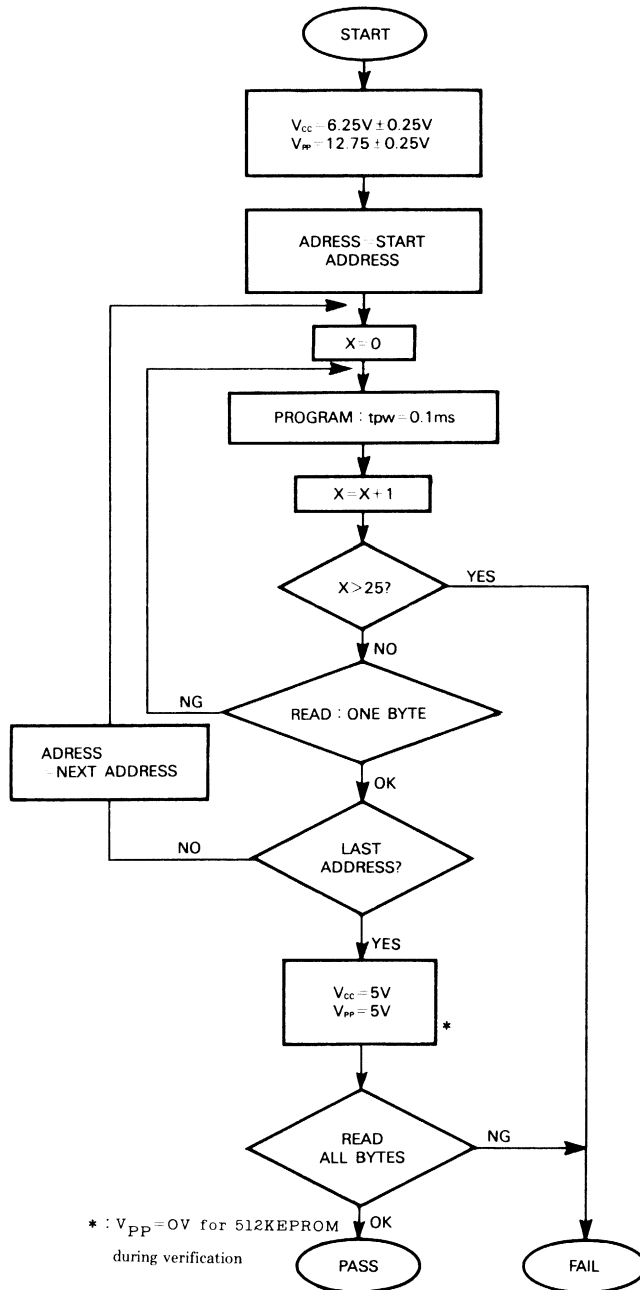


Figure 2

## HIGH SPEED PROGRAM II FLOW CHART





# TOSHIBA MOS MEMORY PRODUCT

8,192 WORD × 8 BIT UV ERASABLE AND  
ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

**TMM2764AD-15, TMM2764AD-150**  
**TMM2764AD-20, TMM2764AD-200**

## DESCRIPTION

The TMM2764AD is a 8192 word × 8 bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM2764AD's access time is 150ns/200ns, and the TMM2764AD operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time.

The standby mode is achieved by applying a TTL-high level signal to the  $\overline{CE}$  input.

For program operation, the programming is achieved by using the high speed programming mode.

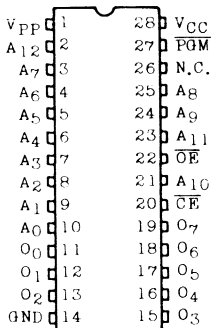
The TMM2764AD is fabricated with the N-channel silicon double layer gate MOS technology.

## FEATURES

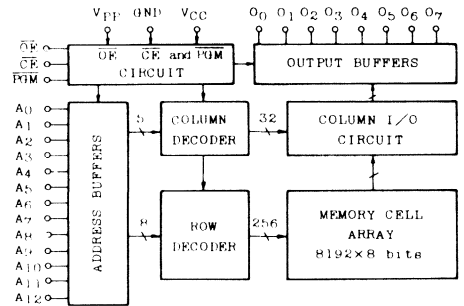
	-15	-20	-150	-200
$V_{CC}$	$5V \pm 5\%$		$5V \pm 10\%$	
$t_{ACC}$	150ns	200ns	150ns	200ns
$I_{CC2}$	100mA		120mA	
$I_{CC1}$	30mA		35mA	

- Fully static operation
- High speed programming mode
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i2764 A

## PIN CONNECTION (TOP VIEW)



## BLOCK DIAGRAM



## PIN NAMES

$A_0 \sim A_{14}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
PGM	Program Control Input
N. C.	No Connection
$V_{PP}$	Program Supply Voltage
$V_{CC}$	$V_{CC}$ Supply Voltage (+5V)
GND	Ground

## MODE SELECTION

MODE	PIN	PGM (27)	CE (20)	OE (22)	$V_{PP}$ (1)	$V_{CC}$ (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER	
Read		H	L	L	5V	5V	Data Out	Active	
Output Deselect		*	*	H			High Impedance		
Standby		*	H	*			High Impedance		Standby
Program		L	L	*			Data In		
Program		*	H	*	12.5V	6V	High Impedance	Active	
Inhibit		H	L	H			High Impedance		
Program Verify		H	L	L			Data Out		

Note \* : H or L

# TMM2764AD-15, TMM2764AD-150 TMM2764AD-20, TMM2764AD-200

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	-0.6 ~ 7.0	V
V <sub>PP</sub>	Program Supply Voltage	-0.6 ~ 14.0	V
V <sub>IN</sub>	Input Voltage	-0.6 ~ 7.0	V
V <sub>OUT</sub>	Output Voltage	-0.6 ~ 7.0	V
P <sub>D</sub>	Power Dissipation	1.5	W
T <sub>SOLDER</sub>	Soldering Temperature · Time	260 · 10	°C·sec
T <sub>STRG</sub>	Storage Temperature	-65 ~ 125	°C
T <sub>OPR</sub>	Operating Temperature	0 ~ 70	°C

## READ OPERATION

### D. C. AND A. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM2764AD-15/20	TMM2764AD-150/200
T <sub>a</sub>	Operating Temperature	0 ~ 70°C	0 ~ 70°C
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	5V ± 5%	5V ± 10%
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	2.0 ~ V <sub>CC</sub> ± 0.6V	2.0 ~ V <sub>CC</sub> + 0.6V

### D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT	
I <sub>LI</sub>	Input Current	V <sub>IN</sub> = 0 ~ V <sub>CC</sub>	—	—	± 10	μA	
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0.4 ~ V <sub>CC</sub>	—	—	± 10	μA	
I <sub>CC1</sub>	Supply Current (Standby)	$\overline{CE} = V_{IH}$	-15/20	—	—	30	mA
			-150/200	—	—	35	
I <sub>CC2</sub>	Supply Current (Active)	$\overline{CE} = V_{IL}$	-15/20	—	—	100	mA
			-150/200	—	—	120	
V <sub>IH</sub>	Input High Voltage	—	2.0	—	V <sub>CC</sub> + 1.0	V	
V <sub>IL</sub>	Input Low Voltage	—	-0.3	—	0.8	V	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400μA	2.4	—	—	V	
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA	—	—	0.4	V	
I <sub>PP1</sub>	V <sub>PP</sub> Current	V <sub>PP</sub> = 0 ~ V <sub>CC</sub> + 0.6	—	—	± 10	μA	



# TMM2764AD-15, TMM2764AD-150 TMM2764AD-20, TMM2764AD-200

## A. C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM2764AD-15/150		TMM2764AD-20/200		UNIT
		MIN.	MAX.	MIN.	MAX.	
$t_{ACC}$	Address Access Time	—	150	—	200	ns
$t_{CE}$	$\overline{CE}$ to Output Valid	—	150	—	200	ns
$t_{OE}$	$\overline{OE}$ to Output Valid	—	70	—	70	ns
$t_{PGM}$	PGM to Output Valid	—	70	—	70	ns
$t_{DF1}$	$\overline{CE}$ to Output in High-Z	0	60	0	60	ns
$t_{DF2}$	$\overline{OE}$ to Output in High-Z	0	60	0	60	ns
$t_{DF3}$	PGM to Output in High-Z	0	60	0	60	ns
$t_{OH}$	Output Data Hold Time	0	—	0	—	ns

## A. C. TEST CONDITIONS

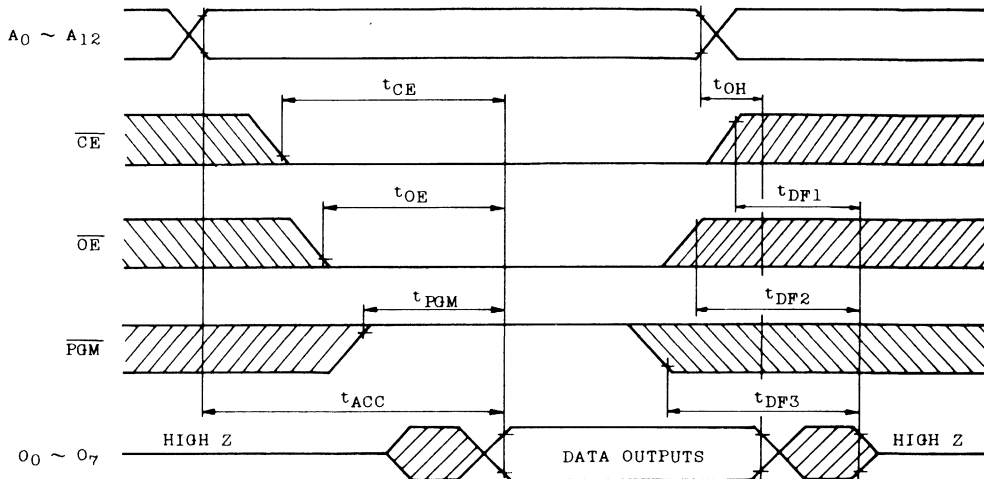
- Output Load : 1 TTL Gate and  $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

## CAPACITANCE \* ( $T_a = 25^\circ\text{C}$ , $f = 1\text{MHz}$ )

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$C_{IN}$	Input Capacitance	$V_{IN} = 0\text{V}$	—	4	6	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0\text{V}$	—	8	12	pF

\* This parameter is periodically sampled and is not 100% tested.

## TIMING WAVEFORMS (READ)



# TMM2764AD-15, TMM2764AD-150 TMM2764AD-20, TMM2764AD-200

## HIGH SPEED PROGRAM OPERATION

### D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.0	—	V <sub>CC</sub> + 1.0	V
V <sub>IL</sub>	Input Low Voltage	-0.3	—	0.8	V
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	5.75	6.0	6.25	V
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	12.0	12.5	13.0	V

### D. C. and OPERATING CHARACTERISTICS (T<sub>a</sub> = 25 ± 5 °C, V<sub>CC</sub> = 6V ± 0.25V, V<sub>PP</sub> = 12.5V ± 0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>LI</sub>	Input Current	V <sub>IN</sub> = 0 ~ V <sub>CC</sub>	—	—	± 10	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400 μA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA	—	—	0.4	V
I <sub>CC</sub>	V <sub>CC</sub> Supply Current	—	—	—	120	mA
I <sub>PP2</sub>	V <sub>PP</sub> Supply Current	V <sub>PP</sub> = 13.0V	—	—	50	mA
V <sub>ID</sub>	A9 Auto Select Voltage	—	11.5	12.0	12.5	V

### A. C. PROGRAMMING CHARACTERISTICS (T<sub>a</sub> = 25 ± 5 °C, V<sub>CC</sub> = 6V ± 0.25V, V<sub>PP</sub> = 12.5V ± 0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t <sub>AS</sub>	Address Setup Time	—	2	—	—	μs
t <sub>AH</sub>	Address Hold Time	—	2	—	—	μs
t <sub>CEs</sub>	CE Setup Time	—	2	—	—	μs
t <sub>CEH</sub>	CE Hold Time	—	2	—	—	μs
t <sub>DS</sub>	Data Setup Time	—	2	—	—	μs
t <sub>DH</sub>	Data Hold Time	—	2	—	—	μs
t <sub>VS</sub>	V <sub>PP</sub> Setup Time	—	2	—	—	μs
t <sub>PW</sub>	Program Pulse Width	—	0.95	1.0	1.05	ms
t <sub>OPW</sub>	Additional Program Pulse Width	Note 1	2.85	—	78.75	ms
t <sub>PRT</sub>	Program Pulse Rise Time	—	5	—	—	ns
t <sub>PF1</sub>	Program Pulse Fall Time	—	5	—	—	ns
t <sub>OF</sub>	OE to Output Valid	—	—	—	100	ns
t <sub>DF2</sub>	OE to Output in High Z	CE = V <sub>IL</sub>	—	—	90	ns

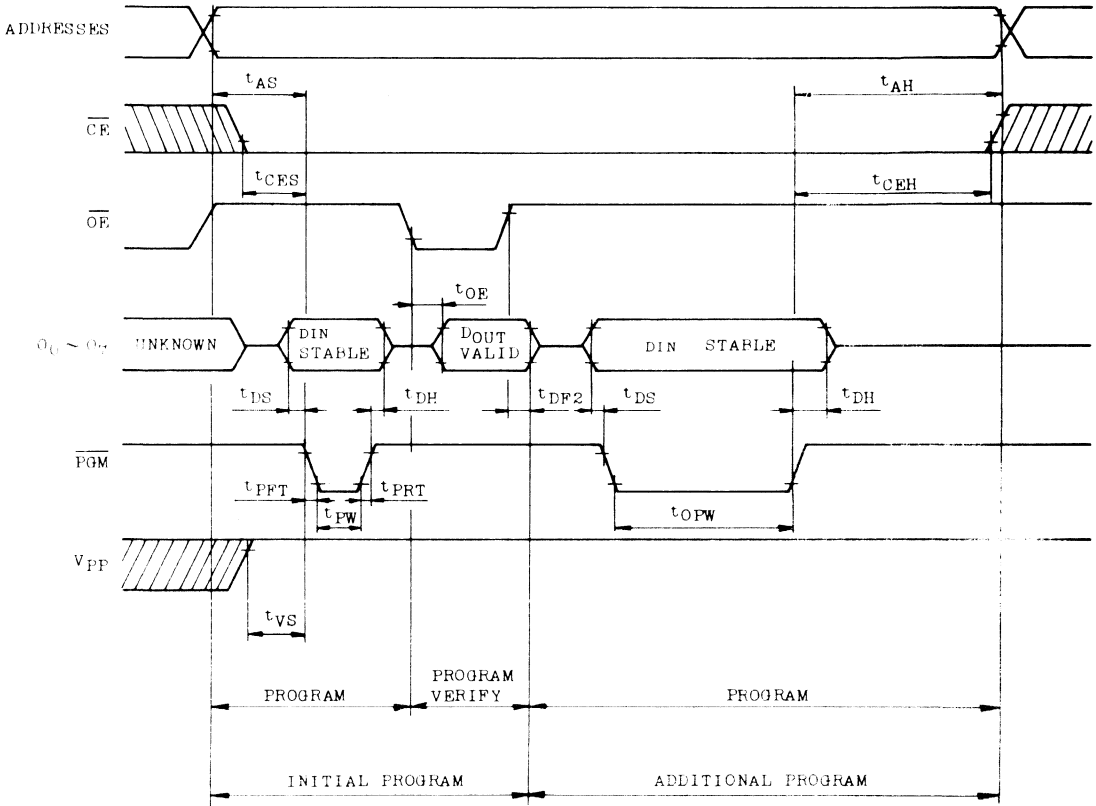
#### A. C. Test Conditions

- Output Load : 1 TTL Gate and C<sub>L</sub>(100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45 to 2.4V
- Timing Measurement Reference Level : Input 1V and 2V ; Output 0.8V and 2.0V

Note : 1. t<sub>OPW</sub> depends on the program pulse width which is required in the initial Program.

**TMM2764AD-15, TMM2764AD-150  
TMM2764AD-20, TMM2764AD-200**

**TIMING WAVEFORMS (PROGRAM)**



- Note :
1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and cut off simultaneously or after  $V_{PP}$ .
  2. Removing the device from socket and setting the device in socket with  $V_{PP} = 12.5V$  may cause permanent damage to the device.
  3. The  $V_{PP}$  supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the  $V_{PP}$  terminal.

When the switching pulse voltage is applied to the  $V_{PP}$  terminal, the overshoot voltage of its pulse should not be exceeded 14V.

# TMM2764AD-15, TMM2764AD-150 TMM2764AD-20, TMM2764AD-200

## ERASURE CHARACTERISTICS

The TMM2764AD's erasure is achieved by applying shortwave ultraviolet light which has a wave length of 2537Å (Angstroms) to the chip through the transparent window.

The integrated dose (Ultraviolet light intensity [w/cm<sup>2</sup>] × exposure time [sec.]) for erasure should be a minimum of 15 [W sec/cm<sup>2</sup>]

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is 12000 [μw/cm<sup>2</sup>] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm<sup>2</sup>] × (20×60) [sec] ≅ 15 [w·sec/cm<sup>2</sup>].)

The TMM2764AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available

## OPERATION INFORMATION

The TMM2764AD's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL

		PGM (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V <sub>PP</sub> (1)	V <sub>CC</sub> (28)	O <sub>0</sub> ~O <sub>7</sub> (11~13, 15~19)	POWER
READ OPERATION (T <sub>a</sub> =0~70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (T <sub>a</sub> =25±5°C)	Program	L	L	*	12.5V	6V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	Active
		H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note H : V<sub>IH</sub>, L : V<sub>IL</sub>, \* : V<sub>IH</sub> or V<sub>IL</sub>

## READ MODE

The TMM2764AD has three control functions. The chip enable ( $\overline{CE}$ ) controls the operation power and should be used for device selection.

The output enable ( $\overline{OE}$ ) and the program control ( $\overline{PGM}$ ) control the output buffers, independent of device selection.

Assuming that  $\overline{CE} = \overline{OE} = V_{IL}$  and  $\overline{PGM} = V_{IH}$ , the output data is valid at the outputs after address access time from stabilizing of all addresses.

The  $\overline{CE}$  to output valid (t<sub>CE</sub>) is equal to the address access time (t<sub>ACC</sub>).

Assuming that  $\overline{CE} = V_{IL}$ ,  $\overline{PGM} = V_{IH}$  and all addresses are valid, the output data is valid at the outputs after t<sub>OE</sub> from the falling edge of  $\overline{OE}$ .

And assuming that  $\overline{CE} = \overline{OE} = V_{IL}$  and all addresses are valid, the output data is valid at the outputs after t<sub>PGM</sub> from the rising edge of  $\overline{PGM}$ .

## OUTPUT Deselect MODE

Assuming that  $\overline{CE} = V_{IH}$  or  $\overline{OE} = V_{IH}$ , the outputs will be in a high impedance state.

So two or more TMM2764AD can be connected

together on a common bus line.

When  $\overline{CE}$  is decoded for device selection, all deselected devices are in low power standby mode.

# TMM2764AD-15, TMM2764AD-150 TMM2764AD-20, TMM2764AD-200

## STANDBY MODE

The TMM2764AD has a low power standby mode controlled by the  $\overline{CE}$  signal.

By applying a TTL high level to the  $\overline{CE}$  input, the TMM2764AD is placed in the standby mode which

## PROGRAM MODE

Initially, when received by customers, all bits of the TMM2764AD are in the "1" state which is erased state.

Therefore the program operation is to introduce "0s" data into the desired bit locations by electrically

## PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

## PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to  $V_{PP}$  terminal, a high level  $\overline{CE}$  or  $\overline{PGM}$  input inhibits the TMM2764AD from being programmed.

Programming of two or more TMM2764AD's in parallel with different data is easily accomplished.

## HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode.

The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the  $V_{PP}$  terminal with  $V_{CC}=6V$  and  $\overline{PGM}=V_{IH}$ .

The programming is achieved by applying a single TTL low level 1ms pulse the  $\overline{PGM}$  input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another

reduce 70% of the operating current and then the outputs are in a high impedance state, independent of the  $\overline{OE}$  and the  $\overline{PGM}$  inputs.

programming.

The levels required for all inputs are TTL.

The TMM2764AD can be programmed any location at anytime—either individually, sequentially, or at random.

The verify is accomplished with  $\overline{OE}$  and  $\overline{CE}$  at  $V_{IL}$  and  $\overline{PGM}$  at  $V_{IH}$ .

That is, all inputs except for  $\overline{CE}$  or  $\overline{PGM}$  may be commonly connected, and a TTL low level program pulse is applied to the  $\overline{CE}$  and  $\overline{PGM}$  of the desired device only and TTL high level signal is applied to the other devices.

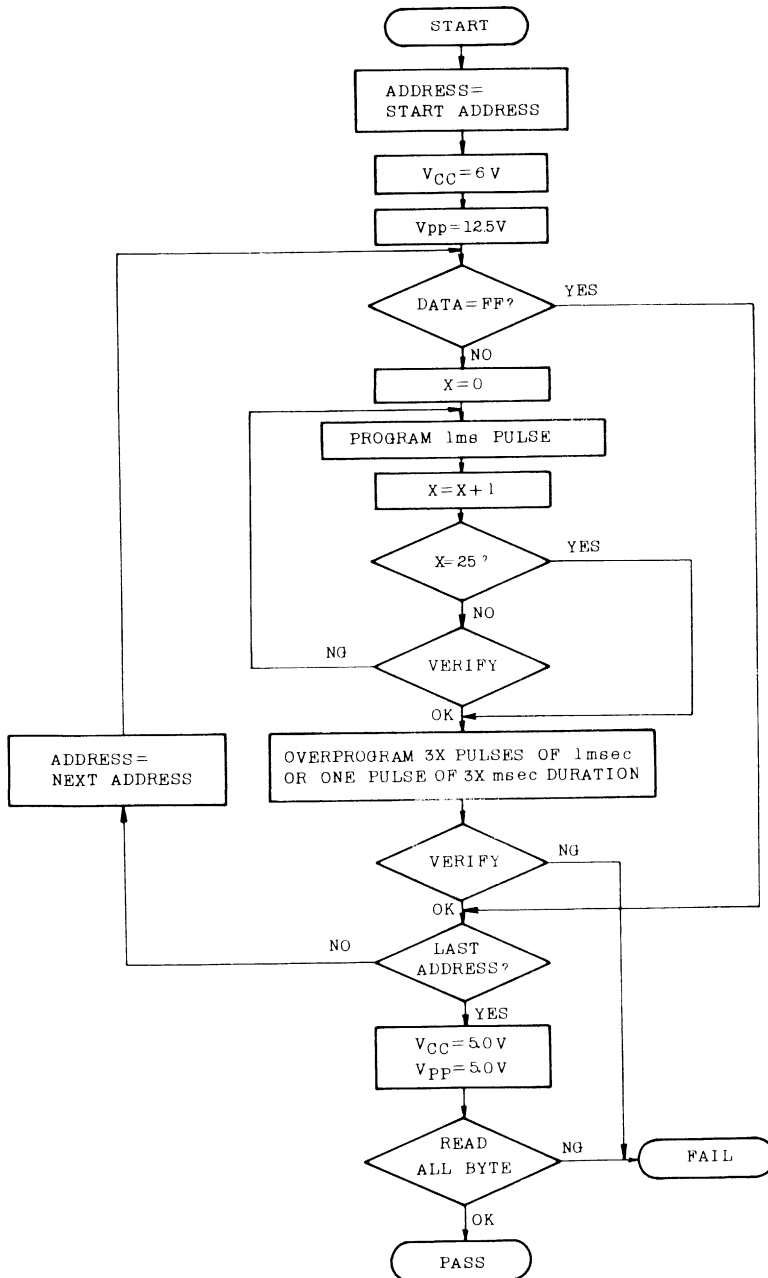
program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max.25 times)

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with  $V_{CC}=V_{PP}=5V$ .

**TMM2764AD-15, TMM2764AD-150  
TMM2764AD-20, TMM2764AD-200**

**HIGH SPEED PROGRAM MODE FLOW CHART**



# TMM2764AD-15, TMM2764AD-150 TMM2764AD-20, TMM2764AD-200

## ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM2764AD which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from TMM2764AD by using this mode before program operation and automatically set program voltage ( $V_{PP}$ ) and algorithm.

Electric signature mode is set up when 12V is

applied to address line A9 and the rest of address lines is set to  $V_{IL}$  in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to  $V_{IH}$ . These two codes possess an odd parity with the parity bit of MSB (O7).

The following table shows electric signature of TMM2764AD.

SIGNATURE \ PINS	A <sub>9</sub> (10)	O <sub>7</sub> (19)	O <sub>6</sub> (18)	O <sub>5</sub> (17)	O <sub>4</sub> (16)	O <sub>3</sub> (15)	O <sub>2</sub> (13)	O <sub>1</sub> (12)	O <sub>0</sub> (11)	HEX. DATA
Manufacture Code	$V_{IH}$	1	0	0	1	1	0	0	0	98
Device Code	$V_{IH}$	0	1	0	1	0	0	1	0	52

Notes : A9 = 12V ± 0.5V

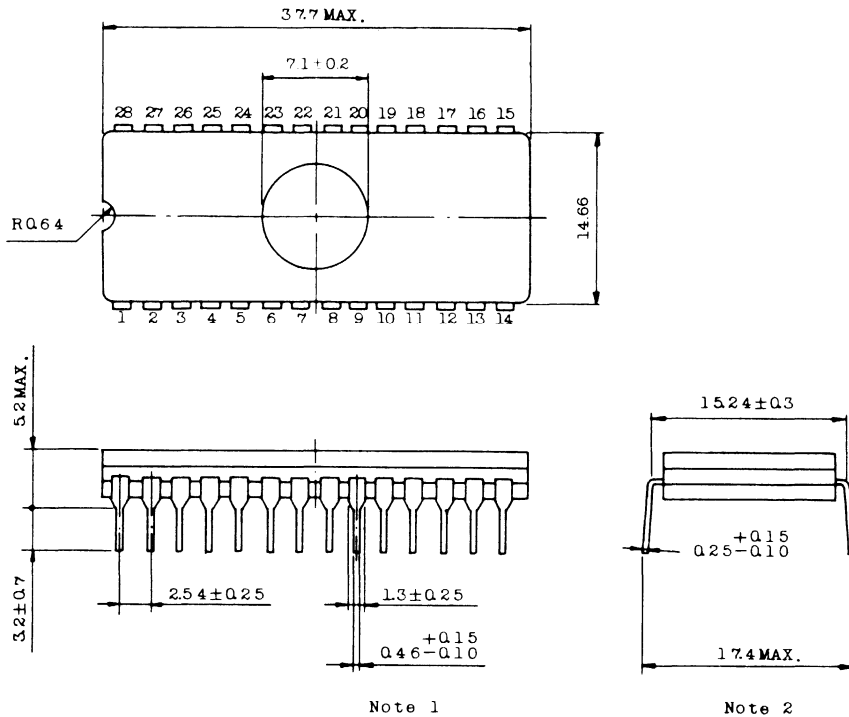
A1 ~ A8, A10 ~ A12,  $\overline{CE}$ ,  $\overline{OE}$  =  $V_{IL}$

PGM =  $V_{IH}$

# TMM2764AD-15, TMM2764AD-150 TMM2764AD-20, TMM2764AD-200

## OUTLINE DRAWINGS

Unit in mm



- Note: 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.  
2. This value is measured at the end of leads.  
3. All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.  
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# TOSHIBA MOS MEMORY PRODUCT

8,192 WORD × 8 BIT UV ERASABLE AND  
ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

## TMM2764ADI-15 TMM2764ADI-20

### DESCRIPTION

The TMM2764ADI is a 8192 word × 8bit ultra-violet light erasable and electrically programmable read only memory. For read operation, the TMM2764AD's access time is 150/200ns and the TMM2764ADI operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time.

The standby mode is achieved by applying a TTL-high level signal to the  $\overline{CE}$  input.

For program operation, the programming is achieved by using the high speed programming mode.

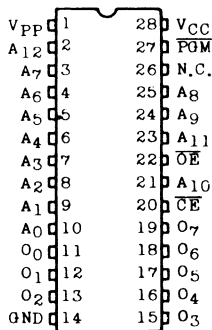
The TMM2764ADI is fabricated with the Nchannel silicon double layer gate MOS technology.

### FEATURES

	- 15	- 20
V <sub>CC</sub>	5V ± 5%	
t <sub>ACC</sub>	150ns	200ns
I <sub>CC2</sub>	100mA	
I <sub>CC1</sub>	30mA	

- Wide operating temperature range -40~85°C
- Fully static operation
- High speed programming mode
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i2764 A

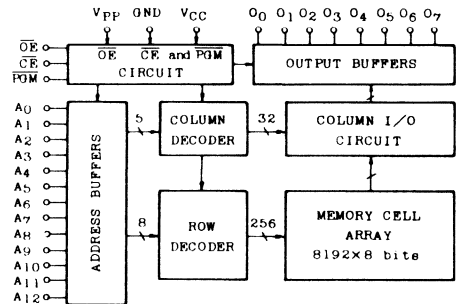
### PIN CONNECTION (TOP VIEW)



### PIN NAMES

A <sub>0</sub> ~A <sub>14</sub>	Address Inputs
O <sub>0</sub> ~O <sub>7</sub>	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
PGM	Program Control Input
N. C.	No Connection
V <sub>PP</sub>	Program Supply Voltage
V <sub>CC</sub>	V <sub>CC</sub> Supply Voltage (+5V)
GND	Ground

### BLOCK DIAGRAM



### MODE SELECTION

MODE	PIN	PGM (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V <sub>PP</sub> (1)	V <sub>CC</sub> (28)	O <sub>0</sub> ~O <sub>7</sub> (11~13, 15~19)	POWER
Read		H	L	L	5V	5V	Data Out	Active
Output Deselect		*	*	H			High Impedance	
Standby		*	H	*	12.5V	6V	High Impedance	Standby
Program		L	L	*			Data In	
Program Inhibit		*	H	*			High Impedance	
Program Verify		H	L	L	12.5V	6V	High Impedance	Active
		H	L	L			Data Out	

Note \* : H or L

# TMM2764ADI-15

# TMM2764ADI-20

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
$V_{CC}$	$V_{CC}$ Power Supply Voltage	-0.6 ~ 7.0	V
$V_{PP}$	Program Supply Voltage	-0.6 ~ 14.0	V
$V_{IN}$	Input Voltage	-0.6 ~ 7.0	V
$V_{OUT}$	Output Voltage	-0.6 ~ 7.0	V
$P_D$	Power Dissipation	1.5	W
$T_{SOLDER}$	Soldering Temperature · Time	260 · 10	°C·sec
$T_{STRG}$	Storage Temperature	-65 ~ 125	°C
$T_{OPR}$	Operating Temperature	-40 ~ 85	°C

## READ OPERATION

### D. C. AND A. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM2764ADI-15/20
$T_a$	Operating Temperature	-40 ~ 85 C
$V_{CC}$	$V_{CC}$ Power Supply Voltage	5V ± 5%
$V_{PP}$	$V_{PP}$ Power Supply Voltage	2.2 ~ $V_{CC} \pm 0.6V$

### D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
$I_{LI}$	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	+10	$\mu A$
$I_{LO}$	Output Leakage Current	$V_{OUT} = 0.4 \sim V_{CC}$	—	—	+10	$\mu A$
$I_{CC1}$	Supply Current (Standby)	$\overline{CE} = V_{IH}$	—	—	35	mA
$I_{CC2}$	Supply Current (Active)	$\overline{CE} = V_{IL}$	—	—	120	mA
$V_{IH}$	Input High Voltage	—	2.2	—	$V_{CC} + 1.0$	V
$V_{IL}$	Input Low Voltage	—	-0.3	—	0.8	V
$V_{OH}$	Output High Voltage	$I_{OH} = -400\mu A$	2.4	—	—	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2.1mA$	—	—	0.4	V
$I_{PP1}$	$V_{PP}$ Current	$V_{PP} = 0 \sim V_{CC} + 0.6$	—	—	±10	$\mu A$

# TMM2764ADI-15

# TMM2764ADI-20

## A. C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM2764ADI-15		TMM2764ADI-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
$t_{ACC}$	Address Access Time	—	150	—	200	ns
$t_{CE}$	$\overline{CE}$ to Output Valid	—	150	—	200	ns
$t_{OE}$	$\overline{OE}$ to Output Valid	—	70	—	70	ns
$t_{PGM}$	$\overline{PGM}$ to Output Valid	—	70	—	70	ns
$t_{DF1}$	$\overline{CE}$ to Output in High-Z	0	60	0	60	ns
$t_{DF2}$	$\overline{OE}$ to Output in High-Z	0	60	0	60	ns
$t_{DF3}$	$\overline{PGM}$ to Output in High-Z	0	60	0	60	ns
$t_{OH}$	Output Data Hold Time	0	—	0	—	ns

## A. C. TEST CONDITIONS

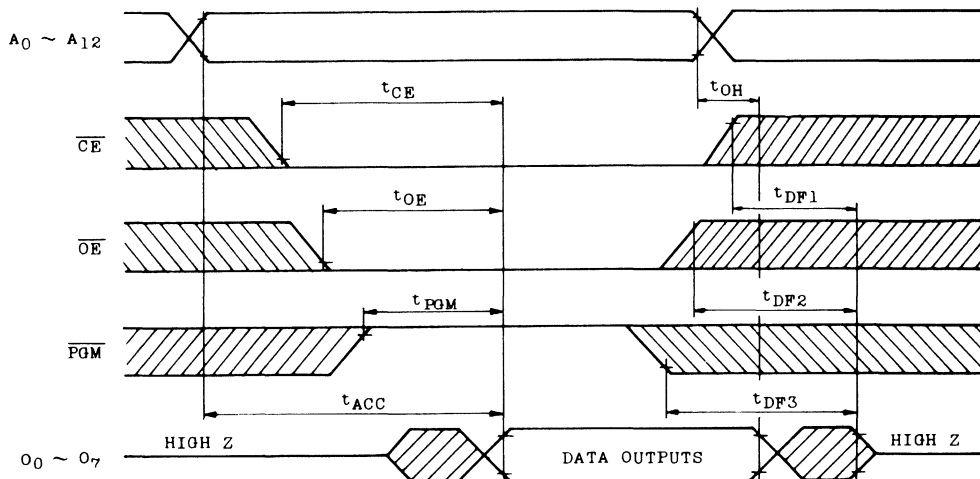
- Output Load : 1 TTL Gate and  $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V. Outputs 0.8V and 2.0V

## CAPACITANCE \* ( $T_a = 25^\circ\text{C}$ , $f = 1\text{MHz}$ )

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$C_{IN}$	Input Capacitance	$V_{IN} = 0\text{V}$	—	4	6	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0\text{V}$	—	8	12	pF

\* This parameter is periodically sampled and is not 100% tested.

## TIMING WAVEFORMS (READ)



# TMM2764ADI-15

# TMM2764ADI-20

## HIGH SPEED PROGRAM OPERATION

### D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>CC</sub> + 1.0	V
V <sub>IL</sub>	Input Low Voltage	-0.3	—	0.8	V
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	5.75	6.0	6.25	V
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	12.0	12.5	13.0	V

### D. C. and OPERATING CHARACTERISTICS (T<sub>a</sub> = 25 ± 5°C, V<sub>CC</sub> = 6V ± 0.25V, V<sub>PP</sub> = 12.5V ± 0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>I1</sub>	Input Current	V <sub>IN</sub> = 0 ~ V <sub>CC</sub>	—	—	± 10	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400μA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA	—	—	0.4	V
I <sub>CC</sub>	V <sub>CC</sub> Supply Current	—	—	—	120	mA
I <sub>PP2</sub>	V <sub>PP</sub> Supply Current	V <sub>PP</sub> = 13.0V	—	—	50	mA
V <sub>ID</sub>	A9 Auto Select Voltage	—	11.5	12.0	12.5	V

### A. C. PROGRAMMING CHARACTERISTICS (T<sub>a</sub> = 25 ± 5°C, V<sub>CC</sub> = 6V ± 0.25V, V<sub>PP</sub> = 12.5V ± 0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t <sub>AS</sub>	Address Setup Time	—	2	—	—	μs
t <sub>AH</sub>	Address Hold Time	—	2	—	—	μs
t <sub>CES</sub>	$\overline{CE}$ Setup Time	—	2	—	—	μs
t <sub>CEH</sub>	$\overline{CE}$ Hold Time	—	2	—	—	μs
t <sub>DS</sub>	Data Setup Time	—	2	—	—	μs
t <sub>DH</sub>	Data Hold Time	—	?	—	—	μs
t <sub>VS</sub>	V <sub>PP</sub> Setup Time	—	2	—	—	μs
t <sub>PW</sub>	Program Pulse Width	—	0.95	1.0	1.05	ms
t <sub>OPW</sub>	Additional Program Pulse Width	Note 1	2.85	—	78.75	ms
t <sub>PRT</sub>	Program Pulse Rise Time	—	5	—	—	ns
t <sub>PFT</sub>	Program Pulse Fall Time	—	5	—	—	ns
t <sub>OE</sub>	$\overline{OE}$ to Output Valid	—	—	—	100	ns
t <sub>DF2</sub>	$\overline{OE}$ to Output in High Z	$\overline{CE} = V_{IL}$	—	—	90	ns

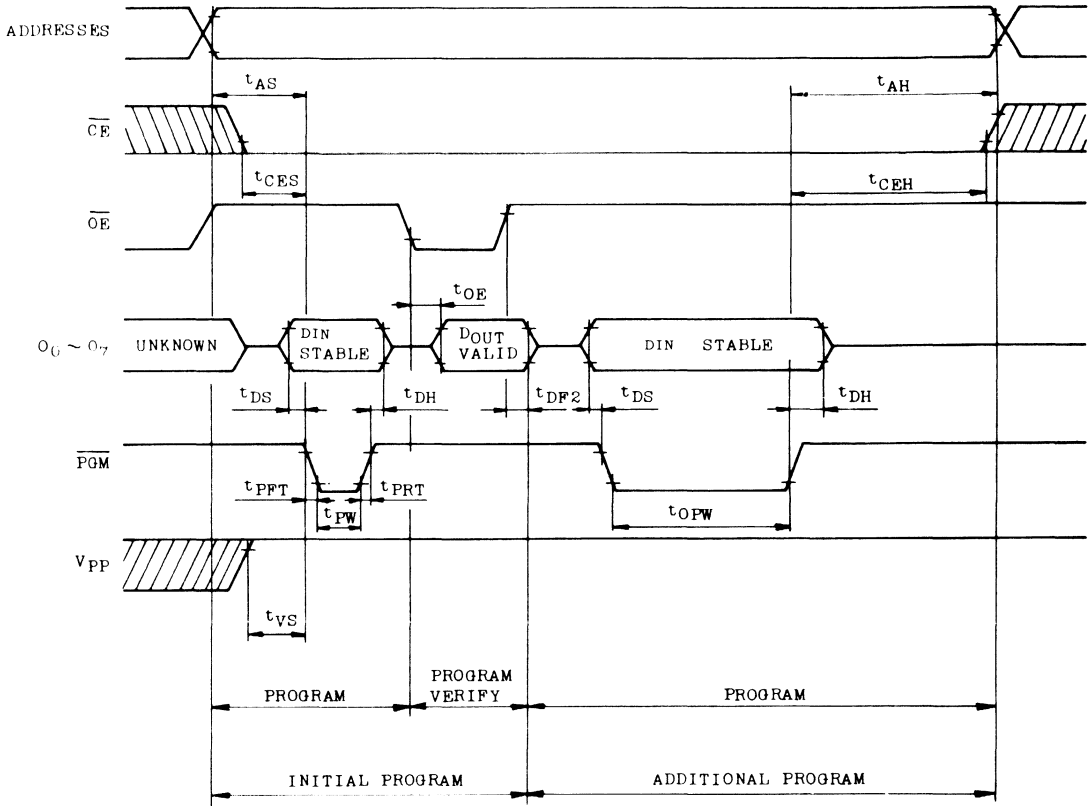
#### A. C. Test Conditions

- Output Load : 1 TTL Gate and C<sub>L</sub>(100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 1V and 2V ; Output 0.8V and 2.0V

Note : 1. t<sub>OPW</sub> depends on the program pulse width which is required in the initial Program

# TMM2764ADI-15 TMM2764ADI-20

## TIMING WAVEFORMS (PROGRAM)



- Note :
1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and cut off simultaneously or after  $V_{PP}$ .
  2. Removing the device from socket and setting the device in socket with  $V_{PP}=12.5V$  may cause permanent damage to the device.
  3. The  $V_{PP}$  supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the  $V_{PP}$  terminal.

When the switching pulse voltage is applied to the  $V_{PP}$  terminal, the overshoot voltage of its pulse should not be exceeded 14V

# TMM2764ADI-15

# TMM2764ADI-20

## ERASURE CHARACTERISTICS

The TMM2764ADI's erasure is achieved by applying shortwave ultraviolet light which has a wave length of 2537Å (Angstroms) to the chip through the transparent window.

The integrated dose (Ultraviolet light intensity [w/cm<sup>2</sup>] × exposure time [sec.]) for erasure should be a minimum of 15 [W sec/cm<sup>2</sup>]

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is 12000 [μw/cm<sup>2</sup>] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [μw/cm<sup>2</sup>] × (20×60) [sec] ≅ 15 [w · sec/cm<sup>2</sup>].)

The TMM2764ADI's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the flourescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available

## OPERATION INFORMATION

The TMM 2764ADI's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

MODE		PIN NAMES (NUMBER)	PGM (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V <sub>PP</sub> (1)	V <sub>CC</sub> (28)	O <sub>0</sub> ~O <sub>7</sub> (11~13, 15~19)	POWER
READ OPERATION (Ta = -40~85°C)	Read		H	L	L	5V	5V	Data Out	Active
	Output Deselect		*	*	H			High Impedance	Active
	Standby		*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta = 25 ± 5°C)	Program		L	L	*	12.5V	6V	Data In	Active
	Program Inhibit		*	H	*			High Impedance	Active
			H	L	H			High Impedance	Active
	Program Verify		H	L	L			Data Out	Active

Note: H : V<sub>IH</sub>, L : V<sub>IL</sub>, \* : V<sub>IH</sub> or V<sub>IL</sub>

## READ MODE

The TMM2764ADI has three control functions. The chip enable ( $\overline{CE}$ ) controls the operation power and should be used for device selection.

The output enable ( $\overline{OE}$ ) and the program control ( $\overline{PGM}$ ) control the output buffers, independent of device selection.

Assuming that  $\overline{CE} = \overline{OE} = V_{IL}$  and  $\overline{PGM} = V_{IH}$ , the output data is valid at the outputs after address access time from stabilizing of all addresses.

The  $\overline{CE}$  to output valid (t<sub>CE</sub>) is equal to the address access time (t<sub>ACC</sub>).

Assuming that  $\overline{CE} = V_{IL}$ ,  $\overline{PGM} = V_{IH}$  and all addresses are valid, the output data is valid at the outputs after t<sub>OE</sub> from the falling edge of  $\overline{OE}$ .

And assuming that  $\overline{CE} = \overline{OE} = V_{IL}$  and all addresses are valid, the output data is valid at the outputs after t<sub>PGM</sub> from the rising edge of  $\overline{PGM}$ .

## OUTPUT DESELECT MODE

Assuming that  $\overline{CE} = V_{IH}$  or  $\overline{OE} = V_{IH}$ , the outputs will be in a high impedance state.

So two or more TMM2764ADI can be connected

together on a common bus line.

When  $\overline{CE}$  is decoded for device selection, all deselected devices are in low power standby mode.

# TMM2764ADI-15

# TMM2764ADI-20

## STANDBY MODE

The TMM2764ADI has a low power standby mode controlled by the  $\overline{CE}$  signal.

By applying a TTL high level to the  $\overline{CE}$  input, the TMM2764ADI is placed in the standby mode which

## PROGRAM MODE

Initially, when received by customers, all bits of the TMM2764ADI are in the "1" state which is erased state. The programming operation introduces "0s" data into the desired bit locations by electrically programming.

## PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

## PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to  $V_{PP}$  terminal, a high level  $\overline{CE}$  or  $\overline{PGM}$  input inhibits the TMM2764ADI from being programmed.

Programming of two or more TMM2764ADI's in parallel with different data is easily accomplished

## HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode.

The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the  $V_{PP}$  terminal with  $V_{CC}=6V$  and  $\overline{PGM}=V_{IH}$ .

The programming is achieved by applying a single TTL low level 1ms pulse the  $\overline{PGM}$  input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another

reduce 70% of the operating current and then the outputs are in a high impedance state, independent of the  $\overline{OE}$  and the  $\overline{PGM}$  inputs.

The levels required for all inputs are TTL.

The TMM2764ADI can be programmed any location at anytime — either individually, sequentially or at random.

The verify is accomplished with  $\overline{OE}$  and  $\overline{CE}$  at  $V_{IL}$  and  $\overline{PGM}$  at  $V_{IH}$ .

That is, all inputs except for  $\overline{CE}$  or  $\overline{PGM}$  may be commonly connected, and a TTL low level program pulse is applied to the  $\overline{CE}$  and  $\overline{PGM}$  of the desired device only and TTL high level signal is applied to the other devices.

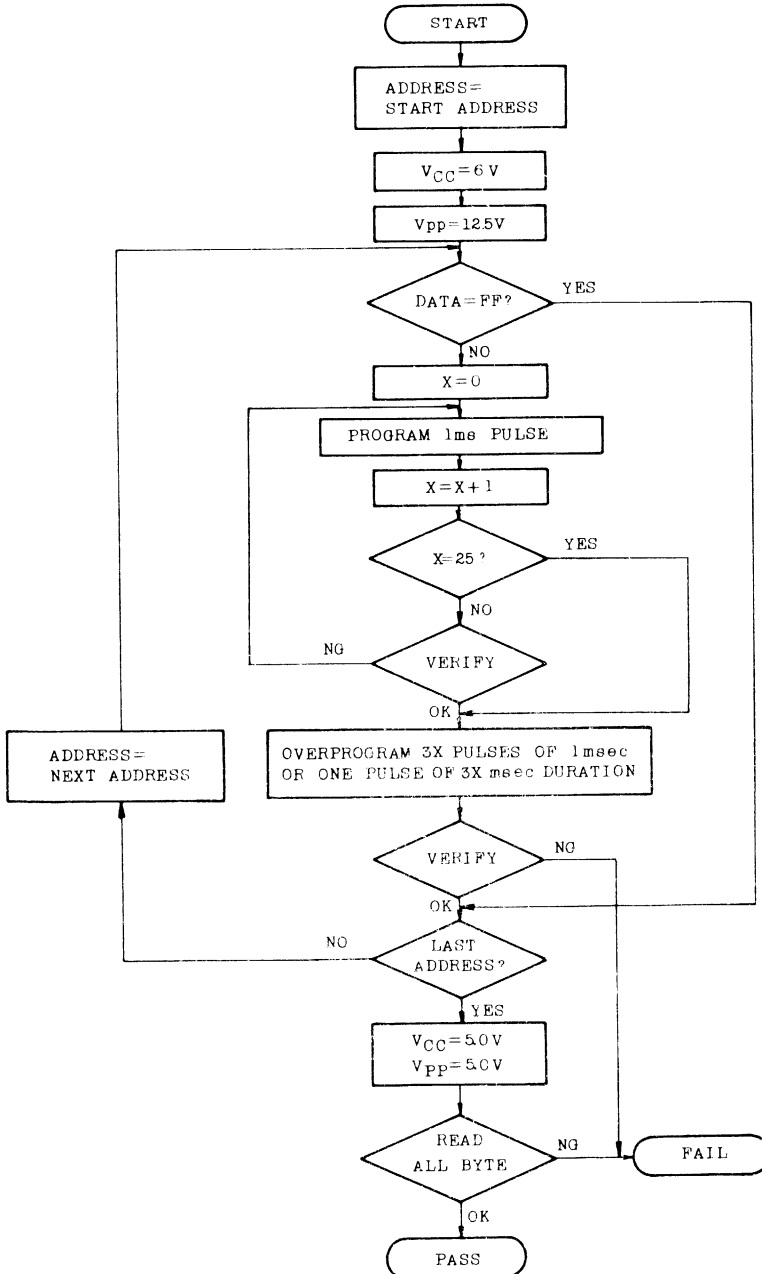
program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max.25 times)

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with  $V_{CC}=V_{PP}=5V$ .

# TMM2764ADI-15 TMM2764ADI-20

## HIGH SPEED PROGRAM MODE FLOW CHART





# TMM2764ADI-15

# TMM2764ADI-20

## ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TMM2764ADI which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from the TMM2764ADI by using this mode before program operation and automatically set program voltage ( $V_{pp}$ ) and algorithm.

Electric signature mode is set up when 12V is

applied to address line A9 and the rest of address lines are set to  $V_{LL}$  in read operation. Data output under these conditions is manufacturer code. Device code is identified when address A0 is set to  $V_{IH}$ . These two code possess an odd parity with the parity bit of MSB (07).

The following table shows electric signature of the TMM2764ADI.

	PINS	A <sub>9</sub> (10)	O <sub>7</sub> (19)	O <sub>6</sub> (18)	O <sub>5</sub> (17)	O <sub>4</sub> (16)	O <sub>3</sub> (15)	O <sub>2</sub> (13)	O <sub>1</sub> (12)	O <sub>0</sub> (11)	HEX DATA
Signature		$V_{LL}$	1	0	0	1	1	0	0	0	98
Device Code		$V_{IH}$	0	1	0	1	0	0	1	0	52

Notes: A9 = 12V ± 0.5V

A1 ~ A8, A10 ~ A12,  $\overline{CE}$ ,  $\overline{OE}$  =  $V_{LL}$

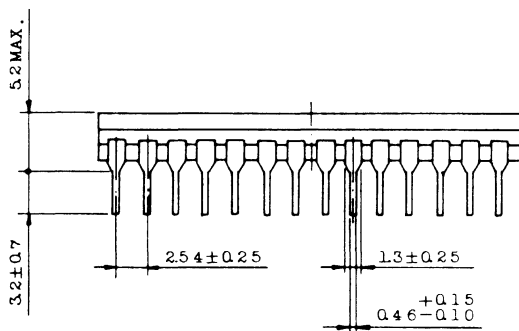
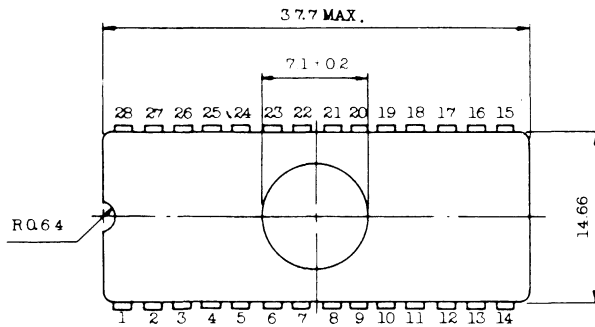
PGM =  $V_{IH}$

# TMM2764ADI-15

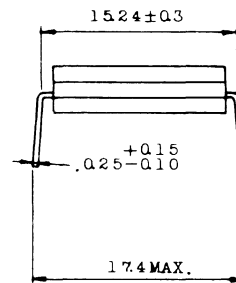
# TMM2764ADI-20

## OUTLINE DRAWINGS

Unit in mm



Note 1



Note 2

- Note: 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.  
 2. This value is measured at the end of leads.  
 3. All dimensions are in millimeters.

Toshiba does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.  
 May, 1986 Toshiba Corporation

# TOSHIBA MOS MEMORY PRODUCT

16,384 WORD × 8 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY  
N-CHANNEL SILICON STACKED GATE MOS

TMM27128AD-15, TMM27128AD-150  
TMM27128AD 20, TMM27128AD-200

## DESCRIPTION

The TMM27128AD is a 16,384 word × 8 bit ultra-violet light erasable and electrically programmable read only memory. For read operation, the TMM27128AD's access time is 150ns/200ns, and the TMM27128AD operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time.

## FEATURES

	-15	-20	-150	-200
V <sub>CC</sub>	5V ± 5%		5V ± 10%	
t <sub>ACC</sub>	150ns	200ns	150ns	200ns
I <sub>OP</sub>	100mA		120mA	
I <sub>CC1</sub>	30mA		35mA	

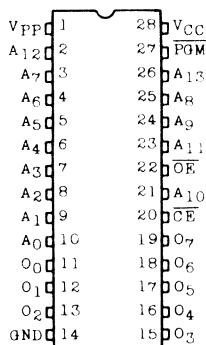
The standby mode is achieved by applying a TTL-high level signal to the  $\overline{CE}$  input.

For program operation, the program is achieved by using the high speed programming mode.

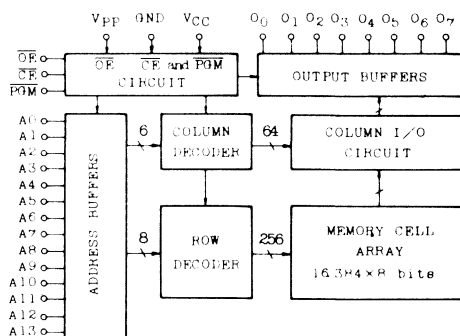
The TMM27128AD is fabricated with the N-channel silicon double layer gate MOS technology.

- Fully static operation
- High speed programming mode
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i27128A

## PIN CONNECTION (TOP VIEW)



## BLOCK DIAGRAM



## PIN NAMES

A <sub>0</sub> ~A <sub>13</sub>	Address Inputs
O <sub>0</sub> ~O <sub>7</sub>	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
PGM	Program Control Input
V <sub>PP</sub>	Program Supply Voltage
V <sub>CC</sub>	V <sub>CC</sub> Supply Voltage (+5V)
GND	Ground

## MODE SELECTION

MODE	PIN	PGM (27)	CE (20)	OE (22)	V <sub>PP</sub> (1)	V <sub>CC</sub> (28)	O <sub>0</sub> ~O <sub>7</sub> (11~13, 15~19)	POWER
Read		H	L	L	5V	5V	Data Out	Active
Output Deselect		*	*	H			High Impedance	
Standby		*	H	*	12.5V	6V	High Impedance	Standby
Program		L	L	*			Data In	
Program Inhibit		*	H	*			High Impedance	
Program Verify		H	L	H			High Impedance	
		H	L	L			Data Out	Active

Note \* : H or L

**TMM27128AD-15, TMM27128AD-150**  
**TMM27128AD-20, TMM27128AD-200**

**MAXIMUM RATINGS**

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	-0.6~7.0	V
V <sub>PP</sub>	Program Supply Voltage	-0.6~14.0	V
V <sub>IN</sub>	Input Voltage	-0.6~7.0	V
V <sub>OUT</sub>	Output Voltage	-0.6~7.0	V
P <sub>D</sub>	Power Dissipation	1.5	W
T <sub>SOLED</sub>	Soldering Temperature · Time	260 · 10	C·sec
T <sub>STAG</sub>	Storage Temperature	-65~125	C
T <sub>OPR</sub>	Operating Temperature	0~70	C

**READ OPERATION**

**D. C. RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	TMM27128AD-15, 20	TMM27128AD-150, 200
T <sub>a</sub>	Operating Temperature	0~70 C	0~70 C
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	5V±5%	5V±10%
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	2.0~V <sub>CC</sub> +0.6V	2.0~V <sub>CC</sub> +0.6V

**D. C. AND OPERATING CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>LI</sub>	Input Current	V <sub>IN</sub> =0~V <sub>CC</sub>	—	—	±10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> =0.4~V <sub>CC</sub>	—	—	±10	μA
I <sub>CC1</sub>	Supply Current (Standby)	$\overline{CE} = V_{IH}$	-15/20	—	30	mA
			-150/200	—	35	
I <sub>CC2</sub>	Supply Current (Active)	$\overline{CE} = V_{IL}$	-15/20	—	100	mA
			-150/200	—	120	
V <sub>IH</sub>	Input High Voltage	—	2.0	—	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input Low Voltage	—	-0.3	—	0.8	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400μA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA	—	—	0.4	V
I <sub>PP1</sub>	V <sub>PP</sub> Current	V <sub>PP</sub> =0~V <sub>CC</sub> +0.6	—	—	±10	μA

**TMM27128AD-15, TMM27128AD-150  
TMM27128AD-20, TMM27128AD-200**

**A. C. CHARACTERISTICS**

SYMBOL	PARAMETER	TMM27128AD 15 150		TMM27128AD 20 200		UNIT
		MIN.	MAX.	MIN.	MAX.	
$t_{ACC}$	Address Access Time	-	150	-	200	ns
$t_{CE}$	CE to Output Valid	-	150	-	200	ns
$t_{OE}$	OE to Output Valid	-	70	-	70	ns
$t_{PGM}$	PGM to Output Valid	-	70	-	70	ns
$t_{CE-HZ}$	CE to Output in High Z	0	60	0	60	ns
$t_{OE-HZ}$	OE to Output in High Z	0	60	0	60	ns
$t_{PGM-HZ}$	PGM to Output in High Z	0	60	0	60	ns
$t_{OH}$	Output Data Hold Time	0	-	0	-	ns

**A. C. TEST CONDITIONS**

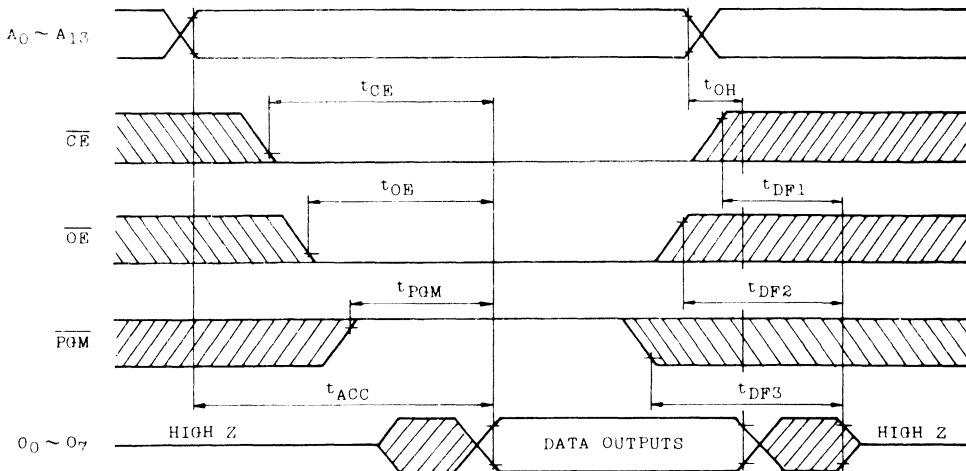
- Output Load : 1 TTL Gate and  $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

**CAPACITANCE \* ( $T_a = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ )**

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
$C_{IN}$	Input Capacitance	$V_{IN} = 0\text{V}$	-	4	6	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0\text{V}$	-	8	12	pF

\* This parameter is periodically sampled is not 100% tested.

**TIMING WAVEFORMS (READ)**



**TMM27128AD-15, TMM27128AD-150**  
**TMM27128AD-20, TMM27128AD-200**

**HIGH SPEED PROGRAM OPERATION**

**D. C. RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.0	—	V <sub>CC</sub> + 1.0	V
V <sub>IL</sub>	Input Low Voltage	-0.3	—	0.8	V
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	5.75	6.0	6.25	V
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	12.0	12.5	13.0	V

**D. C. and OPERATING CHARACTERISTICS** (T<sub>a</sub> = 25 ± 5 °C, V<sub>CC</sub> = 6V ± 0.25V, V<sub>PP</sub> = 12.5V ± 0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>I1</sub>	Input Current	V <sub>IN</sub> = 0 ~ V <sub>CC</sub>	—	—	± 10	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400 μA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA	—	—	0.4	V
I <sub>CC</sub>	V <sub>CC</sub> Supply Current	—	—	—	120	mA
I <sub>PP2</sub>	V <sub>PP</sub> Supply Current	V <sub>PP</sub> = 13.0V	—	—	50	mA
V <sub>ID</sub>	A9 Auto Select Voltage	—	11.5	12.0	12.5	V

**A. C. PROGRAMMING CHARACTERISTICS** (T<sub>a</sub> = 25 ± 5 °C, V<sub>CC</sub> = 6V ± 0.25V, V<sub>PP</sub> = 12.5V ± 0.5V)

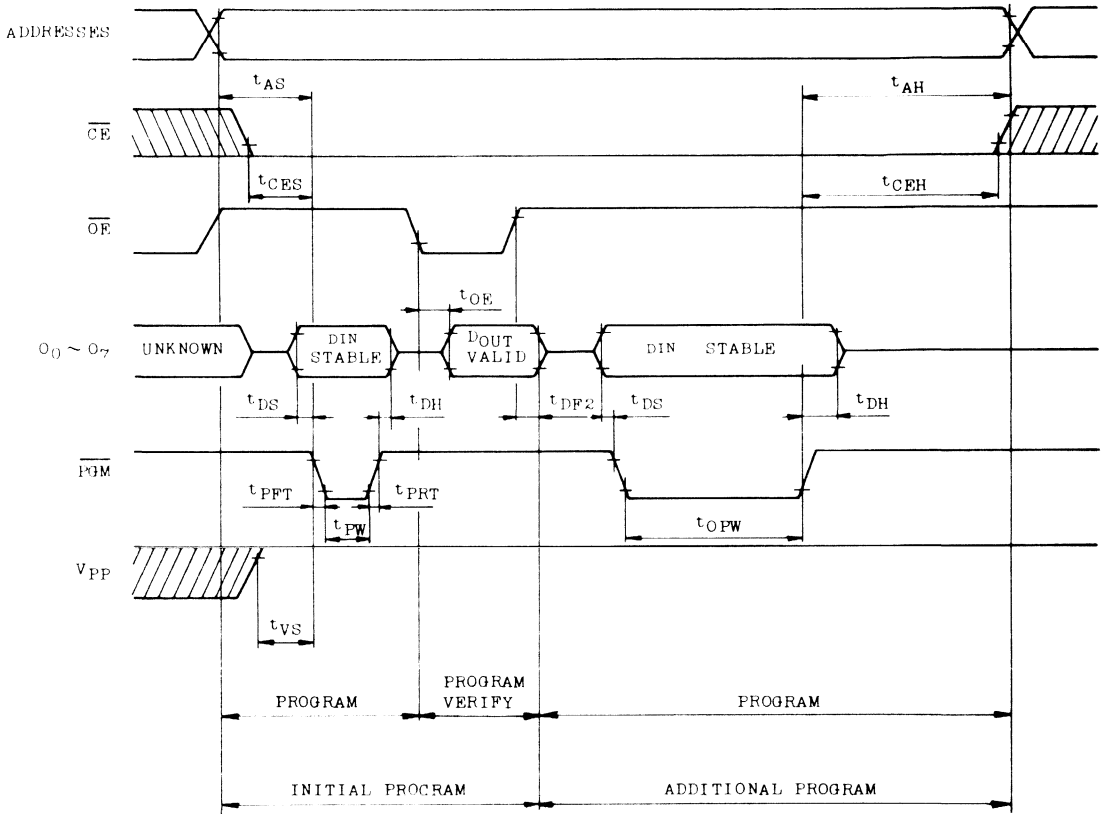
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t <sub>AS</sub>	Address Setup Time	—	2	—	—	μS
t <sub>AH</sub>	Address Hold Time	—	2	—	—	μS
t <sub>CE S</sub>	CE Setup Time	—	2	—	—	μS
t <sub>CE H</sub>	CE Hold Time	—	2	—	—	μS
t <sub>DS</sub>	Data Setup Time	—	2	—	—	μS
t <sub>DH</sub>	Data Hold Time	—	2	—	—	μS
t <sub>VS</sub>	V <sub>PP</sub> Setup Time	—	2	—	—	μS
t <sub>PW</sub>	Program Pulse Width	—	0.95	1.0	1.05	ms
t <sub>DPW</sub>	Additional Program Pulse Width	Note 1	2.85	3	78.75	ms
t <sub>PRT</sub>	Program pulse Rise Time	—	5	—	—	ns
t <sub>PF1</sub>	Program Pulse Fall Time	—	5	—	—	ns
t <sub>OE</sub>	OE to Output Valid Valid	—	—	—	100	ns
t <sub>DF2</sub>	OE to Output is High-Z	CE = V <sub>IL</sub>	—	—	90	ns

**A. C. TEST CONDITIONS**

- Output Load : 1 TTL Gate and C<sub>L</sub> (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

**TMM27128AD-15, TMM27128AD-150  
TMM27128AD-20, TMM27128AD-200**

**TIMING WAVEFORMS (READ)**



- Note :
1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and cut off simultaneously or after  $V_{PP}$ .
  2. Removing the device from socket and setting the device in socket with  $V_{PP}=12.5V$  may cause permanent damage to the device.
  3. The  $V_{PP}$  supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the  $V_{PP}$  terminal.
- When the switching pulse voltage is applied to the  $V_{PP}$  terminal, the overshoot voltage of its pulse should not be exceeded 14V.

# TMM27128AD-15, TMM27128AD-150 TMM27128AD-20, TMM27128AD-200

## ERASURE CHARACTERISTICS

The TMM27128AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) through the chips transparent window.

The integrated dose (ultraviolet light intensity [W/cm<sup>2</sup>] × exposure time [sec.]) for erasure should be a minimum of 15 [W.sec/cm<sup>2</sup>].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is 12000 [μw/cm<sup>2</sup>] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm<sup>2</sup>] × (20×60) [sec] ≅ 15 [w·sec/cm<sup>2</sup>].)

The TMM27128AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. Sunlight and flourescent lamps include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

## OPERATION INFORMATION

The TMM27128AD's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

MODE		PIN NAMES (NUMBER)	PGM (27)	CE (20)	OE (22)	V <sub>PP</sub> (1)	V <sub>CC</sub> (28)	O <sub>0</sub> ~O <sub>7</sub> (11~13, 15~19)	POWER
READ OPERATION (T <sub>a</sub> =0~70°C)	Read		H	L	L	5V	5V	Data Out	Active
	Output Deselect		*	*	H			High Impedance	Active
	Standby		*	H	*			High Impedance	Standby
PROGRAM OPERATION (T <sub>a</sub> =25±5°C)	Program		L	L	*	12.5V	6V	Data In	Active
	Program Inhibit		*	H	*			High Impedance	Active
			H	L	H			High Impedance	Active
		Program Verify		H	L			L	Data Out

Note H : V<sub>IH</sub>, L : V<sub>IL</sub>, \* : V<sub>IH</sub> or V<sub>IL</sub>

## READ MODE

The TMM27128AD has three control functions. The chip enable ( $\overline{CE}$ ) controls the operation power and should be used for device selection.

The output enable ( $\overline{OE}$ ) and the program control ( $\overline{PGM}$ ) control the output buffers, independent of device selection.

Assuming that  $\overline{CE} = \overline{OE} = V_{IL}$  and  $\overline{PGM} = V_{IH}$ , the output data is valid at the output after address access time from stabilizing of all addresses.

The  $\overline{CE}$  to output valid ( $t_{CE}$ ) is equal to the address access time ( $t_{ACC}$ ).

Assuming that  $\overline{CE} = V_{IL}$ ,  $\overline{PGM} = V_{IH}$  and all addresses are valid, the output is valid at the outputs after  $t_{OE}$  from the falling edge of  $\overline{OE}$ .

And assuming that  $\overline{CE} = \overline{OE} = V_{IL}$  and all addresses are valid, the output data is valid at the outputs after  $t_{PGM}$  from the rising edge of  $\overline{PGM}$ .

## OUTPUT Deselect MODE

Assuming that  $\overline{CE} = V_{IH}$  or  $\overline{OE} = V_{IH}$ , the outputs will be in high impedance state. Thus, two or more TMM27128AD's can be connected

together on a common bus line.

When  $\overline{CE}$  is decoded for device selection, all deselected devices are in low power standby mode.



## **TMM27128AD-15, TMM27128AD-150 TMM27128AD-20, TMM27128AD-200**

### **STANDBY MODE**

The TMM27128AD has a low power standby mode controlled by the  $\overline{CE}$  signal.

By applying a TTL high level to the  $\overline{CE}$  input, the TMM27128AD is placed in the standby mode which

reduces 70% of operating current. The outputs are in a high impedance state, independent of the  $\overline{OE}$  and the  $\overline{PGM}$  inputs.

### **PROGRAM MODE**

Initially, when received by customers, all bits of the TMM27128AD are in the "1" state which is the erased state.

The programming operation introduces "0s" data into the desired bit locations by electrical programming.

The levels required for all inputs are TTL.

The TMM27128AD can be programmed at any location, anytime — either individually, sequentially or at random.

### **PROGRAM VERIFY MODE**

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with  $\overline{OE}$  and  $\overline{CE}$  at  $V_{IH}$  and  $\overline{PGM}$  at  $V_{IH}$ .

### **PROGRAM INHIBIT MODE**

Under the condition that the program voltage (+12.5V) is applied to  $V_{PP}$  terminal, a high level  $\overline{CE}$  or  $\overline{PGM}$  input inhibits the TMM27128AD from being programmed.

Programming of two or more TMM27128AD's in parallel with different data is easily accomplished.

That is, all inputs except for  $\overline{CE}$  or  $\overline{PGM}$  may be commonly connected, and a TTL low level program pulse is applied to the  $\overline{CE}$  and  $\overline{PGM}$  of the desired device only and TTL high level signal is applied to the other devices.

### **HIGH SPEED PROGRAMMING MODE**

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the  $V_{PP}$  terminal with  $V_{CC} = 6V$  and  $\overline{PGM} = V_{IH}$ .

The programming is achieved by applying a single TTL low level 1ms pulse the  $\overline{PGM}$  input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another

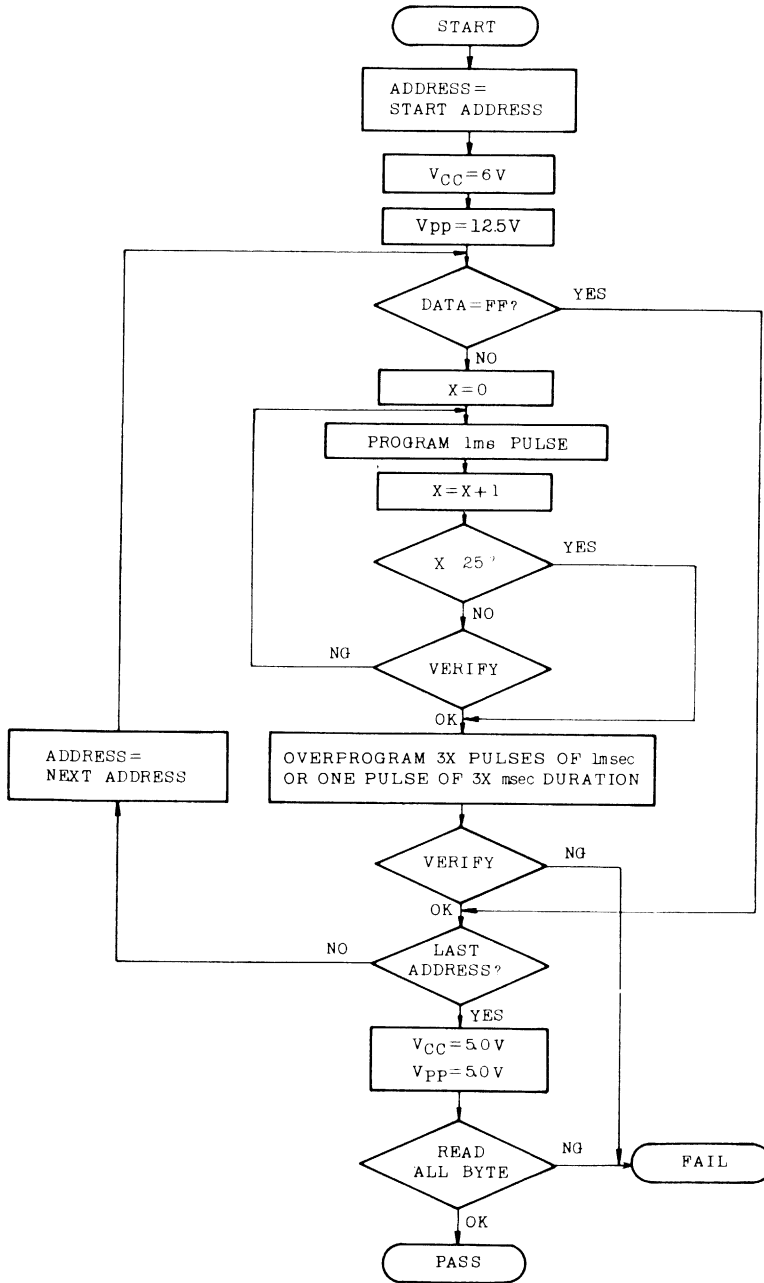
program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times)

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with  $V_{CC} = V_{PP} = 5V$ .

**TMM27128AD-15, TMM27128AD-150  
TMM27128AD-20, TMM27128AD-200**

**HIGH SPEED PROGRAM MODE FLOW CHART**



**TMM27128AD-15, TMM27128AD-150  
TMM27128AD-20, TMM27128AD-200**

**ELECTRIC SIGNATURE MODE**

Electric signature mode allows a code to be read from the TMM27128AD which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from the TMM2764AD by using this mode before program operation and automatically set program voltage ( $V_{pp}$ ) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to  $V_{IL}$  in read operation. Data output is this conditions is manufacturer code. Device code is identified when address A0 is set to  $V_{IH}$ . These two code possess an odd parity with the parity bit of MSB (O7).

The following table shows electric signature of the TMM27128AD.

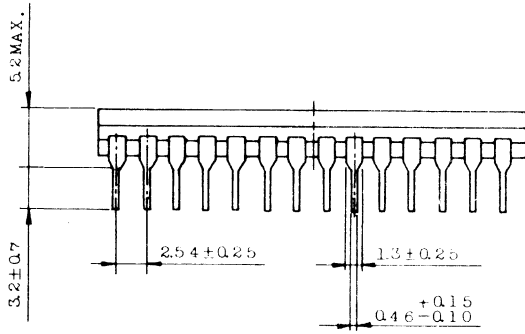
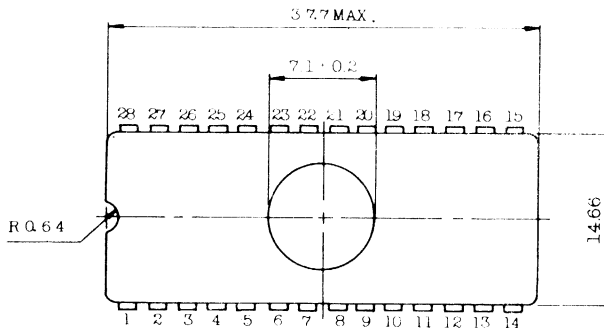
SIGNATURE	PINS	A <sub>0</sub> (10)	O <sub>7</sub> (19)	O <sub>6</sub> (18)	O <sub>5</sub> (17)	O <sub>4</sub> (16)	O <sub>3</sub> (15)	O <sub>2</sub> (13)	O <sub>1</sub> (12)	O <sub>0</sub> (11)	HEX. DATA
Manufacture Code	$V_{IL}$	1	0	0	0	1	1	0	0	0	98
Device Code	$V_{IH}$	1	1	0	0	1	0	0	1	1	D3

Notes A9 = 12V ± 0.5V  
A1 ~ A8, A10 ~ A13,  $\overline{CE}$ ,  $\overline{OE}$  =  $V_{IL}$   
PGM =  $V_{IH}$

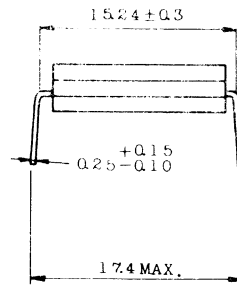
**TMM27128AD-15, TMM27128AD-150  
TMM27128AD-20, TMM27128AD-200**

**OUTLINE DRAWINGS**

Unit in mm



Note 1



Note 2

- Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.  
 2. This value is measured at the end of leads.  
 3. All dimensions are in millimeters.

**TMM27128AD-15, TMM27128AD-150**  
**TMM27128AD-20, TMM27128AD-200**

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**TMM27128AD-15, TMM27128AD-150**  
**TMM27128AD-20, TMM27128AD-200**

# TOSHIBA MOS MEMORY PRODUCT

16,384 WORD × 8 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY  
N-CHANNEL SILICON STACKED GATE MOS

## TMM27128ADI-15 TMM27128ADI-20

### DESCRIPTION

The TMM27128ADI is a 16,384 word × 8 bit ultra-violet light erasable and electrically programmable read only memory. For read operation, the TMM27128ADI's access time is 150ns/200ns, and the TMM27128ADI operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time.

The standby mode is achieved by applying a TTL-high level signal to the  $\overline{CE}$  input.

For program operation, the program is achieved by using the high speed programming mode.

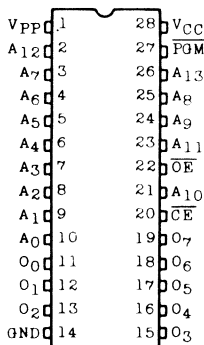
The TMM27128ADI is fabricated with the N-channel silicon double layer gate MOS technology.

### FEATURES

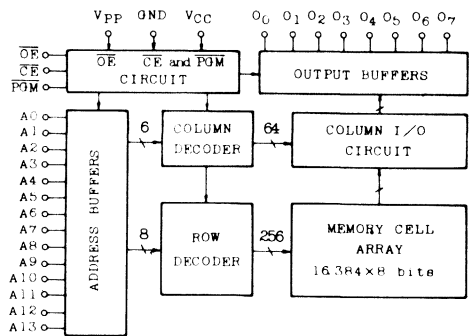
	-15	-20
V <sub>CC</sub>	5V ± 5%	
t <sub>ACC</sub>	150ns	200ns
I <sub>CC2</sub>	100mA	
I <sub>CC1</sub>	30mA	

- Wide operating temperature range -40~85°C
- Full static operation
- High speed programming mode
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i27128A

### PIN CONNECTION (TOP VIEW)



### BLOCK DIAGRAM



### MODE SELECTION

MODE	PIN	PGM (27)	CE (20)	OE (22)	V <sub>PP</sub> (1)	V <sub>CC</sub> (28)	O <sub>0</sub> ~O <sub>7</sub> (11~13, 15~19)	POWER
Read		H	L	L	5V	5V	Data Out	Active
Output Deselect		*	*	H			High Impedance	
Standby		*	H	*			High Impedance	
Program		L	L	*	12.5V	6V	Data In	Active
Program Inhibit		*	H	*			High Impedance	
		H	L	H			High Impedance	
Program Verify		H	L	L			Data Out	

Note \* : H or L

### PIN NAMES

A <sub>0</sub> ~A <sub>13</sub>	Address Inputs
O <sub>0</sub> ~O <sub>7</sub>	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
PGM	Program Control Input
V <sub>PP</sub>	Program Supply Voltage
V <sub>CC</sub>	V <sub>CC</sub> Supply Voltage (+5V)
GND	Ground

# TMM27128ADI-15

# TMM27128ADI-20

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	-0.6~7.0	V
V <sub>PP</sub>	Program Supply Voltage	-0.6~14.0	V
V <sub>IN</sub>	Input Voltage	-0.6~7.0	V
V <sub>OUT</sub>	Output Voltage	-0.6~7.0	V
P <sub>D</sub>	Power Dissipation	1.5	W
T <sub>SOLDER</sub>	Soldering Temperature · Time	260 · 10	°C·sec
T <sub>STG</sub>	Storage Temperature	-65~125	°C
T <sub>OPR</sub>	Operating Temperature	-40~85	°C

## READ OPERATION

### D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27128ADI-15/20
T <sub>a</sub>	Operating Temperature	-40~85°C
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	5V±5%
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	2.0~V <sub>CC</sub> ±0.6V

### D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>LI</sub>	Input Current	V <sub>IN</sub> =0~V <sub>CC</sub>	—	—	±10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> =0.4~V <sub>CC</sub>	—	—	±10	μA
I <sub>CC1</sub>	Supply Current (Standby)	$\overline{CE} = V_{IH}$	—	—	35	mA
I <sub>CC2</sub>	Supply Current (Active)	$\overline{CE} = V_{IL}$	—	—	120	mA
V <sub>IH</sub>	Input High Voltage	—	2.0	—	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input Low Voltage	—	-0.3	—	0.8	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> =-400μA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> =2.1mA	—	—	0.4	V
I <sub>PP1</sub>	V <sub>PP</sub> Current	V <sub>PP</sub> =0~V <sub>CC</sub> +0.6	—	—	±10	μA



# TMM27128ADI-15

# TMM27128ADI-20

## A. C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM27128ADI-15		TMM27128ADI-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
$t_{ACC}$	Address Access Time	--	150	--	200	ns
$t_{CE}$	$\overline{CE}$ to Output Valid	--	150	--	200	ns
$t_{OE}$	$\overline{OE}$ to Output Valid	--	70	--	70	ns
$t_{PGM}$	$\overline{PGM}$ to Output Valid	--	70	--	70	ns
$t_{DH1}$	$\overline{CE}$ to Output in High-Z	0	60	0	60	ns
$t_{DF2}$	$\overline{OE}$ to Output in High-Z	0	60	0	60	ns
$t_{DF3}$	$\overline{PGM}$ to Output in High-Z	0	60	0	60	ns
$t_{DH}$	Output Data Hold Time	0	--	0	--	ns

## A. C. TEST CONDITIONS

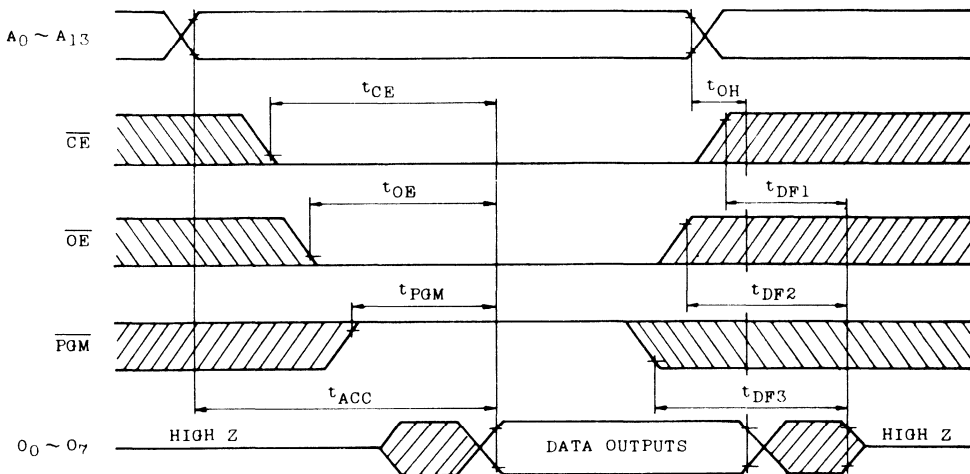
- Output Load : 1 TTL Gate and  $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

## CAPACITANCE \* ( $T_a = 25^\circ C$ , $f = 1MHz$ )

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	--	4	6	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V$	--	8	12	pF

\* This parameter is periodically sampled is not 100% tested.

## TIMING WAVEFORMS (READ)



# TMM27128ADI-15

# TMM27128ADI-20

## HIGH SPEED PROGRAM OPERATION

### D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{IH}$	Input High Voltage	2.2	—	$V_{CC} + 1.0$	V
$V_{IL}$	Input Low Voltage	-0.3	—	0.8	V
$V_{CC}$	$V_{CC}$ Power Supply Voltage	5.75	6.0	6.25	V
$V_{PP}$	$V_{PP}$ Power Supply Voltage	12.0	12.5	13.0	V

### D. C. and OPERATING CHARACTERISTICS (Ta = 25 ± 5 C, VCC = 6V ± 0.25V, VPP = 12.5V ± 0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$I_{LI}$	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	±10	μA
$V_{OH}$	Output High Voltage	$I_{OH} = -400\mu A$	2.4	—	—	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2.1mA$	—	—	0.4	V
$I_{CC}$	$V_{CC}$ Supply Current	—	—	—	120	mA
$I_{PP2}$	$V_{PP}$ Supply Current	$V_{PP} = 13.0V$	—	—	50	mA
$V_{ID}$	A9 Auto Select Voltage	—	11.5	12.0	12.5	V

### A. C. PROGRAMMING CHARACTERISTICS (Ta = 25 ± 5 C, VCC = 6V ± 0.25V, VPP = 12.5V ± 0.5V)

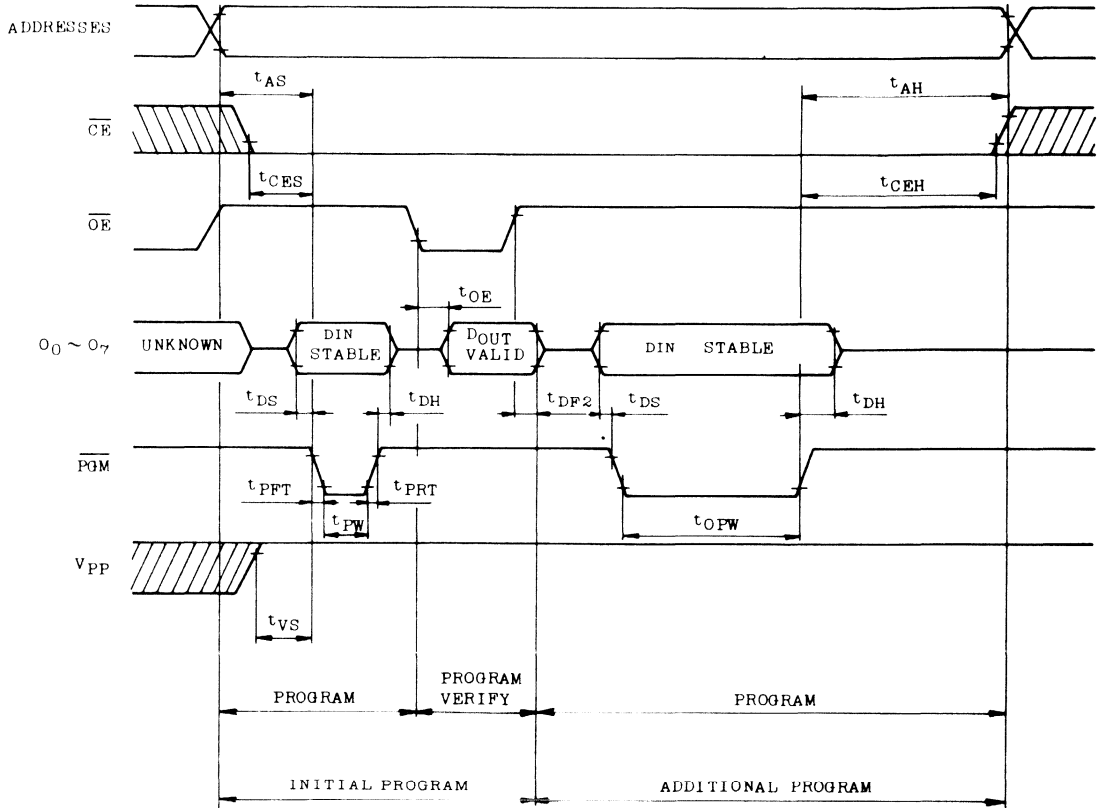
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$t_{AS}$	Address Setup Time	—	2	—	—	μs
$t_{AH}$	Address Hold Time	—	2	—	—	μs
$t_{CES}$	$\overline{CE}$ Setup Time	—	2	—	—	μs
$t_{CEH}$	$\overline{CE}$ Hold Time	—	2	—	—	μs
$t_{DS}$	Data Setup Time	—	2	—	—	μs
$t_{DH}$	Data Hold Time	—	2	—	—	μs
$t_{VS}$	$V_{PP}$ Setup Time	—	2	—	—	μs
$t_{PW}$	Program Pulse Width	—	0.95	1.0	1.05	ms
$t_{OPW}$	Additional Program Pulse Width	Note 1	2.85	3	78.75	ms
$t_{PR1}$	Program pulse Rise Time	—	5	—	—	ns
$t_{PF1}$	Program Pulse Fall Time	—	5	—	—	ns
$t_{OE}$	$\overline{OE}$ to Output Valid Valid	—	—	—	100	ns
$t_{DF2}$	$\overline{OE}$ to Output is High-Z	$\overline{CE} = V_{IL}$	—	—	90	ns

### A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and  $C_L$  (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

# TMM27128ADI-15 TMM27128ADI-20

## TIMING WAVEFORMS (READ)



- Note :
1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and cut off simultaneously or after  $V_{PP}$ .
  2. Removing the device from socket and setting the device in socket with  $V_{PP}=12.5V$  may cause permanent damage to the device.
  3. The  $V_{PP}$  supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the  $V_{PP}$  terminal.

When the switching pulse voltage is applied to the  $V_{PP}$  terminal, the overshoot voltage of its pulse should not be exceeded 14V.

# TMM27128ADI-15

# TMM27128ADI-20

## ERASURE CHARACTERISTICS

The TMM27128ADI's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) of the chip through the transparent window.

The integrated dose (ultraviolet light intensity [W/cm<sup>2</sup>] × exposure time [sec.]) for erasure should be a minimum of 15 [W.sec/cm<sup>2</sup>]

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is 12000 [μw/cm<sup>2</sup>] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm<sup>2</sup>] × (20×60) [sec] ≈ 15 [w·sec/cm<sup>2</sup>].)

The TMM27128ADI's erasure begins to occur when exposed to light with wavelengths shorter than 4000Å. Sunlight and flourescent lamps include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

## OPERATION INFORMATION

The TMM27128ADI's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

MODE		PIN NAME (MODE)	PGM (27)	CE (20)	OE (22)	V <sub>PP</sub> (1)	V <sub>CC</sub> (28)	O <sub>0</sub> ~O <sub>7</sub> (11~13, 15~19)	POWER
READ OPERATION (T <sub>a</sub> = -40~85°C)	Read		H	L	L	5V	5V	Data Out	Active
	Output Deselect		*	*	H			High Impedance	Active
	Standby		*	H	*			High Impedance	Standby
PROGRAM OPERATION (T <sub>a</sub> = 25 ± 5°C)	Program		L	L	*	12.5V	6V	Data In	Active
	Program Inhibit		*	H	*			High Impedance	Active
			H	L	H			High Impedance	Active
	Program Verify		H	L	L			Data Out	Active

Note H : V<sub>IH</sub>, L : V<sub>IL</sub>, \* : V<sub>IH</sub> or V<sub>IL</sub>

## READ MODE

The TMM27128ADI has three control functions. The chip enable ( $\overline{CE}$ ) controls the operation power and should be used for device selection.

The output enable ( $\overline{OE}$ ) and the program control ( $\overline{PGM}$ ) control the output buffers, independent of device selection.

Assuming that  $\overline{CE} = \overline{OE} = V_{IL}$  and  $\overline{PGM} = V_{IH}$ , the output data is valid at the output after address access time from stabilizing of all addresses.

The  $\overline{CE}$  to output valid ( $t_{CE}$ ) is equal to the address access time ( $t_{ACC}$ ).

Assuming that  $\overline{CE} = V_{IL}$ ,  $\overline{PGM} = V_{IH}$  and all addresses are valid, the output is valid at the outputs after  $t_{OE}$  from the falling edge of  $\overline{OE}$ .

And assuming that  $\overline{CE} = \overline{OE} = V_{IL}$  and all addresses are valid, the output data is valid at the outputs after  $t_{PGM}$  from the rising edge of  $\overline{PGM}$ .

## OUTPUT Deselect MODE

Assuming that  $\overline{CE} = V_{IH}$  or  $\overline{OE} = V_{IH}$ , the outputs will be in high impedance state.

So two or more TMM27128ADI's can be connected

together on a common bus line.

When  $\overline{CE}$  is decoded for device selection, all deselected devices are in low power standby mode.

# TMM27128ADI-15

# TMM27128ADI-20

## STANDBY MODE

The TMM27128ADI has a low power standby mode controlled by the  $\overline{CE}$  signal.

By applying a TTL high level to the  $\overline{CE}$  input, the TMM27128ADI is placed in the standby mode which

reduces 70% of operating current. The outputs are then in a high impedance state, independent of the  $\overline{OE}$  and the  $\overline{PGM}$  inputs.

## PROGRAM MODE

Initially, when received by customers, all bits of the TMM27128ADI are in the "1" state which is the erased state.

The programming operation introduces "0s" data into the desired bit locations by electrical program-

ming.

The levels required for all inputs are TTL.

The TMM27128ADI can be programmed at any location, anytime — either individually, sequentially or at random.

## PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with  $\overline{OE}$  and  $\overline{CE}$  at  $V_{IL}$  and  $\overline{PGM}$  at  $V_{IH}$ .

## PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to  $V_{PP}$  terminal, a high level  $\overline{CE}$  or  $\overline{PGM}$  input inhibits the TMM27128ADI from being programmed.

Programming of two or more TMM27128ADI's in parallel with different data is easily accomplished.

That is, all inputs except for  $\overline{CE}$  or  $\overline{PGM}$  may be commonly connected, and a TTL low level program pulse is applied to the  $\overline{CE}$  and  $\overline{PGM}$  of the desired device only and TTL high level signal is applied to the other devices.

## HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the  $V_{PP}$  terminal with  $V_{CC} = 6V$  and  $\overline{PGM} = V_{IH}$ .

The programming is achieved by applying a single TTL low level 1ms pulse the  $\overline{PGM}$  input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another

program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times)

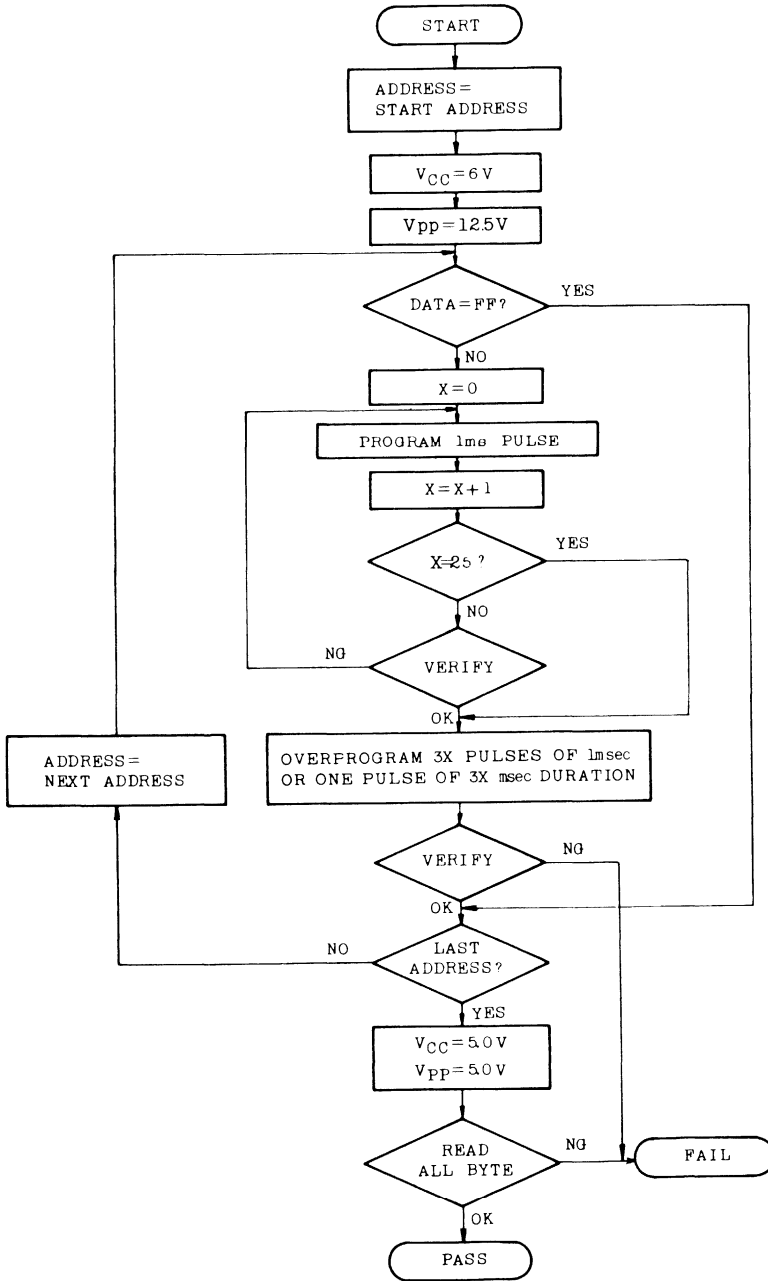
After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with  $V_{CC} = V_{PP} = 5V$ .

# TMM27128ADI-15

# TMM27128ADI-20

## HIGH SPEED PROGRAM MODE FLOW CHART



# TMM27128ADI-15

# TMM27128ADI-20

## ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TMM27128ADI which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from the TMM27128ADI by using this mode before program operation and automatically set program voltage ( $V_{PP}$ ) and algorithm.

Electric signature mode is set up when 12V is

applied to address line A9 and the rest of address lines are set to  $V_{IL}$  in read operation. Data output is this conditions is manufacturer code. Device code is identified when address A0 is set to  $V_{IH}$ . These two code possess an odd parity with the parity bit of MSB (07).

The following table shows electric signature of TMM27128ADI.

SIGNATURE \ PINS	A <sub>9</sub> (10)	O <sub>7</sub> (19)	O <sub>6</sub> (18)	O <sub>5</sub> (17)	O <sub>4</sub> (16)	O <sub>3</sub> (15)	O <sub>2</sub> (13)	O <sub>1</sub> (12)	O <sub>0</sub> (11)	HEX. DATA
Manufacture Code	$V_{IL}$	1	0	0	1	1	0	0	0	98
Device Code	$V_{IH}$	1	1	0	1	0	0	1	1	D3

Notes : A9 = 12V ± 0.5V

A1 ~ A8, A10 ~ A13,  $\overline{CE}$ ,  $\overline{OE}$  =  $V_{IL}$

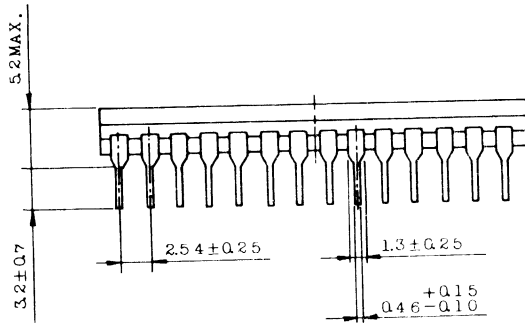
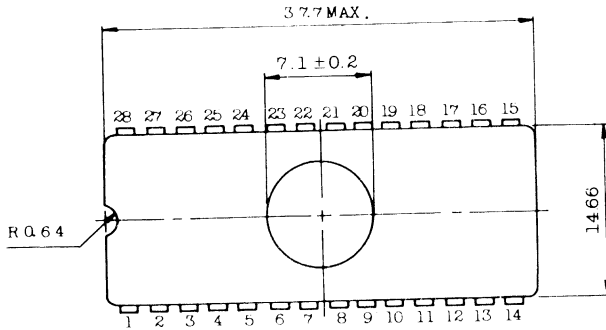
PGM =  $V_{IH}$

# TMM27128ADI-15

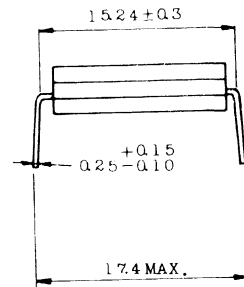
# TMM27128ADI-20

## OUTLINE DRAWINGS

Unit in mm



Note 1



Note 2

- Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No. 1 and No. 28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

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# TOSHIBA MOS MEMORY PRODUCT

32,768 WORD × 8 BIT N-MOS UV ERASABLE AND  
ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY  
SILICON STACKED GATE MOS

TMM27256AD-15, TMM27256AD-150  
TMM27256AD-20, TMM27256AD-200

## DESCRIPTION

The TMM27256AD is a 32,768 word × 8 bit ultraviolet light erasable and electrically programmable read only memory.

For read operation, the TMM27256AD's access time is 150ns-200ns, and the TMM27256AD operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby

mode is achieved by applying a TTL-high level signal to the  $\overline{CE}$  input.

For program operation, the programming is achieved by using the high speed programming mode.

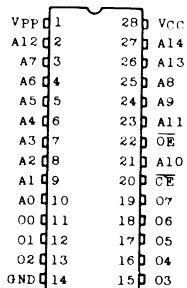
The TMM27256AD is fabricated with the N-channel silicon double layer gate MOS technology.

## FEATURES

	-15	-20	-150	-200
V <sub>cc</sub>	5V ± 5%		5V ± 10%	
t <sub>acc</sub>	150ns	200ns	150ns	200ns
I <sub>cc2</sub>	100mA		120mA	
I <sub>cc1</sub>	30mA		35mA	

- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with  $\mu$ 27256
- Standard 28 pin DIP cerdip package

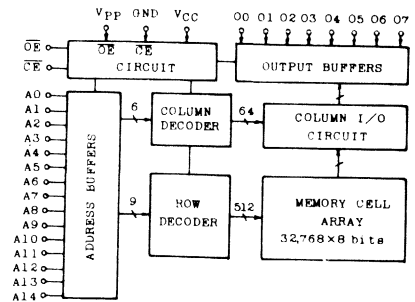
## PIN CONNECTION (TOP VIEW)



## PIN NAMES

A <sub>0</sub> ~A <sub>14</sub>	Address Inputs
O <sub>0</sub> ~O <sub>7</sub>	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V <sub>pp</sub>	Program Supply Voltage
V <sub>cc</sub>	V <sub>cc</sub> Supply Voltage (+5V)
GND	Ground

## BLOCK DIAGRAM



## MODE SELECTION

MODE	PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V <sub>pp</sub> (1)	V <sub>cc</sub> (28)	O <sub>0</sub> ~O <sub>7</sub> (11~13, 15~19)	POWER
Read		L	L	5V	5V	Data Out	Active
Output Deselect	*	H	High Impedance				
Standby	H	*	High Impedance			Standby	
Program		L	H	12.5V	6V	Data In	Active
Program Inhibit	H	*	High Impedance				
Program Verify	*	L	Data Out				

Note \* : H or L

**TMM27256AD-15, TMM27256AD-150**  
**TMM27256AD-20, TMM27256AD-200**

**MAXIMUM RATINGS**

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	-0.6~7.0	V
V <sub>PP</sub>	Program Supply Voltage	-0.6~14.0	V
V <sub>IN</sub>	Input Voltage	-0.6~7.0	V
V <sub>I/O</sub>	Input/Output Voltage	-0.6~7.0	V
P <sub>D</sub>	Power Dissipation	1.5	W
T <sub>SOLDER</sub>	Soldering Temperature · Time	260 · 10	°C·sec
T <sub>STG</sub>	Storage Temperature	-65~125	°C
T <sub>OPR</sub>	Operating Temperature	0~70	°C

**READ OPERATION**

**D. C. AND A. C. RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	TMM27256AD-15/20	TMM27256AD-150/200
T <sub>a</sub>	Operating Temperature	0~70°C	0~70°C
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	5V±5%	5V±10%
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	2.0~V <sub>CC</sub> ±0.6V	2.0~V <sub>CC</sub> +0.6V

**D. C. AND OPERATING CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>I1</sub>	Input Current	V <sub>IN</sub> =0~V <sub>CC</sub>	—	—	±10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> =0.4~V <sub>CC</sub>	—	—	±10	μA
I <sub>CC1</sub>	Supply Current (Standby)	$\overline{CE} = V_{IH}$	-15/20	—	30	mA
			-150/200	—	35	
I <sub>CC2</sub>	Supply Current (Active)	$\overline{CE} = V_{IL}$	-15/20	—	100	mA
			-150/200	—	120	
V <sub>IH</sub>	Input High Voltage	—	2.0	—	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input Low Voltage	—	-0.3	—	0.8	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> =-400μA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> =2.1mA	—	—	0.4	V
I <sub>PP1</sub>	V <sub>PP</sub> Current	V <sub>PP</sub> =0~V <sub>CC</sub> +0.6	—	—	±10	μA

**A. C. CHARACTERISTICS** (T<sub>a</sub>=0~70°C, V<sub>CC</sub>=5V±5%, V<sub>PP</sub>=2.0V~V<sub>CC</sub>+0.6V)

PARAMETER	TEST CONDITION	TMM27256AD-15/150		TMM27256AD-20/200		UNIT
		MIN.	MAX.	MIN.	MAX.	
t <sub>AC1</sub>	Address Access Time	—	150	—	200	ns
t <sub>CE</sub>	CE to Output Valid	—	150	—	200	ns
t <sub>OE</sub>	OE to Output Valid	—	70	—	70	ns
t <sub>DF1</sub>	CE to Output in High-Z	0	60	0	60	ns
t <sub>DF2</sub>	OE to Output in High-Z	0	60	0	60	ns
t <sub>OH</sub>	Output Data Hold Time	0	—	0	—	ns

A.C. Test Conditions

- ⚡ Output Load : 1 TTL Gate and C<sub>L</sub>=100pF
- ⚡ Input Pulse Rise and Fall Times : 10ns Max.
- ⚡ Input Pulse Levels : 0.45V to 2.4V
- ⚡ Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

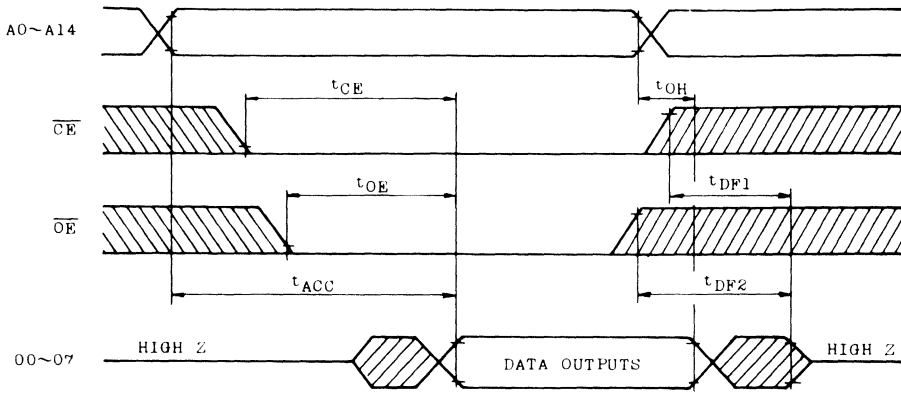
**TMM27256AD-15, TMM27256AD-150**  
**TMM27256AD-20, TMM27256AD-200**

**CAPACITANCE** \* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	—	4	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	—	8	12	pF

\* This parameter is periodically sampled and is not 100% tested.

**TIMING WAVEFORMS (READ)**



**PROGRAM OPERATION**

**D.C. RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.0	—	V <sub>CC</sub> + 1.0	V
V <sub>IL</sub>	Input Low Voltage	-0.3	—	0.8	V
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	5.75	6.0	6.25	V
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	12.0	12.5	13.0	V

**D.C. and OPERATING CHARACTERISTICS** (Ta = 25 ± 5°C, V<sub>CC</sub> = 6V ± 0.25V, V<sub>PP</sub> = 12.5V ± 0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>I1</sub>	Input Current	V <sub>IN</sub> = 0 ~ V <sub>CC</sub>	—	—	± 10	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400 μA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA	—	—	0.4	V
I <sub>CC</sub>	V <sub>CC</sub> Supply Current	—	—	—	120	mA
I <sub>PP2</sub>	V <sub>PP</sub> Supply Current	V <sub>PP</sub> = 13.0V	—	—	50	mA

**TMM27256AD-15, TMM27256AD-150**  
**TMM27256AD-20, TMM27256AD-200**

**A. C. PROGRAMMING CHARACTERISTICS** ( $T_a = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6V \pm 0.25V$ ,  $V_{PP} = 12.5V \pm 0.5V$ )

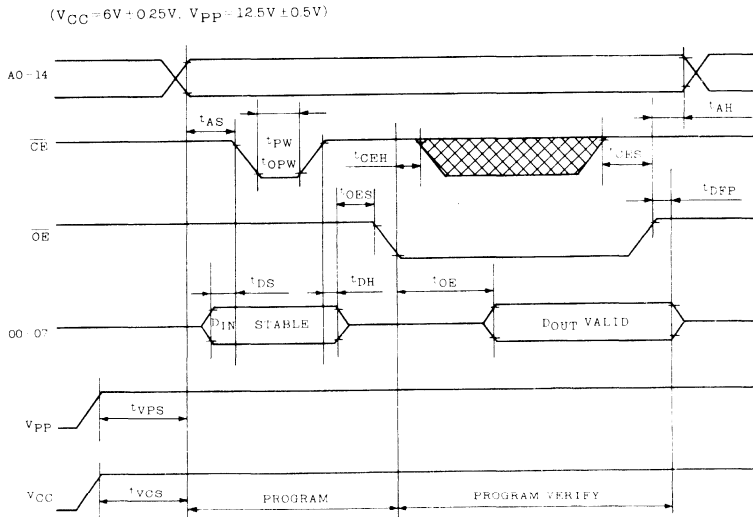
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$t_{AS}$	Address Setup Time	—	2	—	—	$\mu\text{s}$
$t_{AH}$	Address Hold Time	—	2	—	—	$\mu\text{s}$
$t_{CES}$	$\overline{CE}$ Setup Time	—	0	—	—	ns
$t_{CEH}$	$\overline{CE}$ Hold Time	—	0	—	—	ns
$t_{OES}$	$\overline{OE}$ Setup Time	—	2	—	—	$\mu\text{s}$
$t_{DS}$	Data Setup Time	—	2	—	—	$\mu\text{s}$
$t_{DH}$	Data Hold Time	—	2	—	—	$\mu\text{s}$
$t_{VPS}$	$V_{PP}$ Setup Time	—	2	—	—	$\mu\text{s}$
$t_{VCS}$	$V_{CC}$ Setup Time	—	2	—	—	$\mu\text{s}$
$t_{PW}$	Initial Program Pulse Width	$\overline{CE} = V_{IL}$ , $\overline{OE} = V_{IH}$	0.95	1	1.05	ms
$t_{OPW}$	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
$t_{OH}$	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IH}$	—	—	150	ns
$t_{OFF}$	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IH}$	—	—	130	ns

A. C. Test Conditions

- Output Load : 1 TTL Gate and  $C_L$  (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note : 1. The length of the overprogram pulse may vary as a function of the counter value X.

**TIMING WAVEFORMS (PROGRAM)**



- Note : 1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and cut off simultaneously or after  $V_{PP}$ .  
 2. Removing the device from socket and setting the device in socket with  $V_{PP} = 12.5V$  may cause permanent damage to the device.  
 3. The  $V_{PP}$  supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the  $V_{PP}$  terminal. When the switching pulse voltage is applied to the  $V_{PP}$  terminal, the overshoot voltage of its pulse should not be exceeded 14V.

# TMM27256AD-15, TMM27256AD-150 TMM27256AD-20, TMM27256AD-200

## ERASURE CHARACTERISTICS

The TMM27256AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) through the chips transparent window.

The integrated dose (ultraviolet light intensity [ $\mu\text{w}/\text{cm}^2$ ]  $\times$  exposure time [sec.]) for erasure should be a minimum of 15 [ $\mu\text{w}\cdot\text{sec}/\text{cm}^2$ ].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is 12000 [ $\mu\text{w}/\text{cm}^2$ ] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [ $\mu\text{w}/\text{cm}^2$ ]  $\times$  (20 $\times$ 60) [sec]  $\cong$  15 [ $\mu\text{w}\cdot\text{sec}/\text{cm}^2$ ].)

The TMM27256AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. Sunlight and fluorescent lamps include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

## OPERATION INFORMATION

The TMM27256AD's six operation modes are listed in the following table. Mode selection can be

achieved by applying TTL level signal to all inputs.

MODE	PIN NAMES(NUMBER)	CE (20)	OE (22)	V <sub>PP</sub> (1)	V <sub>CC</sub> (28)	O <sub>0</sub> ~O <sub>7</sub> (11~13, 15~19)	POWER
Read Operation (T <sub>a</sub> =0~70°C)	Read	L	L	5 V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	Active
	Standby	H	*			High Impedance	Standby
Program Operation (T <sub>a</sub> =25±5°C)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	*			High Impedance	Active
	Program Verify	*	L			Data Out	Active

Note H : V<sub>IH</sub>, L : V<sub>IL</sub>, \* : V<sub>IH</sub> or V<sub>IL</sub>

## READ MODE

The TMM27256AD has two control functions. The chip enable ( $\overline{\text{CE}}$ ) controls the operation power and should be used for device selection.

The output enable ( $\overline{\text{OE}}$ ) control the output buffers, independent of device selection.

Assuming that  $\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$ , the output data is valid at the outputs after address access time from

stabilizing of all addresses.

The  $\overline{\text{CE}}$  to output valid ( $t_{CE}$ ) is equal to the address access time ( $t_{ACC}$ ).

Assuming that  $\overline{\text{CE}} = V_{IL}$  and all addresses are valid, the output data is valid at the outputs after  $t_{OE}$  from the falling edge of  $\overline{\text{OE}}$ .

## OUTPUT DESELECT MODE

Assuming that  $\overline{\text{CE}} = V_{IH}$  or  $\overline{\text{OE}} = V_{IH}$ , the outputs will be in a high impedance state.

So two or more TMM27256AD's can be con-

nected together on a common bus line.

When  $\overline{\text{CE}}$  is decoded for device selection, all deselected devices are in low power standby mode.

## TMM27256AD-15, TMM27256AD-150 TMM27256AD-20, TMM27256AD-200

### STANDBY MODE

The TMM27256AD has a low power standby mode controlled by the  $\overline{CE}$  signal.

By applying a high level to the  $\overline{CE}$  input, the TMM27256AD is placed in standby mode which

reduces the operating current by 70%. The outputs are then in a high impedance state, independent of the  $\overline{OE}$  inputs.

### PROGRAM MODE

Initially, when received by customers, all bits of the TMM27256AD are in the "1" state which is the erased state.

The programming operation introduces "0s" data into the desired bit locations by electrical programming.

The TMM27256AD is in the programming mode when the V input is at 12.5V and  $\overline{CE}$  is at TTL-Low with  $\overline{OE}=V_{IH}$ .

The TMM27256AD can be programmed at any location, anytime — either individually, sequentially or at randomly.

### PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with  $\overline{OE}$  of  $V_{IL}$  and  $\overline{CE}$   $V_{IH}$  or  $V_{IL}$ .

### PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to  $V_{PP}$  terminal, a high level  $\overline{CE}$  input inhibits the TMM27256AD from being programmed.

Programming of two or more TMM27256ADs in parallel with different data is easily accomplished.

That is, all inputs except for  $\overline{CE}$  and  $\overline{OE}$  may be commonly connected, and a TTL low level program pulse is applied to the  $\overline{CE}$  of the desired device only and TTL high level signal is applied to the other devices.

### HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the  $V_{PP}$  terminal with  $V_{CC}=6V$ .

The programming is achieved by applying a single TTL low level 1ms pulse to the  $\overline{CE}$  input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

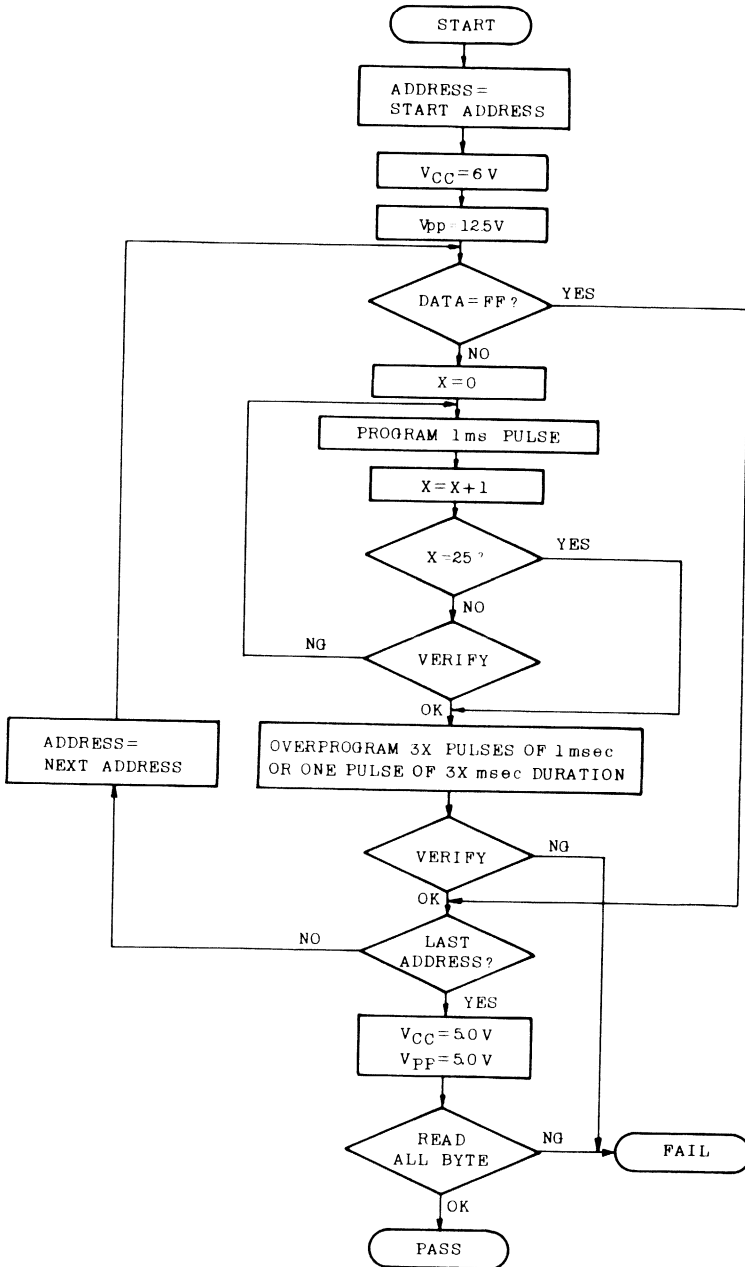
If the programmed data is not correct, another

program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width 3 times that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with  $V_{CC}=V_{PP}=5V$ .

HIGH SPEED PROGRAM MODE FLOW CHART



# TMM27256AD-15, TMM27256AD-150 TMM27256AD-20, TMM27256AD-200

## ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TMM27256AD which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from the TMM27256AD by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric signature mode is set up when 12V is

applied to address line A9 and the rest of address lines are set to  $V_{IL}$  in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to  $V_{IH}$ . These two code possess an odd parity with the parity bit of MSB (07).

The following table shows electric signature of the TMM27256AD.

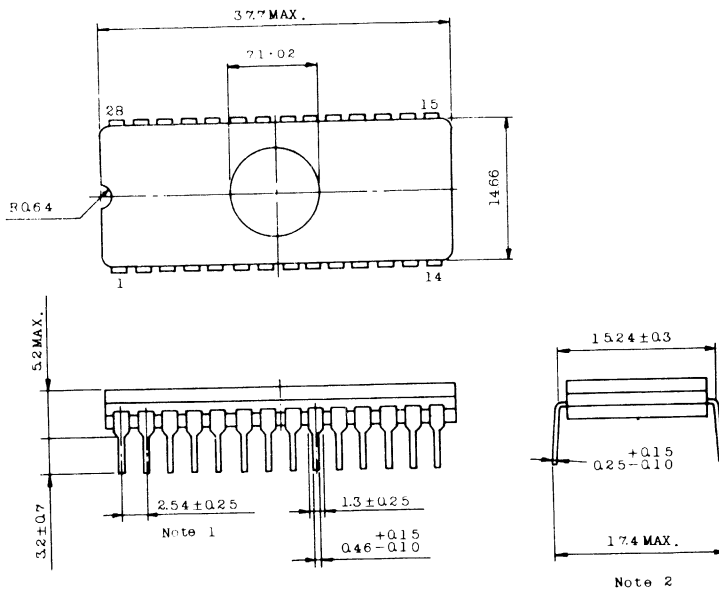
SIGNATURE	PINS	A <sub>0</sub> (10)	O <sub>7</sub> (19)	O <sub>6</sub> (18)	O <sub>5</sub> (17)	O <sub>4</sub> (16)	O <sub>3</sub> (15)	O <sub>2</sub> (13)	O <sub>1</sub> (12)	O <sub>0</sub> (11)	HEX. DATA
Manufacturer Code		$V_{IL}$	1	0	0	1	1	0	0	0	98
Device Code		$V_{IH}$	0	1	0	1	0	1	0	0	54

Notes : A<sub>9</sub> = 12V ± 0.5V

A<sub>1</sub>-A<sub>8</sub>, A<sub>10</sub>-A<sub>14</sub>,  $\overline{CE}$ ,  $\overline{OE}$  =  $V_{IL}$

## OUTLINE DRAWINGS

Unit in mm



- Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No. 1 and No.28 leads.  
2. This value is measured at the end of leads.  
3. All dimensions are in millimeters.

Note Toshiba does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry

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# TOSHIBA MOS MEMORY PRODUCT

32,768 WORD × 8 BIT N-MOS UV ERASABLE AND  
ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY  
SILICON STACKED GATE MOS

## TMM27256ADI-15 TMM27256ADI-20

### DESCRIPTION

The TMM27256ADI is a 32,768 word × 8 bit ultraviolet light erasable and electrically programmable read only memory.

For read operation, The TMM27256ADI's access time is 150ns/200ns, and the TMM27256ADI operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby

mode is achieved by applying a TTL-high level signal to the  $\overline{CE}$  input.

For program operation, the programming is achieved by using the high speed programming mode.

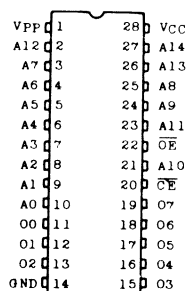
The TMM27256ADI is fabricated with the N-channel silicon double layer gate MOS technology.

### FEATURES

	-15	-20
V <sub>cc</sub>	5V ± 5%	
t <sub>acc</sub>	150ns	200ns
I <sub>cc2</sub>	100mA	
I <sub>cc1</sub>	30mA	

- Wide operating temperature range -40~85°C
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with i27256
- Standard 28 pin DIP cerdip package

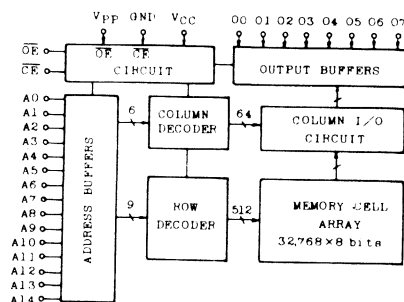
### PIN CONNECTION (TOP VIEW)



### PIN NAMES

A <sub>0</sub> ~A <sub>14</sub>	Address Inputs
O <sub>0</sub> ~O <sub>7</sub>	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V <sub>pp</sub>	Program Supply Voltage
V <sub>cc</sub>	V <sub>cc</sub> Supply Voltage (+5V)
GND	Ground

### BLOCK DIAGRAM



### MODE SELECTION

MODE	PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V <sub>pp</sub> (1)	V <sub>cc</sub> (28)	O <sub>0</sub> ~O <sub>7</sub> (11~13, 15~19)	POWER
Read		L	L	5V	5V	Data Out	Active
Output Deselect		*	H			High Impedance	
Standby		H	*			High Impedance	Standby
Program		L	H	12.5V	6V	Data In	Active
Program Inhibit		H	*			High Impedance	
Program Verify		*	L			Data Out	

Note \* : H or L

# TMM27256ADI-15

# TMM27256ADI-20

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	-0.6~7.0	V
V <sub>PP</sub>	Program Supply Voltage	-0.6~14.0	V
V <sub>IN</sub>	Input Voltage	-0.6~7.0	V
V <sub>IO</sub>	Input/Output Voltage	-0.6~7.0	V
P <sub>D</sub>	Power Dissipation	1.5	W
T <sub>SOLDER</sub>	Soldering Temperature · Time	260 · 10	°C·sec
T <sub>STG</sub>	Storage Temperature	-65~125	°C
T <sub>OPR</sub>	Operating Temperature	-40~85°C	°C

## READ OPERATION

### D. C. AND A. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27256ADI-15/20
T <sub>a</sub>	Operating Temperature	-40~85°C
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	5V±5%
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	2.2~V <sub>CC</sub> ±0.6V

### D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>LI</sub>	Input Current	V <sub>IN</sub> =0~V <sub>CC</sub>	—	—	±10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> =0.4~V <sub>CC</sub>	—	—	±10	μA
I <sub>CC1</sub>	Supply Current (Standby)	$\overline{CE} = V_{IH}$	—	—	35	mA
I <sub>CC2</sub>	Supply Current (Active)	$\overline{CE} = V_{IL}$	—	—	120	mA
V <sub>IH</sub>	Input High Voltage	—	2.2	—	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input Low Voltage	—	-0.3	—	0.8	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400μA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA	—	—	0.4	V
I <sub>PP1</sub>	V <sub>PP</sub> Current	V <sub>PP</sub> =0~V <sub>CC</sub> +0.6	—	—	±10	μA

### A. C. CHARACTERISTICS

(T<sub>a</sub> = -40~85°C, V<sub>CC</sub> = 5V±5%, V<sub>PP</sub> = 2.0V~V<sub>CC</sub>+0.6V)

SYMBOL	PARAMETER	TEST CONDITION	TMM27256AD-15		TMM27256AD-20		UNIT
			MIN.	MAX.	MIN.	MAX.	
t <sub>ACC</sub>	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	—	150	—	200	ns
t <sub>CE</sub>	$\overline{CE}$ to Output Valid	$\overline{OE} = V_{IL}$	—	150	—	200	ns
t <sub>OE</sub>	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IL}$	—	70	—	70	ns
t <sub>DF1</sub>	$\overline{CE}$ to Output in High-Z	$\overline{OE} = V_{IL}$	0	60	0	60	ns
t <sub>DF2</sub>	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	0	60	0	60	ns
t <sub>OH</sub>	Output Data Hold Time	$\overline{CE} = \overline{OE} = V_{IL}$	0	—	0	—	ns

A.C. Test Conditions

- Output Load : 1 TTL Gate and C<sub>L</sub> = 100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

# TMM27256ADI-15

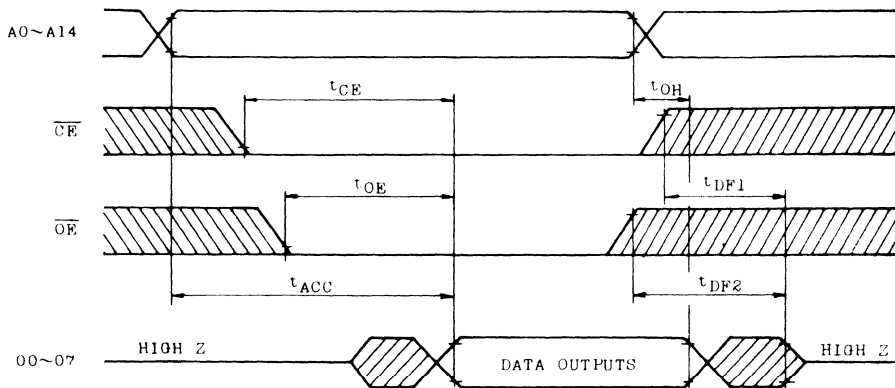
# TMM27256ADI-20

## CAPACITANCE \* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	—	4	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	—	8	12	pF

\* This parameter is periodically sampled and is not 100% tested.

## TIMING WAVEFORMS (READ)



## PROGRAM OPERATION

### D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>CC</sub> + 1.0	V
V <sub>IL</sub>	Input Low Voltage	-0.3	—	0.8	V
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	5.75	6.0	6.25	V
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	12.0	12.5	13.0	V

### D. C. and OPERATING CHARACTERISTICS (Ta = 25 ± 5°C, V<sub>CC</sub> = 6V ± 0.25V, V<sub>PP</sub> = 12.5V ± 0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>LI</sub>	Input Current	V <sub>IN</sub> = 0 ~ V <sub>CC</sub>	—	—	±10	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400 μA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA	—	—	0.4	V
I <sub>CC</sub>	V <sub>CC</sub> Supply Current	—	—	—	120	mA
I <sub>PP2</sub>	V <sub>PP</sub> Supply Current	V <sub>PP</sub> = 13.0V	—	—	50	mA

# TMM27256ADI-15

# TMM27256ADI-20

## A. C. PROGRAMMING CHARACTERISTICS ( $T_a = 25 \pm 5^\circ\text{C}$ , $V_{CC} = 6\text{V} \pm 0.25\text{V}$ , $V_{PP} = 12.5\text{V} \pm 0.5\text{V}$ )

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$t_{AS}$	Address Setup Time	—	2	—	—	$\mu\text{s}$
$t_{AH}$	Address Hold Time	—	2	—	—	$\mu\text{s}$
$t_{CES}$	$\overline{\text{CE}}$ Setup Time	—	0	—	—	ns
$t_{CEH}$	$\overline{\text{CE}}$ Hold Time	—	0	—	—	ns
$t_{OES}$	$\overline{\text{OE}}$ Setup Time	—	2	—	—	$\mu\text{s}$
$t_{DS}$	Data Setup Time	—	2	—	—	$\mu\text{s}$
$t_{DH}$	Data Hold Time	—	2	—	—	$\mu\text{s}$
$t_{VPS}$	$V_{PP}$ Setup Time	—	2	—	—	$\mu\text{s}$
$t_{VCS}$	$V_{CC}$ Setup Time	—	2	—	—	$\mu\text{s}$
$t_{PW}$	Initial Program Pulse Width	$\overline{\text{CE}} = V_{IL}$ , $\overline{\text{OE}} = V_{IH}$	0.95	1	1.05	ms
$t_{OPW}$	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
$t_{OF}$	$\overline{\text{OE}}$ to Output Valid	$\overline{\text{CE}} = V_{IH}$	—	—	150	ns
$t_{OFF}$	$\overline{\text{OE}}$ to Output in High-Z	$\overline{\text{CE}} = V_{IH}$	—	—	130	ns

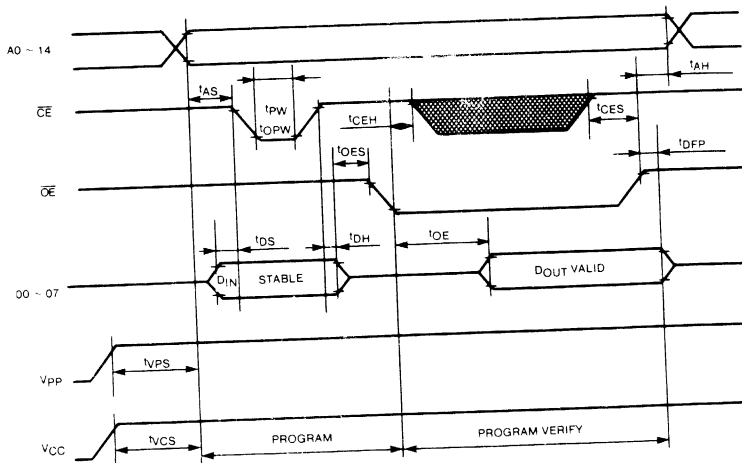
### A. C. Test Conditions

- Output Load : 1 TTL Gate and  $C_L$  (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note : 1. The length of the overprogram pulse may vary as a function of the counter value X.

## TIMING WAVEFORMS (PROGRAM)

( $V_{CC} = 6\text{V} \pm 0.25\text{V}$ ,  $V_{PP} = 12.5\text{V} \pm 0.5\text{V}$ )



- Note : 1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and cut off simultaneously or after  $V_{PP}$ .
2. Removing the device from socket and setting the device in socket with  $V_{PP} = 12.5\text{V}$  may cause permanent damage to the device.
3. The  $V_{PP}$  supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the  $V_{PP}$  terminal. When the switching pulse voltage is applied to the  $V_{PP}$  terminal, the overshoot voltage of its pulse should not be exceeded 14V

# TMM27256ADI-15 TMM27256ADI-20

## ERASURE CHARACTERISTICS

The TMM27256ADI's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) of the chip through the transparent window.

The integrated dose (ultraviolet light intensity [ $\mu\text{w}/\text{cm}^2$ ]  $\times$  exposure time [sec.]) for erasure should be a minimum of 15 [ $\mu\text{w} \cdot \text{sec}/\text{cm}^2$ ]

When the Toshiba GL-15 sterilizing lamp is used and the device is exposed at a distance of 1 cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps with an ultraviolet light intensity of 12000 [ $\mu\text{w}/\text{cm}^2$ ] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [ $\mu\text{w}/\text{cm}^2$ ]  $\times$  (20 $\times$ 60) [sec]  $\cong$  15 [ $\mu\text{w} \cdot \text{sec}/\text{cm}^2$ ].)

The TMM27256ADI's erasure begins to occur when exposed to light with wavelengths shorter than 4000Å. Both Sunlight and fluorescent lamps include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

## OPERATION INFORMATION

The TMM27256ADI's six operation modes are listed in the following table. Mode selection can be

achieved by applying TTL level signal to all inputs.

MODE	PIN NAMES(NUMBER)	$\overline{\text{CE}}$ (20)	$\overline{\text{OE}}$ (22)	$V_{\text{PP}}$ (1)	$V_{\text{CC}}$ (28)	$O_0 \sim O_7$ (11 ~ 13, 15 ~ 19)	POWER
Read Operation ( $T_a = -40 \sim 85 \text{ C}$ )	Read	L	L	5 V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	Active
	Standby	H	*			High Impedance	Standby
Program Operation ( $T_a = 25 \pm 5 \text{ C}$ )	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	*			High Impedance	Active
	Program Verify	*	L			Data Out	Active

Note H :  $V_{\text{IH}}$ , L :  $V_{\text{IL}}$ , \* :  $V_{\text{IH}}$  or  $V_{\text{IL}}$

## READ MODE

The TMM27256ADI has two control functions.

The chip enable ( $\overline{\text{CE}}$ ) controls the operation power and should be used for device selection.

The output enable ( $\overline{\text{OE}}$ ) controls the output buffers, independent of device selection.

Assuming that  $\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}$ , the output data is valid at the outputs after the address access time from

stabilizing of all addresses.

The  $\overline{\text{CE}}$  to output valid ( $t_{\text{CE}}$ ) time is equal to the address access time ( $t_{\text{ACC}}$ ).

Assuming that  $\overline{\text{CE}} = V_{\text{IL}}$  and all addresses are valid, the output data is valid at the outputs after  $t_{\text{OE}}$  from the falling edge of  $\overline{\text{CE}}$ .

## OUTPUT DESELECT MODE

With  $\overline{\text{CE}} = V_{\text{IH}}$  or  $\overline{\text{OE}} = V_{\text{IH}}$ , outputs will be in high impedance state.

Therefore two or more TMM27256ADI's can be con-

nected together on a common bus line.

When  $\overline{\text{CE}}$  is decoded for device selection, all deselected devices are in low power standby mode.

# TMM27256ADI-15

# TMM27256ADI-20

## STANDBY MODE

The TMM27256ADI has a low power standby mode controlled by the  $\overline{CE}$  signal.

By applying a high level to the  $\overline{CE}$  input, the TMM27256ADI is placed in the standby mode which

## PROGRAM MODE

Initially, when received by customers, all bits of the TMM27256ADI are in the "1" state which is the erased state.

The programming operation introduces "0s" data into the desired bit locations by electrical programming.

## PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

## PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to  $V_{PP}$  terminal, a high level  $\overline{CE}$  input inhibits the TMM27256ADI from being programmed.

Programming of two or more TMM27256ADI's in parallel with different data is easily accomplished.

## HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the  $V_{PP}$  terminal with  $V_{CC}=6V$ .

The programming is achieved by applying a single TTL low level 1ms pulse to the  $\overline{CE}$  input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another

reduces 70% of operating current by applying TTL-high level ( $V_{CC}$ ). The outputs are in a high impedance state, independent of the  $\overline{OE}$  inputs.

The TMM27256ADI is in the programming mode when the  $V_{PP}$  input is at 12.5V and  $\overline{CE}$  is at TTL-Low under  $\overline{OE}=V_{IH}$ .

The TMM27256ADI can be programmed at any location, anytime — either individually, sequentially or at random.

The verify is accomplished with  $\overline{OE}$  of  $V_{IL}$  and  $\overline{CE}$  of  $V_{IH}$  or  $V_{IL}$ .

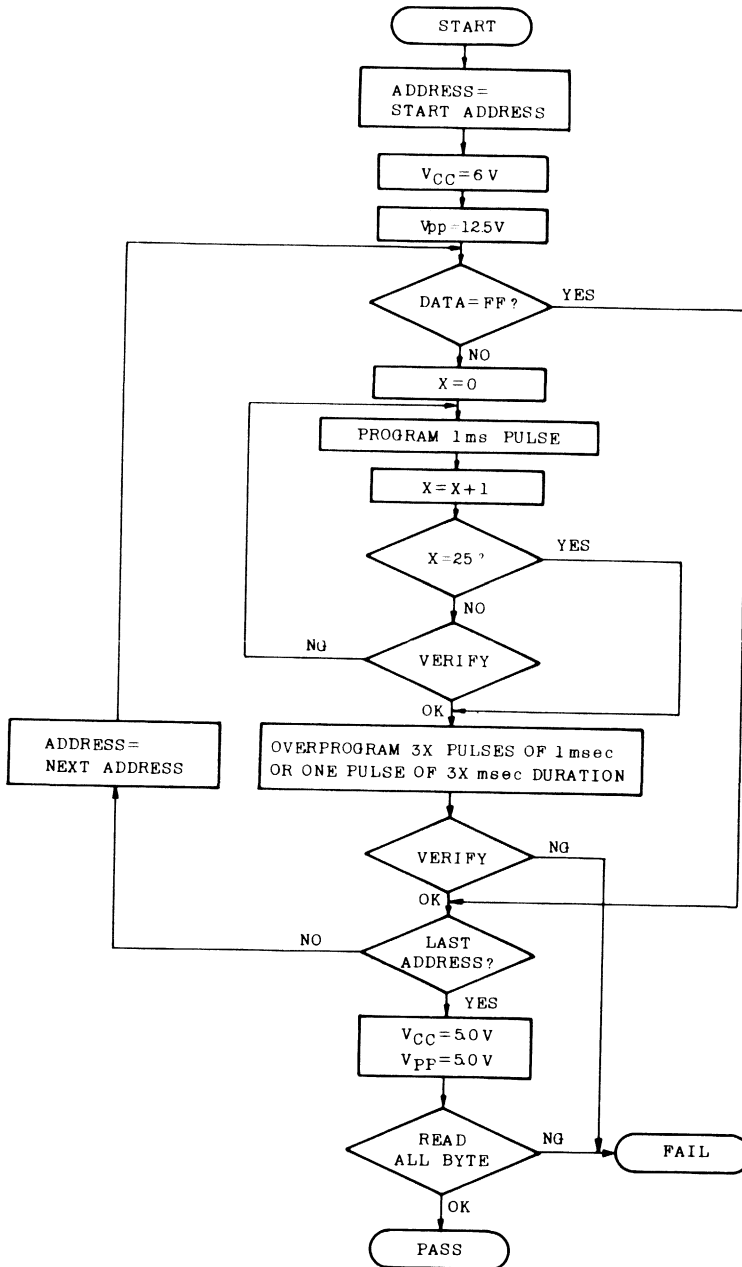
That is, all inputs except for  $\overline{CE}$  and  $\overline{OE}$  may be commonly connected, and a TTL low level program pulse is applied to the  $\overline{CE}$  of the desired device only and TTL high level signal is applied to the other devices.

program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width 3 times that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with  $V_{CC}=V_{PP}=5V$ .

**HIGH SPEED PROGRAM MODE FLOW CHART**



# TMM27256ADI-15

# TMM27256ADI-20

## ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TMM27256ADI which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from the TMM27256ADI by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric signature mode is set up when 12V is

applied to address line A9 and the rest of address lines are set to V<sub>IL</sub> in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V<sub>IH</sub>. These two code possess an odd parity with the parity bit of MSB (07).

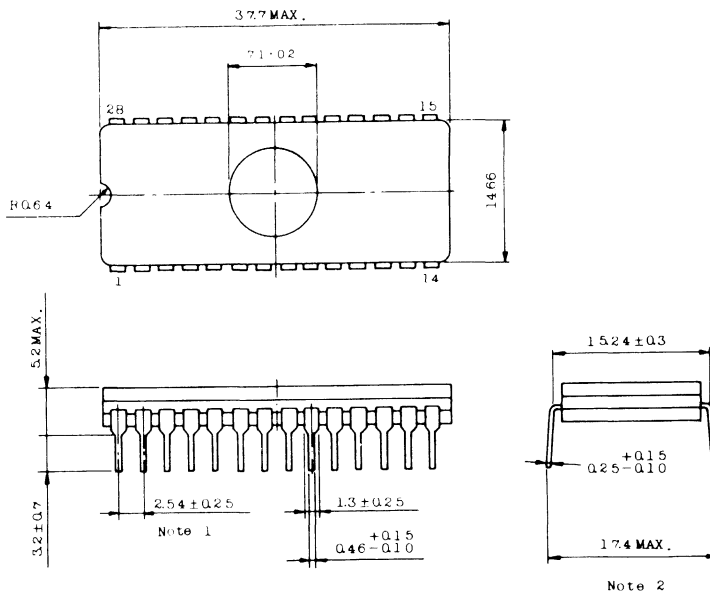
The following table shows electric signature of the TMM27256ADI.

SIGNATURE	PINS	A <sub>0</sub> (10)	O <sub>7</sub> (19)	O <sub>6</sub> (18)	O <sub>5</sub> (17)	O <sub>4</sub> (16)	O <sub>3</sub> (15)	O <sub>2</sub> (13)	O <sub>1</sub> (12)	O <sub>0</sub> (11)	HEX. DATA
Manufacture Code	V <sub>IL</sub>	1	0	0	1	1	0	0	0	0	98
Device Code	V <sub>IH</sub>	0	1	0	1	0	1	0	0	0	54

Notes : A<sub>9</sub> = 12V ± 0.5V  
A<sub>1</sub>-A<sub>8</sub>, A<sub>10</sub>-A<sub>14</sub>,  $\overline{CE}$ ,  $\overline{OE}$  = V<sub>IL</sub>

## OUTLINE DRAWINGS

Unit in mm



- Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No. 1 and No. 28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

Note Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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# TOSHIBA MOS MEMORY PRODUCT

32,768 WORD X 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

## TC57256D-20 TC57256D-25

SILICON STACKED GATE MOS

### DESCRIPTION

The TC57256D is a 32,768 word X8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC57256D's access time is 200ns, and the TC57256D operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the  $\overline{CE}$  input. Advanced CMOS technology reduces the maximum active current to 30 mA/5MHz

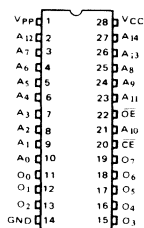
and standby current to 100 $\mu$ A.

For program operation, the programming is achieved by using the high speed programming mode. Program supply voltage is 21V. The programming of the TC57256D is accomplished within one and a half minutes (typ.) TC57256D is fabricated using CMOS technology and N-channel silicon double layer gate MOS technology.

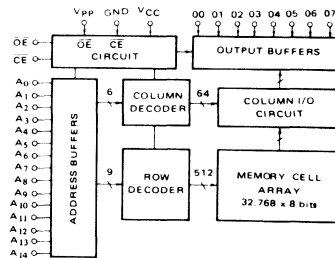
### FEATURES

- Peripheral circuit: CMOS  
Memory cell : N-MOS
- Low power dissipation  
30mA/5MHZ (active)  
100 $\mu$ A (standby)
- Fast access time TC57256D-20 200 ns  
TC57256D-25 250 ns
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROMS TC53257P, TMM23256P and EPROM i27256
- Standard 28 pin DIP cerdip Package

### PIN CONNECTION (TOP VIEW)



### BLOCK DIAGRAM



### PIN NAMES

A <sub>0</sub> ~ A <sub>14</sub>	Address Inputs
O <sub>0</sub> ~ O <sub>7</sub>	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V <sub>PP</sub>	Program Supply Voltage
V <sub>CC</sub>	V <sub>CC</sub> Supply Voltage (+5V)
GND	Ground

### MODE SELECTION

MODE	PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V <sub>PP</sub> (1)	V <sub>CC</sub> (28)	O <sub>0</sub> ~ O <sub>7</sub> (11 ~ 13, 15 ~ 19)	POWER	
Read		L	L	5V	5V	Data Out	Active	
Output Deselect	*	H	5V		5V	High Impedance		
Standby	H	*	5V		5V	High Impedance		
Program		L	H	21V	6V	Data In	Active	
Program Inhibit	H	*	21V			6V		High Impedance
Program Verify	L	L	21V			6V		Data Out

\* \* : H or L

# TC57256D-20

# TC57256D-25

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	-0.6 ~ 7.0	V
V <sub>PP</sub>	Program Supply Voltage	-0.6 ~ 22.0	V
V <sub>IN</sub>	Input Voltage	-0.6 ~ 7.0	V
V <sub>I/O</sub>	Input/Output Voltage	-0.6 ~ V <sub>CC</sub> + 0.5	V
P <sub>D</sub>	Power Dissipation	1.5	W
T <sub>SOLDER</sub>	Soldering Temperature Time	260 · 10	°C · sec
T <sub>STRG</sub>	Storage Temperature	-65 ~ 125	°C
T <sub>OPR</sub>	Operating Temperature	-40 ~ 85	°C

## READ OPERATION

### D.C. RECOMMENDED OPERATING CONDITONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	—	0.8	V
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	4.75	5.00	5.25	V
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	2.0	V <sub>CC</sub>	V <sub>CC</sub> + 0.3	V

### D.C. and OPERATING CHARACTERISTICS (T<sub>a</sub> = -40 ~ 85°C, V<sub>CC</sub> = 5V ± 5%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>LI</sub>	Input current	V <sub>IN</sub> = 0 ~ V <sub>CC</sub>	—	—	± 10	μA
I <sub>CC01</sub>	Operating Current	$\overline{CE} = 0$	f = 5MHz	—	30	mA
I <sub>CC02</sub>			f = 1MHz	—	10	mA
I <sub>CCS1</sub>	Standby Current	$\overline{CE} = V_{IH}$	—	—	1	mA
I <sub>CCS2</sub>		$\overline{CE} = V_{CC} - 0.2V$	—	—	100	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400μA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA	—	—	0.4	V
I <sub>PP1</sub>	V <sub>PP</sub> Current	V <sub>PP</sub> = 0 ~ V <sub>CC</sub> + 0.3V	—	—	± 10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0.4V ~ V <sub>CC</sub>	—	—	± 10	μA

### A.C. CHARACTERISTICS (T<sub>a</sub> = -40 ~ 85°C, V<sub>CC</sub> = 5V ± 5%, V<sub>PP</sub> = 2.0V ~ V<sub>CC</sub> + 0.3V)

SYMBOL	PARAMETER	TEST CONDITION	TC57256D-20		TC57256D-25		UNIT
			MIN.	MAX.	MIN.	MAX.	
t <sub>ACC</sub>	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	—	200	—	250	ns
t <sub>CE</sub>	$\overline{CE}$ to Output Valid	$\overline{OE} = V_{IL}$	—	200	—	250	ns
t <sub>OE</sub>	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IL}$	—	70	—	100	ns
t <sub>DF1</sub>	$\overline{CE}$ to Output in High-Z	$\overline{OE} = V_{IL}$	0	60	0	90	ns
t <sub>DF2</sub>	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	0	60	0	90	ns
t <sub>OH</sub>	Output Data Hold Time	$\overline{CE} = \overline{OE} = V_{IL}$	0	—	0	—	ns

### A.C. TEST CONDITONS

Output Load	: 1 TTL Gate and C <sub>L</sub> = 100pF
Input Pulse Rise and Fall Times	: 10 ns Max.
Input Pulse Levels	: 0.45 ~ 2.4V
Timing Mesurement Reference Level	: Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

# TC57256D-20

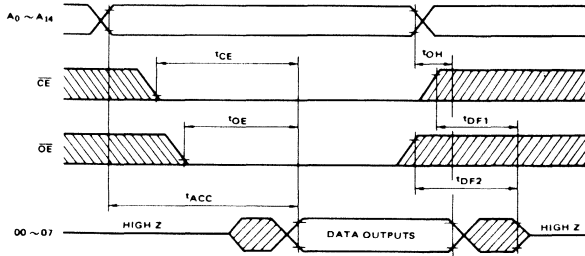
# TC57256D-25

## CAPACITANCE \*(Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	—	4	6	μF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	—	8	12	μF

\*This parameter is periodically sampled and is not 100% tested.

## TIMING WAVEFORMS (READ)



## PROGRAM OPERATION

### D.C. RECOMMENDED OPERATING CONDITONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	—	0.8	V
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	5.75	6.0	6.25	V
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	20.5	21.0	21.5	V

### D.C. and OPERATING CHARACTERISTICS (Ta = 25 ± 5°C, V<sub>CC</sub> = 6V ± 0.25V, V<sub>PP</sub> = 21V ± 0.5)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>LI</sub>	Input Current	V <sub>IN</sub> = 0 ~ V <sub>CC</sub>	—	—	±10	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400μA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA	—	—	0.4	V
I <sub>CC</sub>	V <sub>CC</sub> Supply Current	—	—	—	30	mA
I <sub>PP2</sub>	V <sub>PP</sub> Supply Current	V <sub>PP</sub> = 21.5V	—	—	30	mA

### A.C. PROGRAMMING CHARACTERISTICS (Ta = 25 ± 5°C, V<sub>CC</sub> = 6V ± 0.25V, V<sub>PP</sub> = 21V ± 0.5)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t <sub>AS</sub>	Address Setup Time	—	2	—	—	μs
t <sub>AH</sub>	Address Hold Time	—	2	—	—	μs
t <sub>CES</sub>	CE Setup Time	—	2	—	—	μs
t <sub>CEH</sub>	CE Hold Time	—	2	—	—	μs
t <sub>OES</sub>	OE Setup Time	—	2	—	—	μs
t <sub>OEH</sub>	OE Hold Time	—	2	—	—	μs
t <sub>DS</sub>	Data Setup Time	—	2	—	—	μs
t <sub>DH</sub>	Data Hold Time	—	2	—	—	μs
t <sub>VS</sub>	V <sub>PP</sub> Setup Time	—	2	—	—	μs
t <sub>PW</sub>	Initial Program Pulse Width	CE = V <sub>IL</sub> , OE = V <sub>IH</sub>	0.95	1	1.05	ms
t <sub>OPW</sub>	Overprogram Pulse Width	Note 1	0.95	1	21	ms
t <sub>DV</sub>	CE to Output Valid	OE = V <sub>IL</sub>	—	—	1	μs
t <sub>DF1</sub>	CE to Output in High-Z	OE = V <sub>IL</sub>	—	—	150	ns

# TC57256D-20

# TC57256D-25

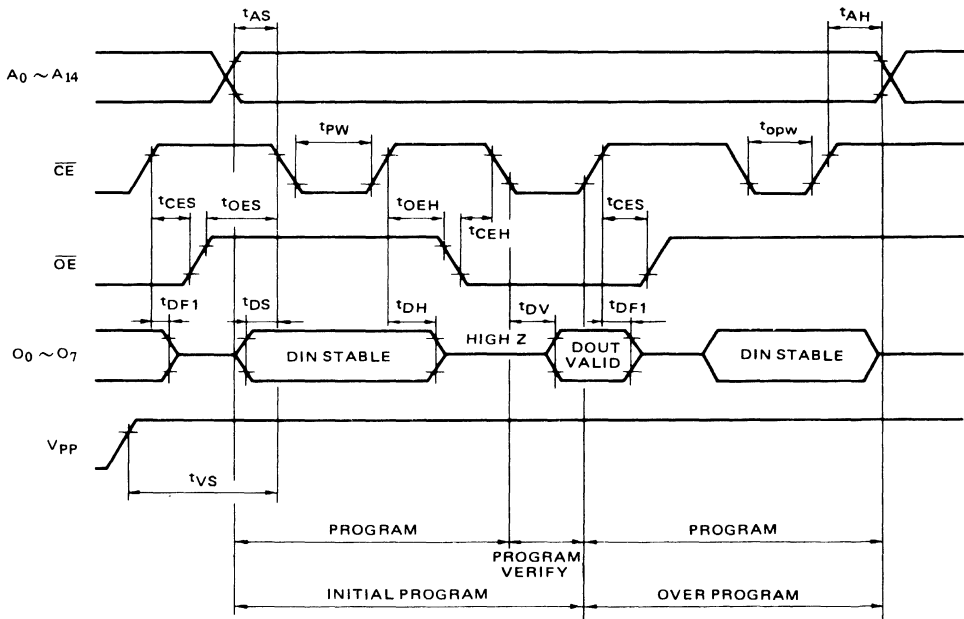
## A.C. TEST CONDITIONS

Output Load : 1 TTL Gate and  $C_L$  (100pF)  
 Input Pulse Rise and Fall Times : 10 ns Max.  
 Input Pulse Levels : 0.45 ~ 2.4V  
 Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as function of the counter value X.

## TIMING WAVEFORMS (PROGRAM)

( $V_{CC} = 6V \pm 0.25V$ ,  $V_{PP} = 21V \pm 0.5V$ )



- Note: (1)  $V_{CC}$  must be applied simultaneously with or before  $V_{PP}$  and cut off simultaneously with or after  $V_{PP}$ .  
 (2) Removing the device from socket and setting the device in socket with  $V_{PP}=21V$  may cause permanent damage to the device.  
 (3) The  $V_{PP}$  supply voltage is permitted up to 22V for program operation; voltages over 22V should not be applied to the  $V_{PP}$  terminal. When the switching pulse voltage is applied to the  $V_{PP}$  terminal, the overshoot voltage of its pulse should not exceed 22V.

# TC57256D-20

# TC57256D-25

## ERASURE CHARACTERISTICS

The TC57256D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) through the chips transparent window.

The integrated dose (ultraviolet light intensity [ $w/cm^2$ ]  $\times$  exposure time [sec.]) for erasure should be a minimum of 15 [ $w \cdot sec/cm^2$ ].

When the Toshiba GL-15 sterilizing lamp is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps with an ultraviolet light intensity of 12000 [ $\mu w/cm^2$ ] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [ $\mu w/cm^2$ ]  $\times$  (20 $\times$ 60) [sec]  $\cong$  15 [ $w \cdot sec/cm^2$ ].)

The TC57256D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. Both sunlight and fluorescent lamps include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

## OPERATION INFORMATION

The TC57256D's six operation modes are listed in the following table. Mode selection can be achieved

by applying TTL level signal to all inputs.

MODE	PIN NAMES (NUMBER)	$\overline{CE}$	$\overline{OE}$	$V_{PP}$ (1)	$V_{CC}$ (28)	$O_0 \sim O_7$ (11 ~ 13, 15 ~ 19)	POWER
		(20)	(22)				
Read Operation ( $T_a = -40 \sim 85^\circ C$ )	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	Active
	Standby	H	*			High Impedance	Standby
Program Operation ( $T_a = 25 \pm 5^\circ C$ )	Program	L	H	21V	6V	Data In	Active
	Program Inhibit	H	*			High Impedance	Active
	Program Verify	L	L			Data Out	Active

Note: H:  $V_{IH}$ , L:  $V_{IL}$ , \*:  $V_{IH}$  or  $V_{IL}$

## READ MODE

The TC57256D has two control functions. The chip enable ( $\overline{CE}$ ) controls the operation power and should be used for device selection.

The output enable ( $\overline{OE}$ ) controls the output buffers, independent of device selection.

Assuming that  $\overline{CE} = \overline{OE} = V_{IL}$ , the output data is valid

at the outputs after the address access time from stabilizing of all addresses.

The  $\overline{CE}$  to output valid ( $t_{CE}$ ) time is equal to the address access time ( $t_{ACC}$ ).

Assuming that  $\overline{CE} = V_{IL}$  and all addresses are valid, the output data is valid at the outputs after  $t_{OE}$  from the falling edge of  $\overline{CE}$ .

# TC57256D-20

# TC57256D-25

## OUTPUT DESELECT MODE

With  $\overline{CE}=V_{IH}$  or  $\overline{OE}=V_{IH}$ , the outputs will be in high impedance state.

Therefore two or more TC57256D's can be connected

together on a common bus line.

When  $\overline{CE}$  is decoded for device selection, all deselected devices are in low power standby mode.

## STANDBY MODE

The TC57256D has a low power standby mode controlled by the  $\overline{CE}$  signal.

By applying a high level to the  $\overline{CE}$  input, the TC57256D is placed in the standby mode which

reduces the operating current to  $100\mu A$ . The outputs will be in a high impedance state, independent of the  $\overline{OE}$  inputs.

## PROGRAM MODE

Initially, when received by customers, all bits of the TC57256D are in the "1" state which is the erased state.

The programming operation introduces "0s" data into the desired bit locations by electrical programming.

The TC57256D is in the programming mode when the  $V_{PP}$  input is at 21V and  $\overline{CE}$  is at TTL-Low  $\overline{OE}=V_{IH}$ .

The TC57256D can be programmed at any location, anytime — either individually, sequentially or at randomly.

## PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with  $\overline{OE}$  and  $\overline{CE}$  at  $V_{IL}$ .

## PROGRAM INHIBIT MODE

Under the condition that the program voltage (+21V) is applied to  $V_{PP}$  terminal, a high level  $\overline{CE}$  input inhibits the TC57256D from being programmed.

Programming two or more TC57256D's in parallel with different data is easily accomplished: All inputs

except for  $\overline{CE}$  may be commonly connected, a TTL low level program pulse is applied to the  $\overline{CE}$  of the desired device only, and TTL high level signal is applied to the other devices.

## HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using a high speed programming mode. The device is set up in the high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+21V) is applied to the  $V_{PP}$  terminal with  $V_{CC}=6V$ .

Programming is achieved by applying a single TTL low level 1ms pulse to the  $\overline{CE}$  input after addresses and data are stable. Then the programmed data is verified in the Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and the programmed

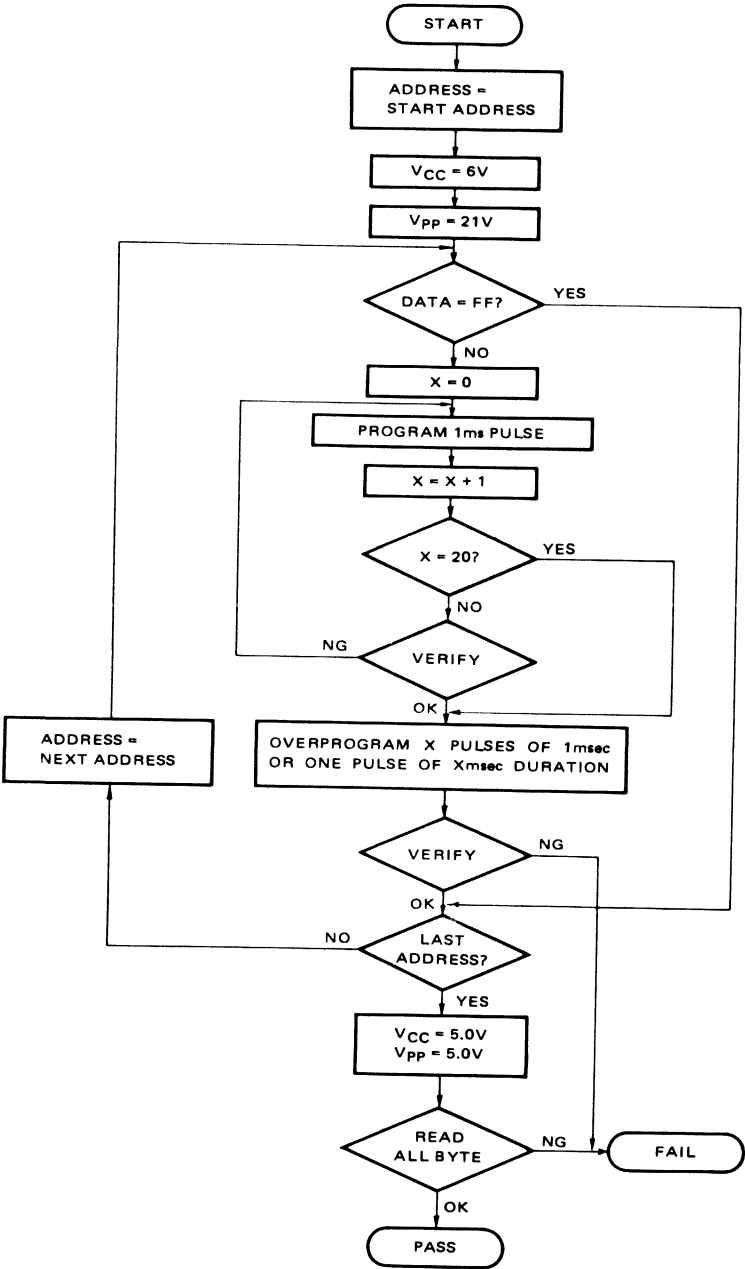
data is verified. This should be repeated until the program operates correctly (max. 20 times).

After correctly programming the selected address, an additional program pulse with a width equal to that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with  $V_{CC}=V_{PP}=5V$ .

This high speed program algorithm allows the programming of the TC57256D to be accomplished within one and a half minutes (typ.)

**HIGH SPEED PROGRAM MODE FLOW CHART**



# TC57256D-20

# TC57256D-25

## ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TC57256D which identifies its manufacture and device type.

The programming equipment may be used to read the manufacturer code and device code from the TC57256D by using this mode before program operation and automatically set program voltage ( $V_{pp}$ ) and algorithm.

Electric Signature mode is set up when 12V is applied to

address line  $A_9$  and the rest of address lines are set to  $V_{IL}$  in read operation. Data output under these conditions is the manufacturer code. Device code is identified when address  $A_0$  is set to  $V_{IH}$ . These two codes possess an odd parity with the parity bit of MSB (07).

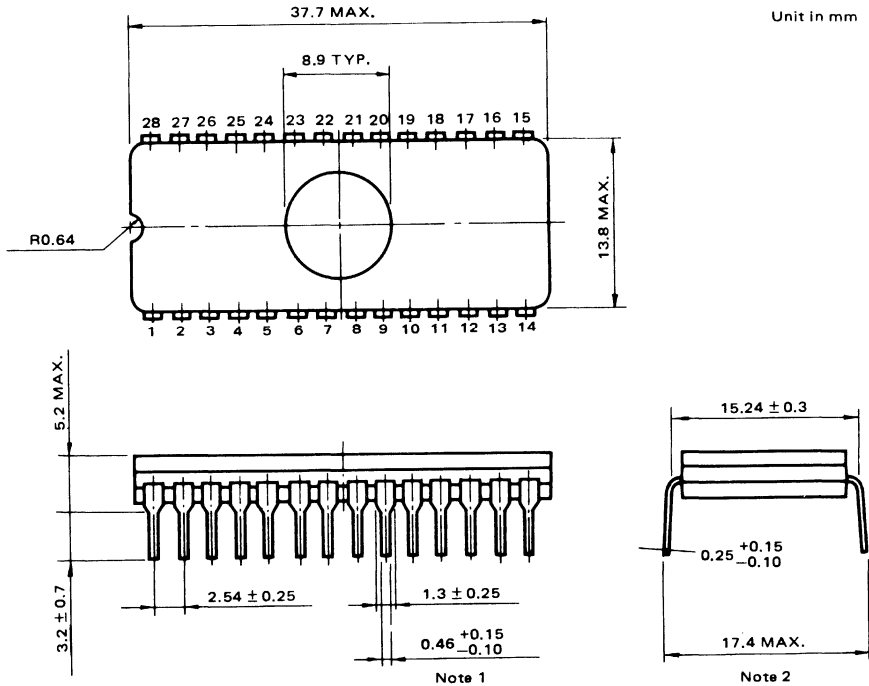
The following table shows electric signature of TC57256D.

SIGNATURE	PINS	$A_9$ (10)	$O_7$ (19)	$O_6$ (18)	$O_5$ (17)	$O_4$ (16)	$O_3$ (15)	$O_2$ (13)	$O_1$ (12)	$O_0$ (11)	HEX. DATA
Manufacturer Code	$V_{IL}$	1	0	0	1	1	0	0	0	0	98
Device Code	$V_{IH}$	0	0	0	0	0	1	0	0	0	04

Notes:  $A_9 = 12V \pm 0.5V$

$A_1 - A_8, A_{10} - A_{14}, \overline{CE}, \overline{OE} = V_{IL}$

## OUTLINE DRAWINGS



- Note: (1) Each lead pitch 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.  
 (2) This value is measured at the end of leads.  
 (3) The dimensions are in millimeters.



# TOSHIBA MOS MEMORY PRODUCT

**TC57256AD-15**  
**TC57256AD-20**

## DESCRIPTION

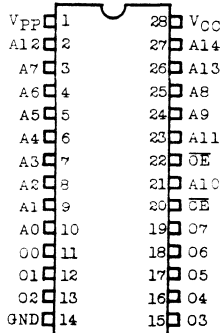
The TC57256AD is a 32,768 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC57256AD's access time is 150ns. The TC57256AD operates from a single 5-volt power supply and has a low power standby mode which reduces power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the  $\overline{CE}$  input. Advanced CMOS technology reduces the maximum active current to 40mA/6.7MHz and the standby current to 100 $\mu$ A. For program operation, the programming is achieved by using the high speed programming mode. The TC57256AD is fabricated using CMOS technology and N-channel silicon double layer gate MOS technology.

## FEATURES

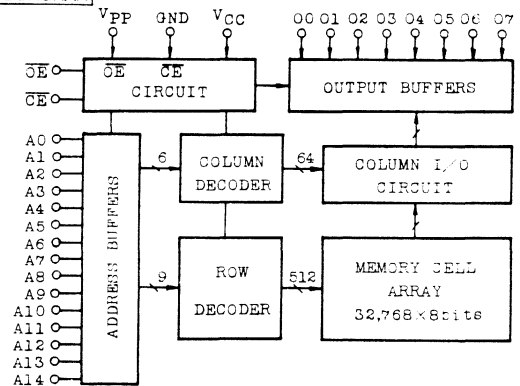
- Peripheral circuit: CMOS  
Memory cell : N-MOS
- Low power dissipation  
Active : 40mA/6.7MHz  
Standby: 100 $\mu$ A
- Fast access time:  
TC57256AD-15 150ns  
TC57256AD-20 200ns
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROMs TC53257P and TMM23256P, TMM27256AD and TC57256AD
- Standard 28 pin DIP cerdip package

## PIN CONNECTION

(TOP VIEW)



## BLOCK DIAGRAM



## PIN NAMES

A0 ~ A14	Address Inputs
00 ~ 07	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V <sub>PP</sub>	Program Supply Voltage
V <sub>CC</sub>	V <sub>CC</sub> Supply Voltage (+5V)
GND	Ground

## MODE SELECTION

MODE	P.L.		V <sub>PP</sub> (1)	V <sub>CC</sub> (28)	00~07 (11 ~ 13, 15 ~ 19)	POWER
	$\overline{CE}$ (20)	$\overline{OE}$ (22)				
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	
Program	L	H	12.5V	6V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

\* H or L

# TC57256AD-15

# TC57256AD-20

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	VCC Power Supply Voltage	-0.6 ~ 7.0	V
V <sub>PP</sub>	Program Supply Voltage	-0.6 ~ 14.0	V
V <sub>IN</sub>	Input Voltage	-0.6 ~ 7.0	V
V <sub>I/O</sub>	Input/Output Voltage	-0.6 ~ V <sub>CC</sub> +0.5	V
P <sub>D</sub>	Power Dissipation	1.5	W
T <sub>SOLDER</sub>	Soldering Temperature Time	260 · 10	°C · sec
T <sub>STRG</sub>	Storage Temperature	-65 ~ 125	°C
T <sub>OPR</sub>	Operating Temperature	-40 ~ 85	°C

## READ OPERATION

### D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	-	0.8	
V <sub>CC</sub>	VCC Power Supply Voltage	4.75	5.00	5.25	
V <sub>PP</sub>	Vpp Power Supply Voltage	V <sub>CC</sub> -0.6	V <sub>CC</sub>	V <sub>CC</sub> +0.6	

### D.C. and OPERATING CHARACTERISTICS (T<sub>a</sub>=-40 ~ 85°C, V<sub>CC</sub>=5V ± 5%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I <sub>LI</sub>	Input Current	V <sub>IN</sub> =0V ~ V <sub>CC</sub>	-	-	±10	μA	
I <sub>CC01</sub>	Operating Current	$\overline{CE}$ =0V	f=6.7MHz	-	-	40	mA
I <sub>CC02</sub>		I <sub>OUT</sub> =0mA	f=1MHz	-	-	10	
I <sub>CCS1</sub>	Standby Current	$\overline{CE}$ =V <sub>IH</sub>	-	-	1	mA	
I <sub>CCS2</sub>		$\overline{CE}$ =V <sub>CC</sub> -0.2V	-	-	100	μA	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> =-400μA	2.4	-	-	V	
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> =2.1mA	-	-	0.4	V	
I <sub>PP1</sub>	V <sub>CC</sub> Current	V <sub>PP</sub> =V <sub>CC</sub> ± 0.6V	-	-	±10	μA	
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> =0.4V ~ V <sub>CC</sub>	-	-	±10	μA	

# TC57256AD-15

# TC57256AD-20

A.C. CHARACTERISTICS (Ta=-40 ~ 85°C, VCC=5V±5%, VPP=VCC±0.6V)

SYMBOL	PARAMETER	TEST CONDITION	TC57256AD-15		TC57256AD-20		UNIT
			MIN.	MAX.	MIN.	MAX.	
t <sub>ACC</sub>	Address Access Time	$\overline{CE}=\overline{OE}=V_{IL}$	-	150	-	200	ns
t <sub>CE</sub>	$\overline{CE}$ to Output Valid	$\overline{OE}=V_{IL}$	-	150	-	200	
t <sub>OE</sub>	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IL}$	-	70	-	70	
t <sub>DF1</sub>	$\overline{CE}$ to Output in High-Z	$\overline{OE}=V_{IL}$	0	60	0	60	
t <sub>DF2</sub>	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	0	60	0	60	
t <sub>OH</sub>	Output Data Hold Time	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	0	-	

## A.C. TEST CONDITIONS

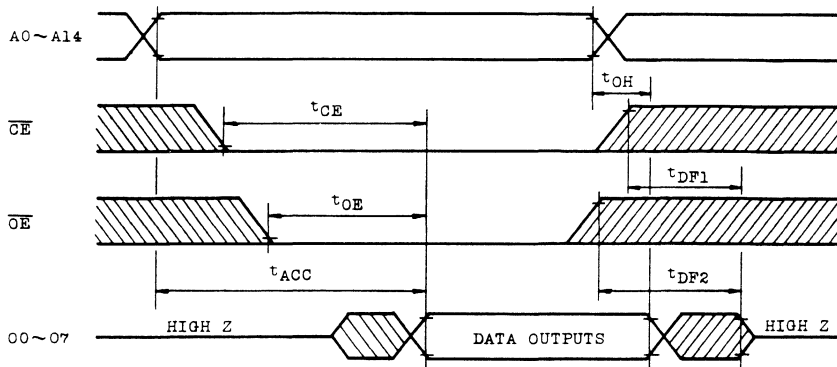
- Output Load : 1 TTL Gate and C<sub>L</sub>=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE \*(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =0V	-	4	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> =0V	-	8	12	

\* This parameter is periodically sampled and is not 100% tested.

## TIMING WAVEFORMS



# TC57256AD-15

# TC57256AD-20

## PROGRAM OPERATION

### D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input Low Voltage	-0.3	-	0.8	
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	5.75	6.0	6.25	
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	12.0	12.5	13.0	

### D.C. and OPERATING CHARACTERISTICS (T<sub>a</sub>=25 ± 5°C, V<sub>CC</sub>=6V ± 0.25V, V<sub>PP</sub>=12.5V ± 0.5V)

SYMBOL	PARAMETER	TESTCONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>LI</sub>	Input Current	V <sub>IN</sub> =0 ~ V <sub>CC</sub>	-	-	±10	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> =-400μA	2.4	-	-	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> =2.1mA	-	-	0.4	V
I <sub>CC</sub>	V <sub>CC</sub> Supply Current	-	-	-	40	mA
I <sub>PP2</sub>	V <sub>PP</sub> Supply Current	V <sub>PP</sub> =13.0V	-	-	50	mA
V <sub>ID</sub>	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

### A.C. PROGRAMMING CHARACTERISTICS (T<sub>a</sub>=25 ± 5°C, V<sub>CC</sub>=6V ± 0.25V, V<sub>PP</sub>=12.5V ± 0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t <sub>AS</sub>	Address Setup Time	-	2	-	-	μs
t <sub>AH</sub>	Address Hold Time	-	2	-	-	μs
t <sub>CES</sub>	$\overline{CE}$ Setup Time	-	0	-	-	ns
t <sub>CEH</sub>	$\overline{CE}$ Hold Time	-	0	-	-	ns
t <sub>OES</sub>	$\overline{OE}$ Setup Time	-	2	-	-	μs
t <sub>DS</sub>	Data Setup Time	-	2	-	-	μs
t <sub>DH</sub>	Data Hold Time	-	2	-	-	μs
t <sub>VPS</sub>	V <sub>PP</sub> Setup Time	-	2	-	-	μs
t <sub>VCS</sub>	V <sub>CC</sub> Setup Time	-	2	-	-	μs
t <sub>PW</sub>	Initial Program Pulse Width	$\overline{CE}=V_{IL}$ , $\overline{OE}=V_{IH}$	0.95	1	1.05	ms
t <sub>OPW</sub>	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t <sub>OE</sub>	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	-	-	150	ns
t <sub>DFP</sub>	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	-	-	130	ns

### A.C. TEST CONDITIONS

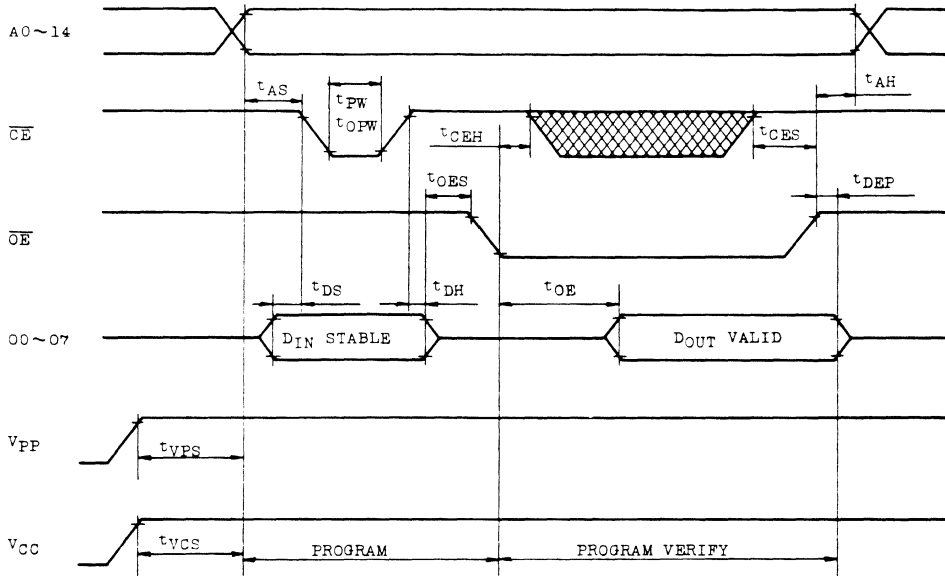
- Output Load : 1 TTL Gate and C<sub>L</sub> (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

# TC57256AD-15 TC57256AD-20

## TIMING WAVEFORMS (PROGRAM)

( $V_{CC}=6V\pm 0.25V$ ,  $V_{PP}=12.5V\pm 0.5V$ )



Note: (1)  $V_{CC}$  must be applied simultaneously with or before  $V_{PP}$  and cut off simultaneously with or after  $V_{PP}$ .

(2) Removing the device from the socket or placing the device in the socket with  $V_{PP}=12.5V$  may cause permanent damage to the device.

(3) The  $V_{PP}$  supply voltage is permitted up to 14V for program operation; voltages over 14V should not be applied to the  $V_{PP}$  terminal. When a switching pulse voltage is applied to the  $V_{PP}$  terminal, the overshoot voltage of the pulse should not exceed 14V.

# TC57256AD-15

# TC57256AD-20

## ERASURE CHARACTERISTICS

The TC57256AD's erasure is achieved by applying shortwave ultraviolet light with a wavelength of 2537Å (Angstroms) through the transparent window of the chip.

The integrated dose (ultraviolet light intensity [ $w/cm^2$ ]  $\times$  exposure time [sec.]) for erasure should be a minimum of 15 [ $w \cdot sec/cm^2$ ].

When the Toshiba GL-15 sterilizing lamp is used and the device is exposed at a distance of 1 cm from the lamp surface, erasure will be achieved within 60 minutes.

Using a commercial lamp with an ultraviolet light intensity of 12000 [ $\mu w/cm^2$ ] reduces the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [ $\mu w/cm^2$ ]  $\times$  (20 $\times$ 60) [sec]  $\cong$  15 [ $w \cdot sec/cm^2$ ].)

The TC57256AD's erasure begins to occur when exposed to light with wavelengths shorter than 4000Å. Both sunlight and fluorescent lamps include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

## OPERATION INFORMATION

The TC57256AD's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE	PIN NAMES (NUMBER)	$\overline{CE}$	$\overline{OE}$	$V_{pp}$ (1)	$V_{CC}$ (28)	00 ~ 07 (11 ~ 13, 15 ~ 19)	POWER
		(20)	(22)				
Read Operation ( $T_a = -40 \sim 85^\circ C$ )	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation ( $T_a = 25 \pm 5^\circ C$ )	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L			Data Out	

Note: H;  $V_{IH}$ , L;  $V_{IL}$ , \*;  $V_{IH}$  or  $V_{IL}$

## READ MODE

The TC57256AD has two control functions. The chip enable ( $\overline{CE}$ ) controls the operation power and should be used for device selection.

The output enable ( $\overline{OE}$ ) controls the output buffers, independent of device selection.

Assuming that  $\overline{CE} = \overline{OE} = V_{IL}$ , the output data is valid at the outputs after address access time from stabilizing of all addresses.

The  $\overline{CE}$  to output valid ( $t_{CE}$ ) time is equal to the address access time ( $t_{ACC}$ ).

Assuming that  $\overline{CE} = V_{IL}$  and all addresses are valid, the output data is valid at the outputs after  $t_{OE}$  from the falling edge of  $\overline{OE}$ .

## OUTPUT DESELECT MODE

With  $\overline{CE} = V_{IH}$  or  $\overline{OE} = V_{IH}$ , outputs will be in high impedance state so two or more TC57256AD's can be connected together on a common bus line.

When  $\overline{CE}$  is decoded for device selection, all deselected devices are in low power standby mode.

# TC57256AD-15

# TC57256AD-20

## STANDBY MODE

The TC57256AD has a low power standby mode controlled by the  $\overline{CE}$  signal. By applying a high level to the  $\overline{CE}$  input, the TC57256AD is placed in the standby mode which reduces the operating current to 100 $\mu$ A. The outputs are in a high impedance state, independent of the  $\overline{OE}$  inputs.

## PROGRAM MODE

Initially, when received by customers, all bits of the TC57256AD are in the "1" state, which is the erased state. The programming operation introduces "0s" data into the desired bit locations by electrical programming. The TC57256AD is in the programming mode when the  $V_{PP}$  input is at 12.5V and  $\overline{CE}$  is at TTL-Low under  $\overline{OE}=V_{IH}$ . The TC57256AD can be programmed at any location, anytime, either individually, sequentially or randomly.

## PROGRAM VERIFY MODE

The verify mode verifies that the desired data is correctly programmed on the programmed bits. The verify is accomplished with  $\overline{OE}$  at  $V_{IL}$ .

## PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to  $V_{PP}$  terminal, a high level  $\overline{CE}$  input inhibits the TC57256AD from being programmed.

Programming of two or more TC57256AD's in parallel with different data is easily accomplished: all inputs except for  $\overline{CE}$  and  $\overline{OE}$  are commonly connected, a TTL low level program pulse is applied to the  $\overline{CE}$  of the desired device only, and TTL high level signals are applied to the other devices.

## HIGH SPEED PROGRAMMING MODE

The program time can be greatly reduced by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the  $V_{PP}$  terminal with  $V_{CC}=6V$ .

The programming is achieved by applying a single TTL low level 1ms pulse to the  $\overline{CE}$  input after addresses and data are stable. The programmed data is then verified by using the Program Verify Mode.

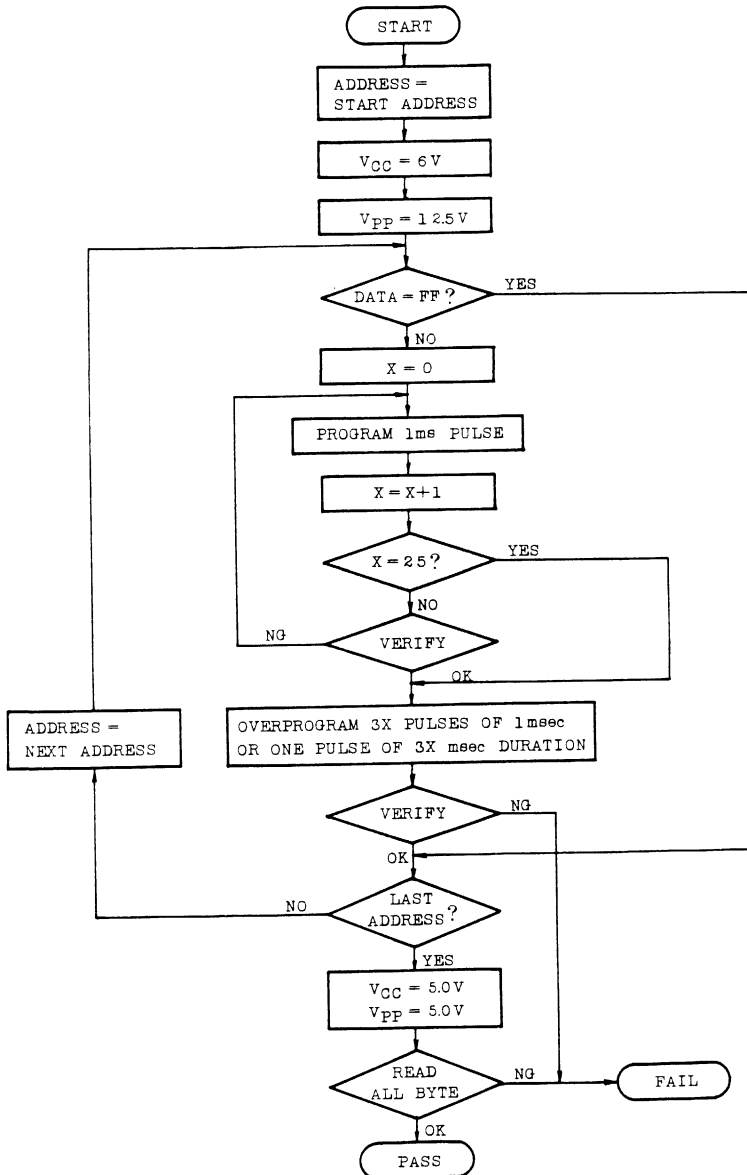
If the programmed data is not correct, another program pulse of 1ms is applied and the programmed data is verified. This should be repeated until the programmed data is correct. (max. 25 times)

After correctly programming the selected addresses, an additional program pulse with a width of 3 times more than that needed for initial programming is applied.

When programming has been completed. Data in all addresses should be verified with  $V_{CC}=V_{PP}=5V$ .

# TC57256AD-15 TC57256AD-20

## HIGH SPEED PROGRAM MODE FLOW CHART





# TC57256AD-15

# TC57256AD-20

## ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TC57256AD which identifies its manufacture and device type.

The programming equipment may be used to read the manufacturer code and device code from the TC57256AD by using this mode before program operation, and automatically set program voltage ( $V_{pp}$ ) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to  $V_{IL}$  in read operation. Data output under these conditions is the manufacturer code. Device code is identified when address A0 is set to  $V_{IH}$ . These two codes possess an odd parity with the parity bit of MSB (07).

The following table shows the electric signature of the TC57256AD.

SIGNATURE	PINS	A0 (10)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	HEX. DATA
Manufacture Code	$V_{IL}$	1	0	0	1	1	0	0	0	0	98
Device Code	$V_{IH}$	1	1	0	0	0	1	0	0	0	C4

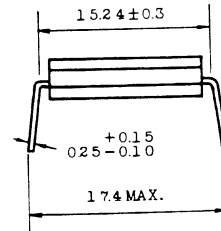
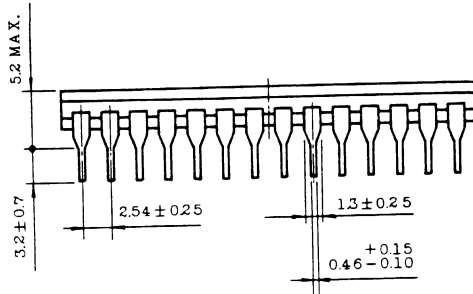
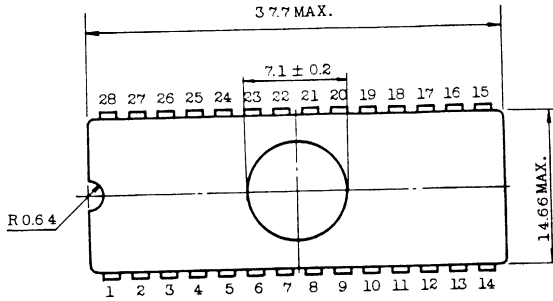
Notes: A9=12V±0.5V

A1 ~ A8, A10 ~ A14,  $\overline{CE}$ ,  $\overline{OE}$ = $V_{IL}$

# TC57256AD-15 TC57256AD-20

## OUTLINE DRAWINGS

Unit in mm



Note 2

Note 1

Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28.

2. This value is measured at the end of leads.

3. All dimensions are in millimeters.

# TOSHIBA MOS MEMORY PRODUCT

65,536 WORD × 8 BIT N-MOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY  
PRELIMINARY

TMM27512D-20, TMM27512D-200  
TMM27512D-25, TMM27512D-250

## DESCRIPTION

The TMM27512D is a 65,536 word × 8 bit ultraviolet light erasable and electrically programmable read memory.

For read operation, the TMM27512D's access time is 200ns/250ns. The TMM27512D operates from a single 5-volt power supply and has a low power standby mode which

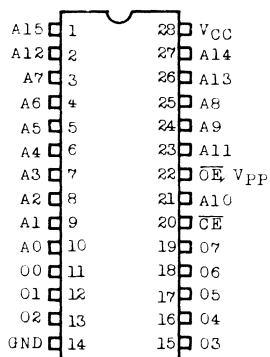
reduces power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the  $\overline{CE}$  input. For program operation, the programming is achieved by using the high speed programming mode. The TMM27512D is fabricated with N-channel silicon double layer gate MOS technology.

## FEATURES

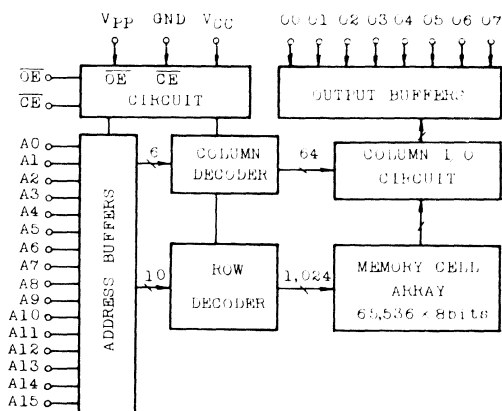
	-20	-25	-200	-250
V <sub>CC</sub>	5V ± 5%		5V ± 10%	
t <sub>acc</sub>	200ns	250ns	200ns	250ns
I <sub>CC2</sub>	120mA		130mA	
I <sub>CC1</sub>	35mA		40mA	

- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with i27512
- Standard 28 pin DIP cerdip package

## PIN CONNECTION (TOP VIEW)



## BLOCK DIAGRAM



## MODE SELECTION

### PIN NAMES

A <sub>0</sub> ~A <sub>15</sub>	Address Inputs
O <sub>0</sub> ~O <sub>7</sub>	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}/V_{PP}$	Output Enable / Program Supply Voltage Input
V <sub>CC</sub>	Power Supply Voltage (+ 5V)
GND	Ground

MODE	PIN	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V <sub>CC</sub> (28)	O <sub>0</sub> ~O <sub>7</sub> (11~13, 15~19)	POWER
Read		L	L	5V	Data Out	Active
Output Deselect		*	H		High Impedance	
Standby		H	*	6V	High Impedance	Standby
Program		L	V <sub>PP</sub>		Data In	
Program Inhibit		H	V <sub>PP</sub>		High Impedance	
Program Verify		L	L	6V	Data Out	Active

\* H or L

**TMM27512D-20, TMM27512D-200**  
**TMM27512D-25, TMM27512D-250**

**MAXIMUM RATINGS**

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	-0.6~7.0	V
V <sub>PP</sub>	Program Supply Voltage	-0.6~14.0	V
V <sub>IN</sub>	Input Voltage	-0.6~7.0	V
V <sub>I/O</sub>	Input/Output Voltage	-0.6~7.0	V
P <sub>D</sub>	Power Dissipation	1.5	W
T <sub>SOLDER</sub>	Soldering Temperature - Time	260 · 10	C·sec
P <sub>STG</sub>	Storage Temperature	-65~125	C
T <sub>OPR</sub>	Operating Temperature	0~70	C

**READ OPERATION**

**D. C. AND RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	TMM27512D-20/25	TMM27512D-200/250
T <sub>a</sub>	Operating Temperature	0~70°C	0~70°C
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	5V±5%	5V±10%

**D. C. AND OPERATING CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>LI</sub>	Input Current	V <sub>IN</sub> =0~V <sub>CC</sub>	—	—	±10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> =0.4~V <sub>CC</sub>	—	—	±10	μA
I <sub>CC1</sub>	Supply Current (Standby)	$\overline{CE}=V_{IH}$	-20/25	—	35	mA
			-200/250	—	40	
I <sub>CC2</sub>	Supply Current (Active)	$\overline{CE}=V_{IL}$	-20/25	—	120	mA
			-20/250	—	130	
V <sub>IH</sub>	Input High Voltage	—	2.0	—	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input Low Voltage	—	-0.3	—	0.8	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> =-400μA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> =2.1mA	—	—	0.4	V
I <sub>PP1</sub>	V <sub>PP</sub> Current	V <sub>PP</sub> =0~V <sub>CC</sub> +0.6	—	—	±10	μA

**TMM27512D-20, TMM27512D-200**  
**TMM27512D-25, TMM27512D-250**

**A. C. CHARACTERISTICS**

SYMBOL	PARAMETER	TMM27512D-20/200		TMM27512D 25/250		UNIT
		MIN.	MAX.	MIN.	MAX.	
$t_{ACC}$	Address Access Time		200	--	250	ns
$t_{CE}$	$\overline{CE}$ to Output Valid		200	--	250	ns
$t_{OE}$	$\overline{OE}$ to Output Valid		70	--	100	ns
$t_{DF1}$	$\overline{CE}$ to Output in High-Z	0	60	0	90	ns
$t_{DF2}$	$\overline{OE}$ to Output in High-Z	0	60	0	90	ns
$t_{OH}$	Output Data Hold Time	0	--	0	--	ns

**A. C. TEST CONDITIONS**

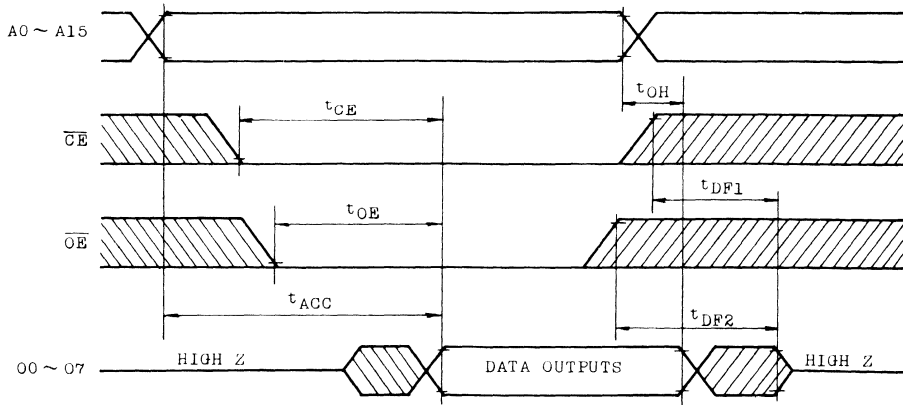
- Output Load : 1 TTL Gate and  $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

**CAPACITANCE \* ( $T_a = 25\text{C}$ ,  $f = 1\text{MHz}$ )**

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$C_{IN1}$	Input Capacitance	$V_{IN} = 0V$	--	4	6	pF
$C_{IN2}$	$\overline{OE}$ $V_{DD}$ Input Capacitance	$V_{IN} = 0V$	--	50	60	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V$	--	8	12	pF

\* This parameter is periodically sampled and is not 100% tested.

**TIMING WAVEFORMS (READ)**



**TMM27512D-20, TMM27512D-200**  
**TMM27512D-25, TMM27512D-250**

**PROGRAM OPERATION**

**D. C. RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.0	—	V <sub>CC</sub> + 1.0	V
V <sub>IL</sub>	Input Low Voltage	-0.3	—	0.8	V
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	5.75	6.0	6.25	V
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	12.0	12.5	13.0	V

**D. C. and OPERATING CHARACTERISTICS** (T<sub>a</sub> = 25 ± 5 °C, V<sub>CC</sub> = 6V ± 0.25V, V<sub>PP</sub> = 12.5V ± 0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>LI</sub>	Input Current	V <sub>IN</sub> = 0 ~ V <sub>CC</sub>	—	—	± 10	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400 μA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA	—	—	0.4	V
I <sub>CC</sub>	V <sub>CC</sub> Supply Current	—	—	—	130	mA
I <sub>PP2</sub>	V <sub>PP</sub> Supply Current	V <sub>PP</sub> = 13.0V	—	—	50	mA
V <sub>ID</sub>	A9 Auto Select Voltage	—	11.5	12.0	12.5	V

**A. C. PROGRAMMING CHARACTERISTICS** (T<sub>a</sub> = 25 ± 5 °C, V<sub>CC</sub> = 6V ± 0.25V, V<sub>PP</sub> = 12.5V ± 0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t <sub>AS</sub>	Address Setup Time	—	2	—	—	μS
t <sub>AH</sub>	Address Hold Time	—	2	—	—	μS
t <sub>OLS</sub>	$\overline{OE}/V_{PP}$ Setup Time	—	2	—	—	μS
t <sub>OEH</sub>	$\overline{OE}/V_{PP}$ Hold Time	—	2	—	—	μS
t <sub>PRT</sub>	$\overline{OE}/V_{PP}$ Pulse Rise Time	—	50	—	—	μS
t <sub>DS</sub>	Data Setup Time	—	2	—	—	μS
t <sub>DH</sub>	Data Hold Time	—	2	—	—	μS
t <sub>VR</sub>	$\overline{OE}/V_{PP}$ Recovery Time	—	2	—	—	μS
t <sub>VCS</sub>	V <sub>CC</sub> Setup Time	—	2	—	—	μS
t <sub>PW</sub>	Initial Program Pulse Width	CE = V <sub>IL</sub> , OE/V <sub>PP</sub> = V <sub>PP</sub>	0.95	1	1.05	ms
t <sub>OPW</sub>	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t <sub>DV</sub>	Data Valid from CE	OE/V <sub>PP</sub> = V <sub>IL</sub>	—	—	1	μS
t <sub>DF</sub>	CE to Output in High-Z	OE/V <sub>PP</sub> = V <sub>IL</sub>	—	—	130	ns

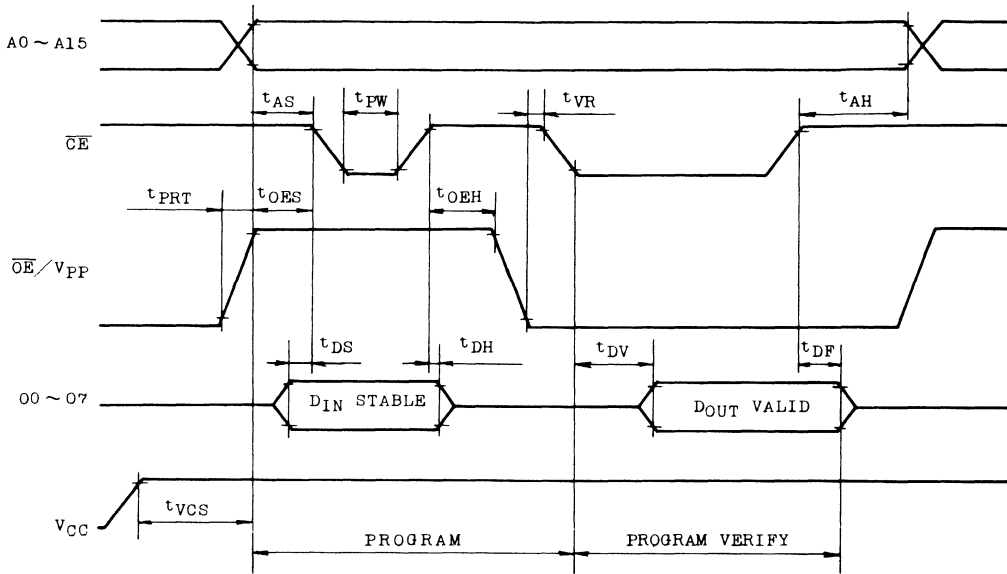
**A. C. TEST CONDITIONS**

- Output Load : 1 TTL Gate and C<sub>L</sub> (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

**TIMING WAVEFORMS (PROGRAM)**

( $V_{CC} = 6V + 0.25V$ ,  $V_{PP} = 12.5V + 0.5V$ )



- Note: (1)  $V_{CC}$  must be applied simultaneously with or before  $V_{PP}$  and cut off simultaneously with or after  $V_{PP}$ .  
(2) Removing the device from the socket and setting the device in the socket with  $V_{PP} = 12.5V$  may cause permanent damage to the device.  
(3) The  $V_{PP}$  supply voltage is permitted up to 14V for program operation; Voltages over 14V should be applied to the  $V_{PP}$  terminal. When the switching pulse voltage is applied to the  $V_{PP}$  terminal, the overshoot voltage of its pulse should not exceed 14V.

# TMM27512D-20, TMM27512D-200 TMM27512D-25, TMM27512D-250

## ERASURE CHARACTERISTICS

The TMM27512D's erasure is achieved by applying shortwave ultraviolet light with a wavelength of 2537Å (Angstroms) through the transparent window of the chip.

The integrated dose (ultraviolet light intensity [ $\mu\text{w}/\text{cm}^2$ ]  $\times$  exposure time [sec.]) for erasure should be a minimum of 15 [ $\text{w} \cdot \text{sec}/\text{cm}^2$ ].

When the Toshiba GL-15 sterilizing lamp is used and the device is exposed at a distance of 1cm from the lamp surface, erasure will be achieved within 60 minutes.

Using a commercial lamp with an ultraviolet light inten-

sity of 12000 [ $\mu\text{w}/\text{cm}^2$ ] reduces the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [ $\mu\text{w}/\text{cm}^2$ ]  $\times$  (10 $\times$ 60) [sec]  $\cong$  15 [ $\text{w} \cdot \text{sec}/\text{cm}^2$ ].)

The TMM27512D's erasure begins to occur when exposed to light with wavelengths shorter than 4000Å. Sunlight and fluorescent lamps both include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

## OPERATION INFORMATION

The TMM27512D's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE	PIN NAMES(NUMBER)	$\overline{\text{CE}}$ (20)	$\overline{\text{OE}}/V_{\text{PP}}$ (22)	$V_{\text{CC}}$ (28)	$O_0 \sim O_7$ (11 ~ 13, 15 ~ 19)	POWER
Read Operation ( $T_a = 0 \sim 70 \text{ C}$ )	Read	L	L	5V	Data Out	Active
	Output Deselect	*	H		High Impedance	Active
	Standby	H	*		High Impedance	Standby
Program Operation ( $T_a = 25 \pm 5 \text{ C}$ )	Program	L	$V_{\text{PP}}$	6V	Data In	Active
	Program Inhibit	H	$V_{\text{PP}}$		High Impedance	Active
	Program Verify	L	L		Data Out	Active

Note : H ;  $V_{\text{IH}}$ , L ;  $V_{\text{IL}}$ , \* ;  $V_{\text{IH}}$  or  $V_{\text{IL}}$

### READ MODE

The TMM27512D has two control functions. The chip enable ( $\overline{\text{CE}}$ ) controls the operation power and should be used for device selection.

The output enable ( $\overline{\text{OE}}$ ) controls the output buffers, independent of device selection.

Assuming that  $\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}$ , the output data is valid at the outputs after address access time from stabilizing of all

addresses.

The  $\overline{\text{CE}}$  to output valid ( $t_{\text{CE}}$ ) is equal to the address access time ( $t_{\text{ACC}}$ ).

Assuming that  $\overline{\text{CE}} = V_{\text{IL}}$ , and all addresses are valid, the output data is valid at the outputs after  $t_{\text{OE}}$  from the falling edge of  $\overline{\text{OE}}$ .

### OUTPUT Deselect MODE

With  $\overline{\text{CE}} = V_{\text{IH}}$  or  $\overline{\text{OE}} = V_{\text{IH}}$ , outputs will be in a high impedance state, so two or more TMM27512D's can be

connected together on a common bus line.

When  $\overline{\text{CE}}$  is decoded for device selection, all deselected devices are in low power standby mode.



## TMM27512D-20, TMM27512D-200 TMM27512D-25, TMM27512D-250

### STANDBY MODE

The TMM27512D has a low power standby mode controlled by the  $\overline{CE}$  signal.

By applying a high level to the  $\overline{CE}$  input, the TMM27512D

is placed in the standby mode which reduces 70% of the operating current. The outputs are in a high impedance state, independent of the  $\overline{OE}$  inputs.

### PROGRAM MODE

Initially, when received by customers, all bits of the TMM27512D are in the "1" state which is the erased state. The programming operation introduces "0s" data into the desired bit locations by electrical programming.

The TMM27512D is in the programming mode when the  $\overline{OE}/V_{PP}$  input is at 12.5V and  $\overline{CE}$  is at TTL-Low level

The TMM27512D can be programmed at any location, anytime, either individually, sequentially or at random.

### PROGRAM VERIFY MODE

The verify mode verifies that desired data is correctly programmed on the programmed bits.

The verify is accomplished with  $\overline{OE}/V_{PP}$  at  $V_{IL}$  and at  $\overline{CE}$  at  $V_{IL}$ .

### PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to  $V_{PP}$  terminal, a TTL high level  $\overline{CE}$  input inhibits the TMM27512D from being programmed.

Programming of two or more TMM27512D's in parallel

with different data is easily accomplished: all inputs except for  $\overline{CE}$  are commonly connected, a TTL Low level program pulse is applied to the  $\overline{CE}$  of the desired device only, and TTL high level signals are applied to the other devices.

### HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode.

This high speed programming mode is performed at  $V_{CC}=6.0V$  and  $\overline{OE}/V_{PP}=12.5V$

The programming is achieved by applying a single TTL low level 1ms pulse to the  $\overline{CE}$  input after addresses and data are stable. The programmed data is then verified by using the Program Verify Mode.

If the programmed data is not correct, another program

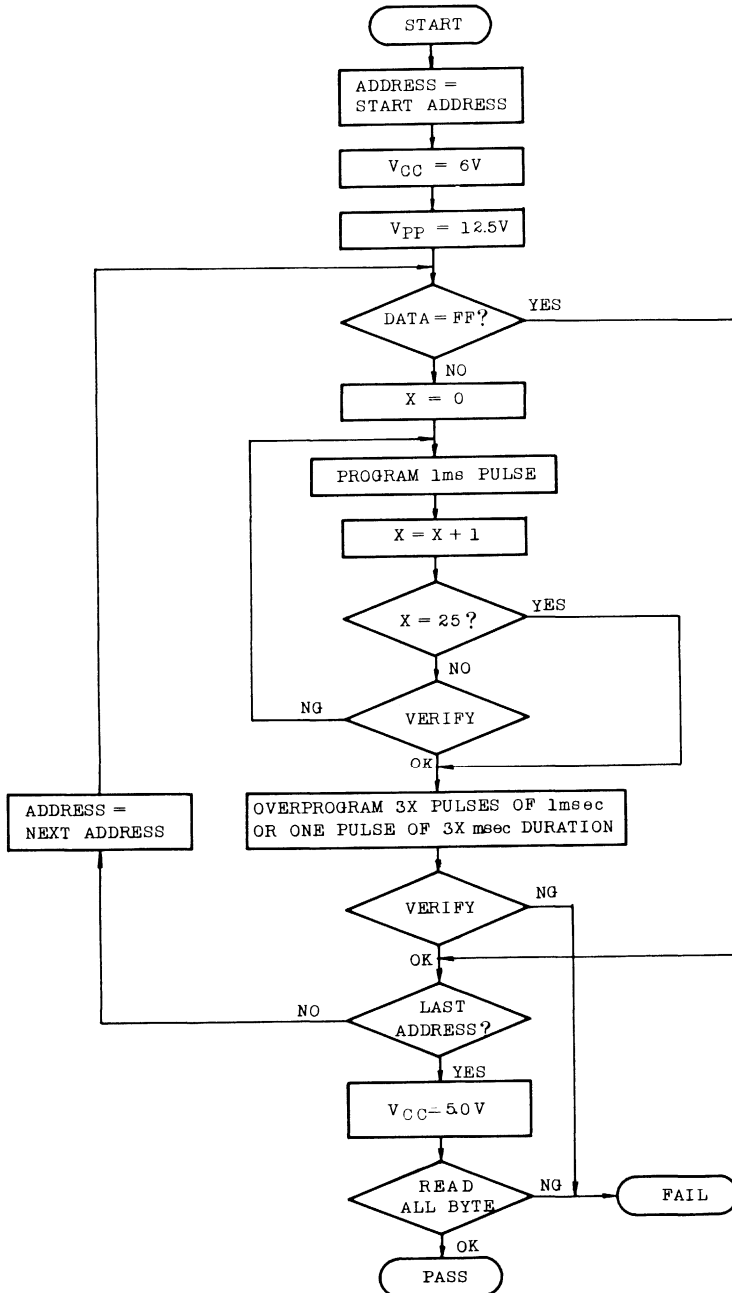
pulse of 1ms is applied and the programmed data is reverified. This should be repeated until the programmed data is correct. (max. 25 times)

After correctly programming the selected address, an additional program pulse with width 3 times that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with  $V_{CC}=5V$ .

TMM27512D-20, TMM27512D-200  
TMM27512D-25, TMM27512D-250

### HIGH SPEED PROGRAM MODE FLOW CHART



**TMM27512D-20, TMM27512D-200  
TMM27512D-25, TMM27512D-250**

**ELECTRIC SIGNATURE MODE**

Electric signature mode allows a code to be read from the TMM27512D which identifies its manufacture and device type.

The programming equipment may be used to read out the manufacturer code and device code from the TMM27512D by using this mode before program operation and automatically set program voltage ( $V_{pp}$ ) and algorithm.

Electric Signature mode is set up when 12V is applied to

address line A9 and the rest of address lines are set to  $V_{IL}$  in read operation. Data output under these conditions is the manufacturer code. Device code is identified when address A0 is set to  $V_{IH}$ . These two codes possess an odd parity with the parity bit of MSB (07).

The following table shows electric signature of the TMM27512D.

SIGNATURE	PINS	A <sub>0</sub> (10)	O <sub>7</sub> (19)	O <sub>6</sub> (18)	O <sub>5</sub> (17)	O <sub>4</sub> (16)	O <sub>3</sub> (15)	O <sub>2</sub> (13)	O <sub>1</sub> (12)	O <sub>0</sub> (11)	HEX DATA
Manufacture Code	$V_{IL}$	1	0	0	1	1	0	0	0	0	98
Device Code	$V_{IH}$	0	0	0	1	0	1	0	1	1	15

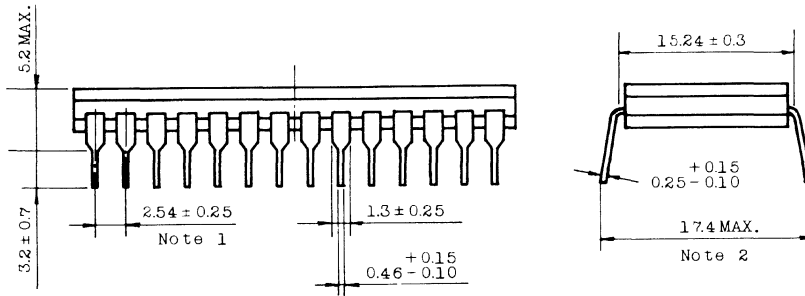
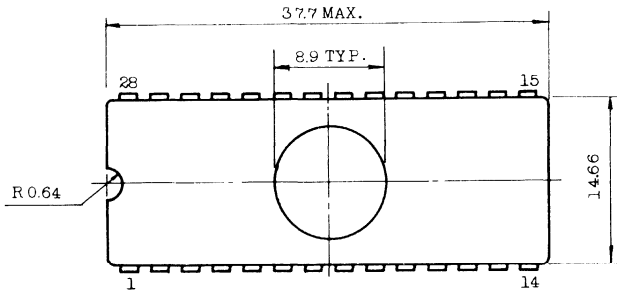
Notes : A9 = 12V ± 0.5V

A1 ~ A8, A10 ~ A15,  $\overline{CE}$ ,  $\overline{OE}$  =  $V_{IL}$

**TMM27512D-20, TMM27512D-200**  
**TMM27512D-25, TMM27512D-250**

**OUTLINE DRAWINGS**

Unit in mm



- Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.  
 2. This value is measured at the end of leads.  
 3. All dimensions are in millimeters.

Note Toshiba does not assume any responsibility for use of any circuitry described without notice, to change said circuitry. no circuit patent licenses are implied, and Toshiba reserves the right, at any time  
 c May, 1986 Toshiba Corporation

# TOSHIBA MOS MEMORY PRODUCT

65,536 WORD × 8 BIT N-MOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY  
PRELIMINARY

## TMM27512DI-20 TMM27512DI-25

### DESCRIPTION

The TMM27512DI is a 65,536 word × 8 bit ultraviolet light erasable and electrically programmable read only memory.

For read operation, the TMM27512DI's access time is 200ns/250ns. The TMM27512DI operates from a single 5-volt power supply and has a low power standby mode which reduces power dissipation without increasing access time.

The standby mode is achieved by applying a TTL-high level signal to the  $\overline{CE}$  input.

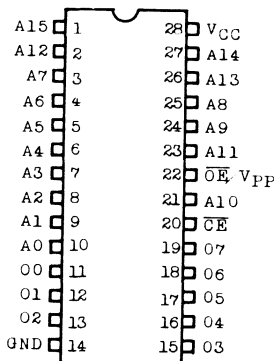
For program operation, the programming is achieved by using the high speed programming mode. TMM27512DI is fabricated with N-channel silicon double layer gate MOS technology.

### FEATURES

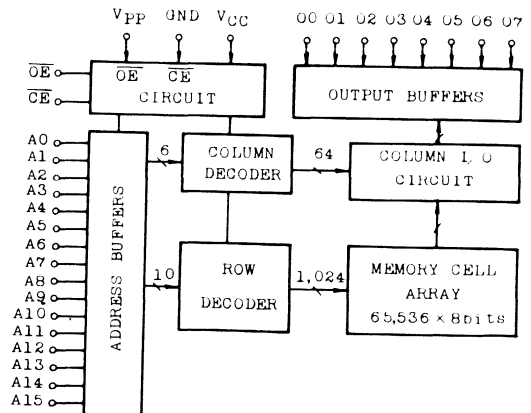
	-15	-20
V <sub>CC</sub>	5V ± 5%	
t <sub>ACC</sub>	150ns	200ns
I <sub>CC2</sub>	120mA	
I <sub>CC1</sub>	35mA	

- Wide operating temperature range -40~85°C
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with i27512
- Standard 28 pin DIP cerdip package

### PIN CONNECTION (TOP VIEW)



### BLOCK DIAGRAM



### PIN NAMES

A <sub>0</sub> ~A <sub>15</sub>	Address Inputs
O <sub>0</sub> ~O <sub>7</sub>	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}/V_{PP}$	Output Enable Input / Program Supply Voltage
V <sub>CC</sub>	Power Supply Voltage (+5V)
GND	Ground

### MODE SELECTION

MODE	PIN	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V <sub>CC</sub> (28)	O <sub>0</sub> ~O <sub>7</sub> (11~13, 15~19)	POWER
Read		L	L	5V	Data Out	Active
Output Deselect		*	H		High Impedance	
Standby		H	*		High Impedance	
Program		L	V <sub>PP</sub>	6V	Data In	Active
Program Inhibit		H	V <sub>PP</sub>		High Impedance	
Program Verify		L	L		Data Out	

\* H or L

# TMM27512DI-20

# TMM27512DI-25

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	-0.6~7.0	V
V <sub>PP</sub>	Program Supply Voltage	-0.6~14.0	V
V <sub>IN</sub>	Input Voltage	-0.6~7.0	V
V <sub>I/O</sub>	Input/Output Voltage	-0.6~7.0	V
P <sub>D</sub>	Power Dissipation	1.5	W
T <sub>SOLDER</sub>	Soldering Temperature · Time	260 · 10	°C·sec
P <sub>STG</sub>	Storage Temperature	-65~125	°C
T <sub>OPR</sub>	Operating Temperature	-40~85	°C

## READ OPERATION

### D. C. AND RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27512DI-20/25
T <sub>a</sub>	Operating Temperature	-40~85°C
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	5V±5%

### D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>LI</sub>	Input Current	V <sub>IN</sub> = 0~V <sub>CC</sub>	—	—	±10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0.4~V <sub>CC</sub>	—	—	±10	μA
I <sub>CC1</sub>	Supply Current (Standby)	CE = V <sub>IH</sub>	—	—	40	mA
I <sub>CC2</sub>	Supply Current (Active)	CE = V <sub>IL</sub>	—	—	130	mA
V <sub>IH</sub>	Input High Voltage	—	2.2	—	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input Low Voltage	—	-0.3	—	0.8	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400μA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA	—	—	0.4	V
I <sub>PP1</sub>	V <sub>PP</sub> Current	V <sub>PP</sub> = 0~V <sub>CC</sub> +0.6	—	—	±10	μA

# TMM27512DI-20

# TMM27512DI-25

## A. C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM27512DI-20		TMM27512DI-25		UNIT
		MIN.	MAX.	MIN.	MAX.	
$t_{ACC}$	Address Access Time	---	200	---	250	ns
$t_{CE}$	CE to Output Valid	---	200	---	250	ns
$t_{OE}$	OE to Output Valid	---	70	---	100	ns
$t_{DF1}$	CE to Output in High-Z	0	60	0	90	ns
$t_{DF2}$	OE to Output in High-Z	0	60	0	90	ns
$t_{OH}$	Output Data Hold Time	0	---	0	---	ns

## A. C. TEST CONDITIONS

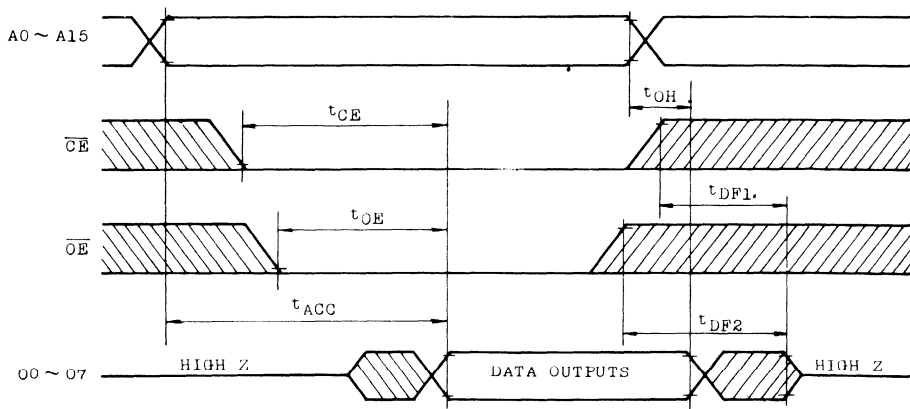
- Output Load : 1 TTL Gate and  $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

## CAPACITANCE \* ( $T_a = 25^\circ\text{C}$ , $f = 1\text{MHz}$ )

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$C_{IN1}$	Input Capacitance	$V_{IN} = 0\text{V}$	---	4	6	pF
$C_{IN2}$	OE $V_{PP}$ Input Capacitance	$V_{IN} = 0\text{V}$	---	50	60	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0\text{V}$	---	8	12	pF

\* This parameter is periodically sampled and is not 100% tested.

## TIMING WAVEFORMS (READ)



# TMM27512DI-20

# TMM27512DI-25

## PROGRAM OPERATION

### D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input Low Voltage	-0.3	—	0.8	V
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	5.75	6.0	6.25	V
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	12.0	12.5	13.0	V

### D. C. and OPERATING CHARACTERISTICS (T<sub>a</sub> = 25 ± 5°C, V<sub>CC</sub> = 6V ± 0.25V, V<sub>PP</sub> = 12.5V ± 0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>LI</sub>	Input Current	V <sub>IN</sub> = 0 ~ V <sub>CC</sub>	—	—	±10	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400μA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA	—	—	0.4	V
I <sub>CC</sub>	V <sub>CC</sub> Supply Current	—	—	—	130	mA
I <sub>PP2</sub>	V <sub>PP</sub> Supply Current	V <sub>PP</sub> = 13.0V	—	—	50	mA
V <sub>ID</sub>	A9 Auto Select Voltage	—	11.5	12.0	12.5	V

### A. C. PROGRAMMING CHARACTERISTICS (T<sub>a</sub> = 25 ± 5°C, V<sub>CC</sub> = 6V ± 0.25V, V<sub>PP</sub> = 12.5V ± 0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t <sub>AS</sub>	Address Setup Time	—	2	—	—	μs
t <sub>AH</sub>	Address Hold Time	—	2	—	—	μs
t <sub>OES</sub>	$\overline{OE}/V_{PP}$ Setup Time	—	2	—	—	μs
t <sub>OEH</sub>	$\overline{OE}/V_{PP}$ Hold Time	—	2	—	—	μs
t <sub>PRT</sub>	$\overline{OE}/V_{PP}$ Pulse Rise Time	—	50	—	—	μs
t <sub>DS</sub>	Data Setup Time	—	2	—	—	μs
t <sub>DH</sub>	Data Hold Time	—	2	—	—	μs
t <sub>VR</sub>	$\overline{OE}/V_{PP}$ Recovery Time	—	2	—	—	μs
t <sub>VCS</sub>	V <sub>CC</sub> Setup Time	—	2	—	—	μs
t <sub>PW</sub>	Initial Program Pulse Width	$\overline{CE} = V_{IL}, \overline{OE}/V_{PP} = V_{PP}$	0.95	1	1.05	ms
t <sub>OPW</sub>	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t <sub>DV</sub>	Data Valid from $\overline{CE}$	$\overline{OE}/V_{PP} = V_{IL}$	—	—	1	μs
t <sub>DF</sub>	$\overline{CE}$ to Output in High-Z	$\overline{OE}/V_{PP} = V_{IL}$	—	—	130	ns

### A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C<sub>L</sub> (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

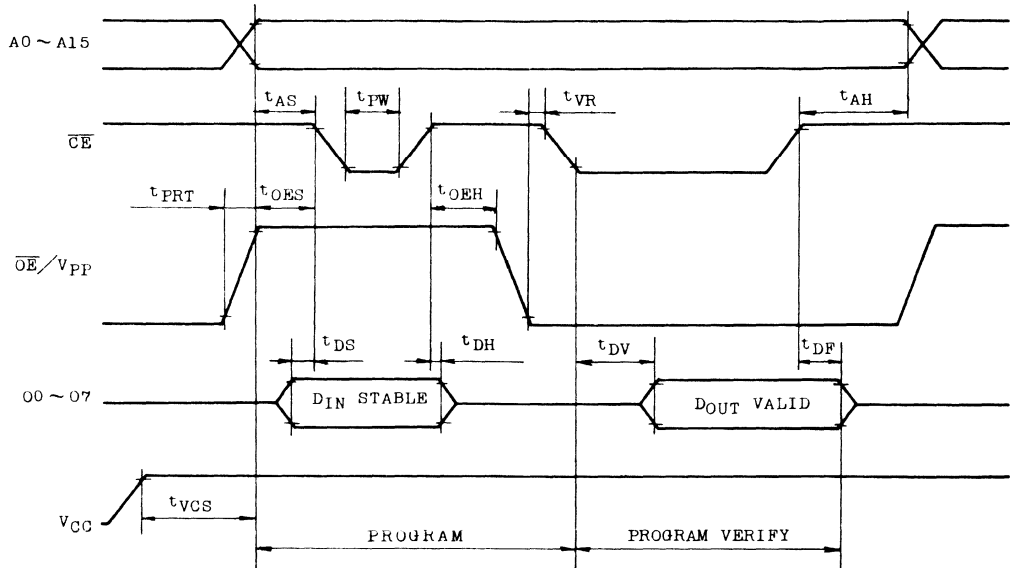
Note : 1. The length of the overprogram pulse may vary as a function of the counter value X.



# TMM27512DI-20 TMM27512DI-25

## TIMING WAVEFORMS (PROGRAM)

( $V_{CC} = 6V \pm 0.25V$ ,  $V_{PP} = 12.5V \pm 0.5V$ )



- Note :
1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and cut off simultaneously or after  $V_{PP}$ .
  2. Removing the device from socket and setting the device in socket with  $V_{PP} = 12.5V$  may cause permanent damage to the device.
  3. The  $V_{PP}$  supply voltage is permitted up to 14V for program operation. So the voltage over 14V should be applied to the  $V_{PP}$  terminal. When the switching pulse voltage is applied to the  $V_{PP}$  terminal, the overshoot voltage of its pulse should not be exceeded 14V.

# TMM27512DI-20

# TMM27512DI-25

## ERASURE CHARACTERISTICS

The TMM27512DI's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the Chip through the transparent window. Then integrated dose (ultraviolet light intensity  $[W/cm^2]$   $\times$  exposure time [sec.] ) for erasure should be a minimum of 15  $[w\cdot sec/cm^2]$

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose

ultraviolet light intensity is a 12000  $[\mu w/cm^2]$  will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000  $[\mu w/cm^2]$   $\times$  (10 $\times$ 60) [sec]  $\cong$  15  $[w\cdot sec/cm^2]$  .)

The TMM27512DI's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

## OPERATION INFORMATION

The TMM27512DI's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE	PIN NAMES(NUMBER)	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	$V_{CC}$ (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read Operation ( $T_a = -40 \sim 85^\circ C$ )	Read	L	L	5V	Data Out	Active
	Output Deselect	*	H		High Impedance	Active
	Standby	H	*		High Impedance	Standby
Program Operation ( $T_a = 25 \pm 5^\circ C$ )	Program	L	$V_{PP}$	6V	Data In	Active
	Program Inhibit	H	$V_{PP}$		High Impedance	Active
	Program Verify	L	L		Data Out	Active

Note : H ;  $V_{IH}$ , L ;  $V_{IL}$ , \* ;  $V_{IH}$  or  $V_{IL}$

## READ MODE

The TMM27512DI has two control functions. The chip enable ( $\overline{CE}$ ) controls the operation power and should be used for device selection.

The output enable ( $\overline{OE}$ ) control the output buffers, independent of device selection.

Assuming that  $\overline{CE} = \overline{OE} = V_{IL}$ , the output data is valid at the outputs after address access time from

stabilizing of all addresses.

The  $\overline{CE}$  to output valid ( $t_{CE}$ ) is equal to address access time ( $t_{ACC}$ ).

Assuming that  $\overline{CE} = V_{IL}$  and all addresses are valid, the output data is valid at the outputs after  $t_{OE}$  from the falling edge of  $\overline{OE}$ .

## OUTPUT Deselect MODE

Assuming that  $\overline{CE} = V_{IH}$  or  $\overline{OE} = V_{IH}$ , the outputs will be in a high impedance state.

So two or more TMM27512DI's can be con-

nected together on a common bus line.

When  $\overline{CE}$  is decoded for device selection, all deselected devices are in low power standby mode.

# TMM27512DI-20

# TMM27512DI-25

## STANDBY MODE

The TMM27512DI has a low power standby mode controlled by the  $\overline{CE}$  signal.

By applying a high level to the  $\overline{CE}$  input, the TMM27512DI is placed in the standby mode which

## PROGRAM MODE

Initially, when received by customers, all bits of the TMM27512DI are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

## PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

## PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to  $V_{PP}$  terminal, a TTL high level  $\overline{CE}$  input inhibits the TMM27512DI from being programmed.

Programming of two or more TMM27512DI's is

## HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode.

This high speed programming mode is performed at  $V_{CC}=6.0V$  and  $\overline{OE}/V_{PP}=12.5V$

The programming is achieved by applying a single TTL low level 1ms pulse to the  $\overline{CE}$  input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another

reduce 70% of the operating current by applying TTL-high level ( $V_{CC}$ ) and then the outputs are in a high impedance state, independent of the  $\overline{OE}$  inputs.

The TMM27512DI is in the programming mode when the  $\overline{OE}/V_{PP}$  input is at 12.5V and  $\overline{CE}$  is at TTL-Low level.

The TMM27512DI can be programmed any location at anytime either individually, sequentially, or at random.

The verify is accomplished with  $\overline{OE}/V_{PP}$  at  $V_{IL}$  and  $\overline{CE}$  at  $V_{IL}$ .

parallel with different data is easily accomplished. That is, all inputs except for  $\overline{CE}$  may be commonly connected, and a TTL Low level program pulse is applied to the  $\overline{CE}$  of the desired device only and TTL high level signal is applied to the other devices.

program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

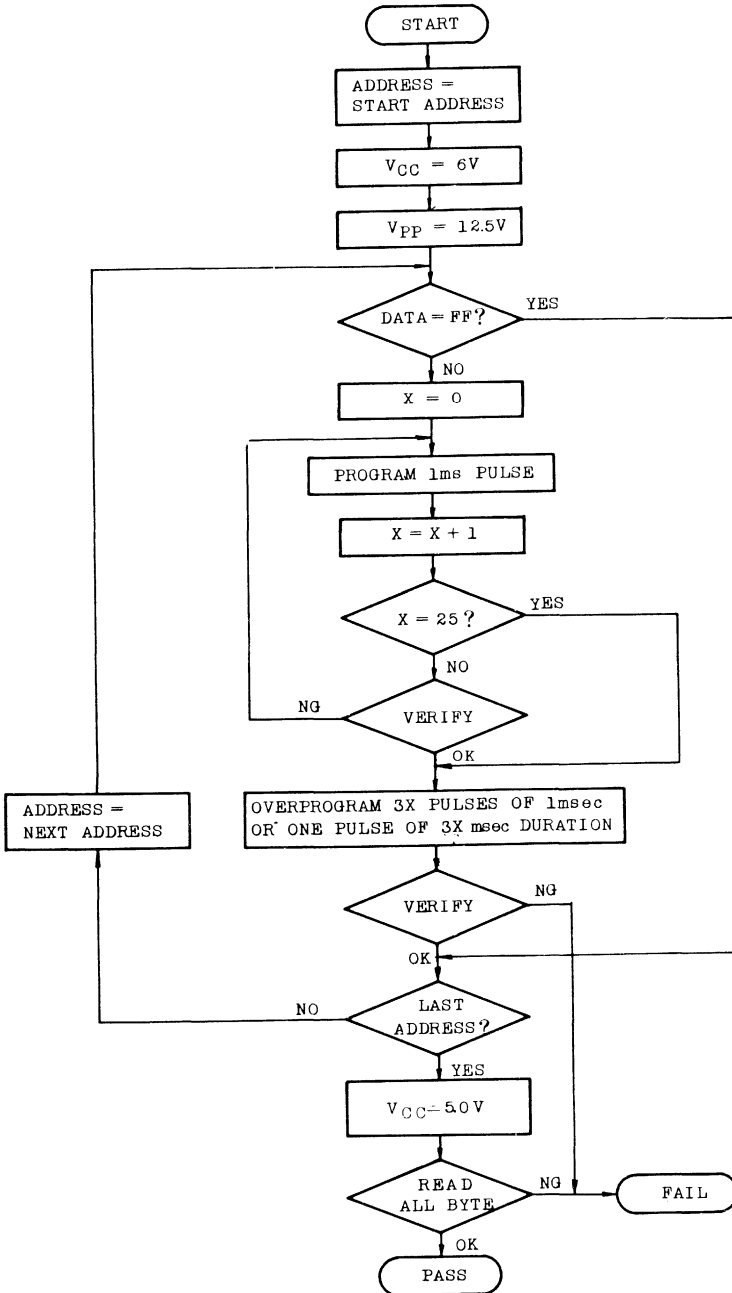
After correctly programming the selected address, the additional program pulse with width 3 times that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with  $V_{CC}=5V$ .

# TMM27512DI-20

# TMM27512DI-25

## HIGH SPEED PROGRAM MODE FLOW CHART



# TMM27512DI-20

# TMM27512DI-25

## ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM27512DI which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM27512DI by using this mode before program operation and automatically set program voltage ( $V_{PP}$ ) and algorithm.

Electric Signature mode is set up when 12V is

applied to address line A9 and the rest of address lines is set to  $V_{IL}$  in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to  $V_{IH}$ . These two codes possess an odd parity with the parity bit of MSB (O7).

The following table shows electric signature of TMM27512DI.

SIGNATURE	PINS	A <sub>0</sub> (10)	O <sub>7</sub> (19)	O <sub>6</sub> (18)	O <sub>5</sub> (17)	O <sub>4</sub> (16)	O <sub>3</sub> (15)	O <sub>2</sub> (13)	O <sub>1</sub> (12)	O <sub>0</sub> (11)	HEX. DATA
Manufacture Code	$V_{IL}$	1	0	0	0	1	1	0	0	0	98
Device Code	$V_{IH}$	0	0	0	0	1	0	1	0	1	15

Notes : A9 = 12V + 0.5V

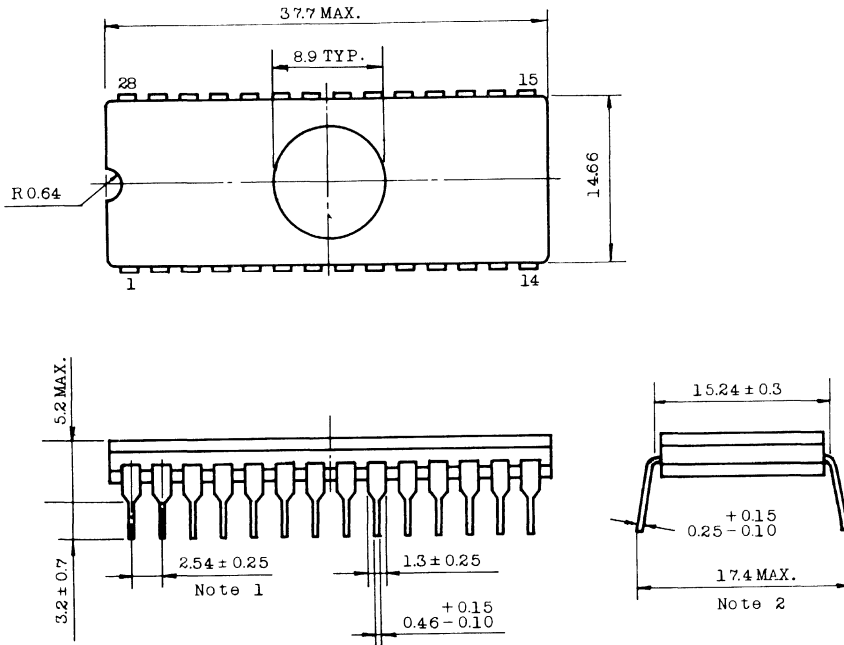
A1 ~ A8, A10 ~ A15, CE, OE =  $V_{IL}$

# TMM27512DI-20

# TMM27512DI-25

## OUTLINE DRAWINGS

Unit in mm



- Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No. 1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in milimeters.

**Note: Toshiba does not assume any responsibility for use of any circuitry described: no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.**  
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# TOSHIBA MOS MEMORY PRODUCT

**1 MEGA BIT (131,072 WORD × 8 BIT)**  
 SILICON STACKED GATE MOS  
 CMOS U.V. Erasable & Electrically  
 Programmable Read Only Memory

**TC571000D-20, TC571000D-25**  
**TC571001D-20, TC571001D-25**

## DESCRIPTION

The TC571000D/TC571001D is a 131,072 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory.

The TC571000D is JEDEC standard pin configuration and the TC571001D is compatible with 28 pin 1M bit Mask ROM. Both products are packed in 32 pin standard cerdip package.

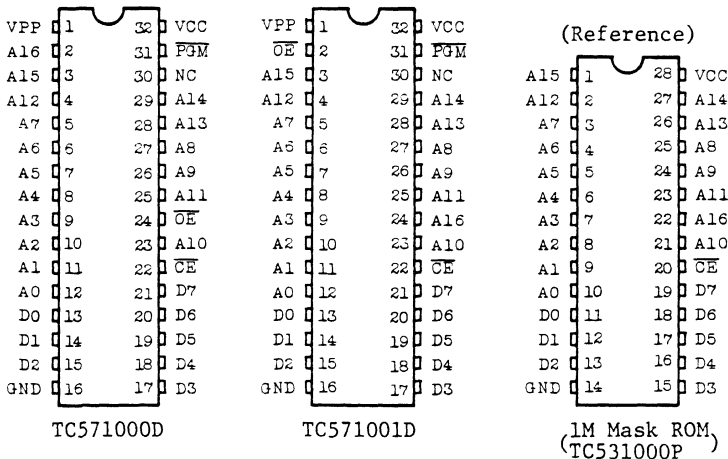
TC571000D/TC571001D is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 30mA/5.0MHz and access time of 200ns/250ns.

The programming times of the TC571000D/TC571001D except overhead times of EPROM programmer is only 14 seconds by using the high speed programming algorithm.

## FEATURES

- Peripheral circuit: CMOS  
 Memory cell : N-MOS
- Fast access Time  
 TC571000D-20/TC571001D-20: 200ns  
 TC571000D-25/TC571001D-25: 250ns
- Low power dissipation  
 Active : 30mA/5.0MHz  
 Standby: 100µA (Ta=85°C)
- Single 5V power supply
- Wide operating temperature range: -40 ~ 85°C
- Full static operation
- High speed programming operation: t<sub>PI</sub> 0.1ms
- Input and output TTL compatible
- JEDEC standard 32 pin: TC571000D
- 1M MROM compatible : TC571001D
- Standard 32 pin DIP cerdip package

## PIN CONNECTION (TOP VIEW)

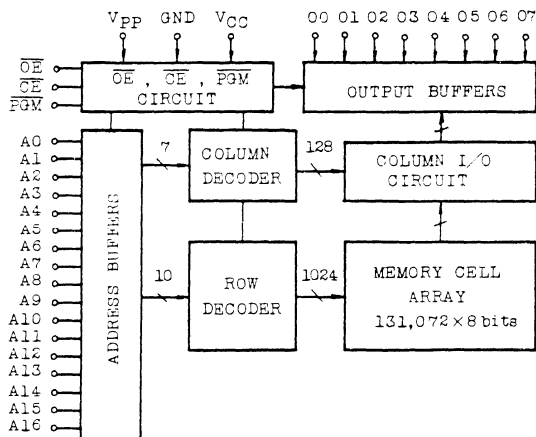


## PIN NAMES

AO ~ A16	Address Inputs
DO ~ D7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
PGM	Program Control Input
VCC	VCC Supply Voltage
VPP	Program Supply Voltage
GND	Ground
NC	No Connection

**TC571000D-20, TC571000D-25**  
**TC571001D-20, TC571001D-25**

**BLOCK DIAGRAM**



**MODE SELECTION**

MODE \ PIN	PGM	CE	OE	V <sub>PP</sub>	V <sub>CC</sub>	00 ~ 07	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	
Program	L	L	*	12.75V	6.25V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

\* : H or L

**MAXIMUM RATINGS**

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	VCC Power Supply Voltage	-0.6 ~ 7.0	V
V <sub>PP</sub>	Program Supply Voltage	-0.6 ~ 14.0	V
V <sub>IN</sub>	Input Voltage	-0.6 ~ 7.0	V
V <sub>I/O</sub>	Input/Output Voltage	-0.6 ~ V <sub>CC</sub> +0.5	V
P <sub>D</sub>	Power Dissipation	1.5	W
T <sub>SOLDER</sub>	Soldering Temperature Time	260 • 10	°C•sec
T <sub>STRG</sub>	Storage Temperature	-65 ~ 125	°C
T <sub>OPR</sub>	Operating Temperature	-40 ~ 85	°C



**TC571000D-20, TC571000D-25**  
**TC571001D-20, TC571001D-25**

**READ OPERATION**

**D.C. RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	-	0.8	
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	4.75	5.00	5.25	
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	V <sub>CC</sub> -0.6	V <sub>CC</sub>	V <sub>CC</sub> +0.6	

**D.C. and OPERATING CHARACTERISTICS (T<sub>a</sub>=-40 ~ 85°C, V<sub>CC</sub>=5V±5%)**

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I <sub>LI</sub>	Input Current	V <sub>IN</sub> =0 ~ V <sub>CC</sub>	-	-	±10	μA	
I <sub>CC01</sub>	Operating Current	$\overline{CE}=0V$ I <sub>out</sub> =0mA	f=5.0MHz	-	-	30	mA
I <sub>CC02</sub>			f=1MHz	-	-	10	
I <sub>CCS1</sub>	Standby Current	$\overline{CE}=V_{IH}$	-	-	1	mA	
I <sub>CCS2</sub>		$\overline{CE}=V_{CC}-0.2V$	-	-	100		μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> =-400μA	2.4	-	-	V	
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> =2.1mA	-	-	0.4	V	
I <sub>PP1</sub>	V <sub>PP</sub> Current	V <sub>PP</sub> =V <sub>CC</sub> ±0.6V	-	-	±10	μA	
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> =0.4V ~ V <sub>CC</sub>	-	-	10	μA	

**A.C. CHARACTERISTICS (T<sub>a</sub>=-40 ~ 85°C, V<sub>CC</sub>=5V±5%, V<sub>pp</sub>=V<sub>CC</sub>±0.6V)**

SYMBOL	PARAMETER	TC571000D-20/TC571001D-20		TC571000D-25/TC571001D-25		UNIT
		MIN.	MAX.	MIN.	MAX.	
t <sub>ACC</sub>	Address Access Time	-	200	-	250	ns
t <sub>CE</sub>	$\overline{CE}$ to Output Valid	-	200	-	250	
t <sub>OE</sub>	$\overline{OE}$ to Output Valid	-	70	-	100	
t <sub>PGM</sub>	$\overline{PGM}$ to Output Valid	-	70	-	100	
t <sub>DF1</sub>	$\overline{CE}$ to Output in High-Z	0	60	0	90	
t <sub>DF2</sub>	$\overline{OE}$ to Output in High-Z	0	60	0	90	
t <sub>DF3</sub>	$\overline{PGM}$ to Output in High-Z	0	60	0	90	
t <sub>OH</sub>	Output Data Hold Time	0	-	0	-	

**A.C. TEST CONDITIONS**

Output Load : 1 TTL Gate and C<sub>L</sub>=100pF  
 Input Pulse Rise and Fall Times : 10ns Max.  
 Input Pulse Levels : 0.45V to 2.4V  
 Timing Measurement Reference Level : Inputs 0.8V and 2.2V Outputs 0.8V and 2.0V

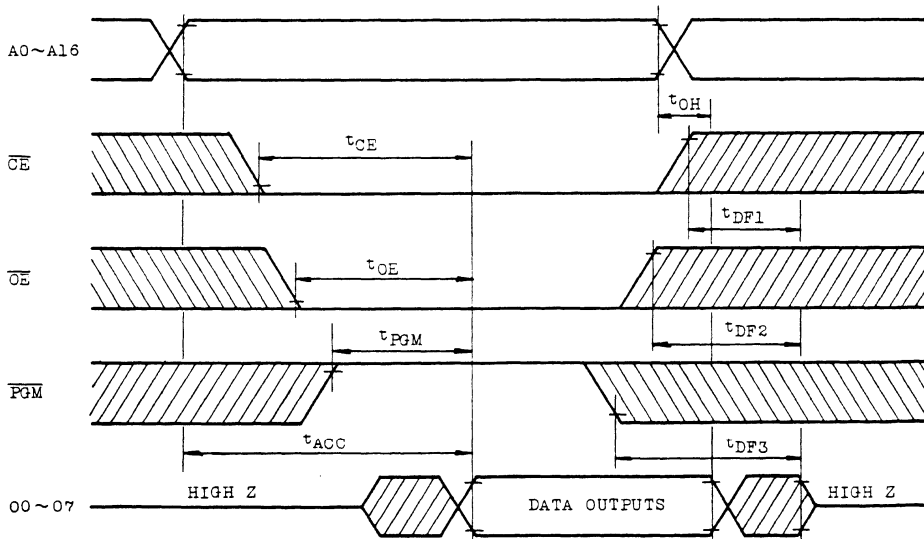
**TC571000D-20, TC571000D-25**  
**TC571001D-20, TC571001D-25**

CAPACITANCE \* ( $T_a=25^\circ\text{C}$ ,  $f=1\text{MHz}$ )

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$C_{IN}$	Input Capacitance	$V_{IN}=0V$	-	4	8	pF
$C_{OUT}$	Output Capacitance	$V_{OUT}=0V$	-	10	12	

\* This parameter is periodically sampled is not 100% tested.

TIMING WAVEFORMS (READ)



**TC571000D-20, TC571000D-25**  
**TC571001D-20, TC571001D-25**

**HIGH SPEED PROGRAM OPERATION**

**D.C. RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{IH}$	Input High Voltage	2.2	-	$V_{CC}+1.0$	V
$V_{IL}$	Input Low Voltage	-0.3	-	0.8	
$V_{CC}$	$V_{CC}$ Power Supply Voltage	6.00	6.25	6.50	
$V_{PP}$	$V_{PP}$ Power Supply Voltage	12.50	12.75	13.00	

**D.C. AND OPERATING CHARACTERISTICS ( $T_a=25\pm 5^\circ\text{C}$ ,  $V_{CC}=6.25\pm 0.25\text{V}$ ,  $V_{PP}=12.75\pm 0.25\text{V}$ )**

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$I_{LI}$	Input Current	$V_{IN}=0 \sim V_{CC}$	-	-	$\pm 10$	$\mu\text{A}$
$V_{OH}$	Output High Voltage	$I_{OH}=-400\mu\text{A}$	2.4	-	-	V
$V_{OL}$	Output Low Voltage	$I_{OL}=2.1\text{mA}$	-	-	0.4	V
$I_{CC}$	$V_{CC}$ Supply Current	-	-	-	30	mA
$I_{PP2}$	$V_{PP}$ Supply Current	$V_{PP}=13.0\text{V}$	-	-	50	mA
$V_{ID}$	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

**A.C. PROGRAMMING CHARACTERISTICS ( $T_a=25\pm 5^\circ\text{C}$ ,  $V_{CC}=6.25\pm 0.25\text{V}$ ,  $V_{PP}=12.75\pm 0.25\text{V}$ )**

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$t_{AS}$	Address Setup Time	-	2	-	-	$\mu\text{s}$
$t_{AH}$	Address Hold Time	-	2	-	-	$\mu\text{s}$
$t_{CES}$	$\overline{CE}$ Setup Time	-	2	-	-	$\mu\text{s}$
$t_{CEH}$	$\overline{CE}$ Hold Time	-	2	-	-	$\mu\text{s}$
$t_{DS}$	Data Setup Time	-	2	-	-	$\mu\text{s}$
$t_{DH}$	Data Hold Time	-	2	-	-	$\mu\text{s}$
$t_{VS}$	$V_{PP}$ Setup Time	-	2	-	-	$\mu\text{s}$
$t_{PW}$	Program Pulse Width	-	0.095	0.1	0.105	ms
$t_{OE}$	$\overline{OE}$ to Output Valid	-	-	-	100	ns
$t_{DF2}$	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	-	-	90	ns

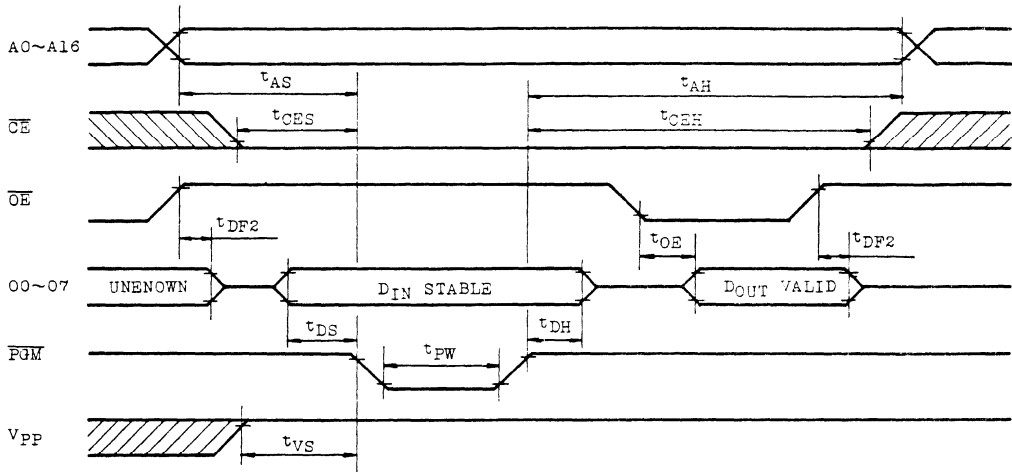
**A.C. TEST CONDITIONS**

- Output Load : 1 TTL Gate and  $C_L$  (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

**TC571000D-20, TC571000D-25**  
**TC571001D-20, TC571001D-25**

HIGH SPEED PROGRAM OPERATION

TIMING CHART



- Note:
1.  $V_{CC}$  must be applied simultaneously or before  $V_{pp}$  and cut off simultaneously or after  $V_{pp}$ .
  2. Removing the device from socket and setting the device in socket with  $V_{pp}=12.75V$  may cause permanent damage to the device.
  3. The  $V_{pp}$  supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the  $V_{pp}$  terminal. When the switching pulse voltage is applied to the  $V_{pp}$  terminal, the overshoot voltage of its pulse should not be exceeded 14V.

**TC571000D-20, TC571000D-25  
TC571001D-20, TC571001D-25**

**ERASURE CHARACTERISTICS**

The TC571000D/571001D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then integrated dose (Ultraviolet light intensity [W/cm<sup>2</sup>] × exposure time [sec.]) for erasure should be a minimum of 15 [W. sec/cm<sup>2</sup>].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1 cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μW/cm<sup>2</sup>] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μW/cm<sup>2</sup>] × (20 × 60) [sec] ≈ 15 [W. sec/cm<sup>2</sup>].)

The TC571000D/TC571001D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals - Toshiba EPROM Protect Seal AC901 - are available.

**OPERATION INFORMATION**

The TC571000D/TC571001D's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

		PC̄M	C̄E	ŌE	V <sub>PP</sub>	V <sub>CC</sub>	Q <sub>0</sub> ~Q <sub>7</sub>	POWER
READ OPERATION (T <sub>a</sub> =-40~85°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (T <sub>a</sub> =25±5°C)	Program	L	L	*	12.75V	6.25V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	
		H	L	H			High Impedance	
	Program Verify	H	L	L			Data Out	

Note: H; V<sub>IH</sub>, L; V<sub>IL</sub>, \*; V<sub>IH</sub> or V<sub>IL</sub>

## TC571000D-20, TC571000D-25 TC571001D-20, TC571001D-25

### READ MODE

The TC571000D/TC571001D has three control functions. The chip enable ( $\overline{CE}$ ) controls the operation power and should be used for device selection.

The output enable ( $\overline{OE}$ ) and the program control ( $\overline{PGM}$ ) control the output buffers, independent of device selection.

Assuming in that  $\overline{CE}=\overline{OE}=V_{IL}$  and  $\overline{PGM}=V_{IH}$ , the output data is valid at the output after address access time from stabilizing of all addresses.

The  $\overline{CE}$  to output valid ( $t_{CE}$ ) is equal to the address access time ( $t_{ACC}$ ).

Assuming that  $\overline{CE}=V_{IL}$ ,  $\overline{PGM}=V_{IH}$  and all addresses are valid, the output data is valid at the outputs after  $t_{OE}$  from the falling edge of  $\overline{OE}$ .

And assuming that  $\overline{CE}=\overline{OE}=V_{IL}$  and all addresses are valid, the output data is valid at the outputs after  $t_{PGM}$  from the rising edge of  $\overline{PGM}$ .

### OUTPUT DESELECT MODE

Assuming that  $\overline{CE}=V_{IH}$  or  $\overline{OE}=V_{IH}$ , the outputs will be in a high impedance state.

So two or more ROMs can be connected together on a common bus line.

When  $\overline{CE}$  is decoded for device selection, all deselected devices are in low power standby mode.

### STANDBY MODE

The TC571000D/TC571001D has a low power standby mode controlled by the  $\overline{CE}$  signal.

By applying a high level to the  $\overline{CE}$  input, the TC571000D/TC571001D is placed in the standby mode which reduce the operating current to 100 $\mu$ A by applying MOS-high level ( $V_{CC}$ ) and then the outputs are in a high impedance state, independent of the  $\overline{OE}$  inputs.

### PROGRAM MODE

Initially, when received by customers, all bits of the TC571000D/TC571001D are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TC571000D/TC571001D can be programmed any location at anytime — either individually, sequentially, or at random.

#### **PROGRAM VERIFY MODE**

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with  $\overline{OE}$  and  $\overline{CE}$  at  $V_{IL}$  and  $\overline{PGM}$  at  $V_{IH}$ .

#### **PROGRAM INHIBIT MODE**

Under the condition that the program voltage (+12.75V) is applied to  $V_{pp}$  terminal, a high level  $\overline{CE}$  or  $\overline{PGM}$  input inhibits the TC571000D/TC571001D from being programmed. Programming of two or more EPROMS in parallel with different data is easily accomplished. That is, all inputs except for  $\overline{CE}$  or  $\overline{PGM}$  may be commonly connected, and a TTL low level program pulse is applied to the  $\overline{CE}$  and  $\overline{PGM}$  of the desired device only and TTL high level signal is applied to the other devices.

#### **HIGH SPEED PROGRAM OPERATION**

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the  $V_{pp}$  terminal with  $V_{CC}=6.25V$  and  $\overline{PGM}=V_{IH}$ .

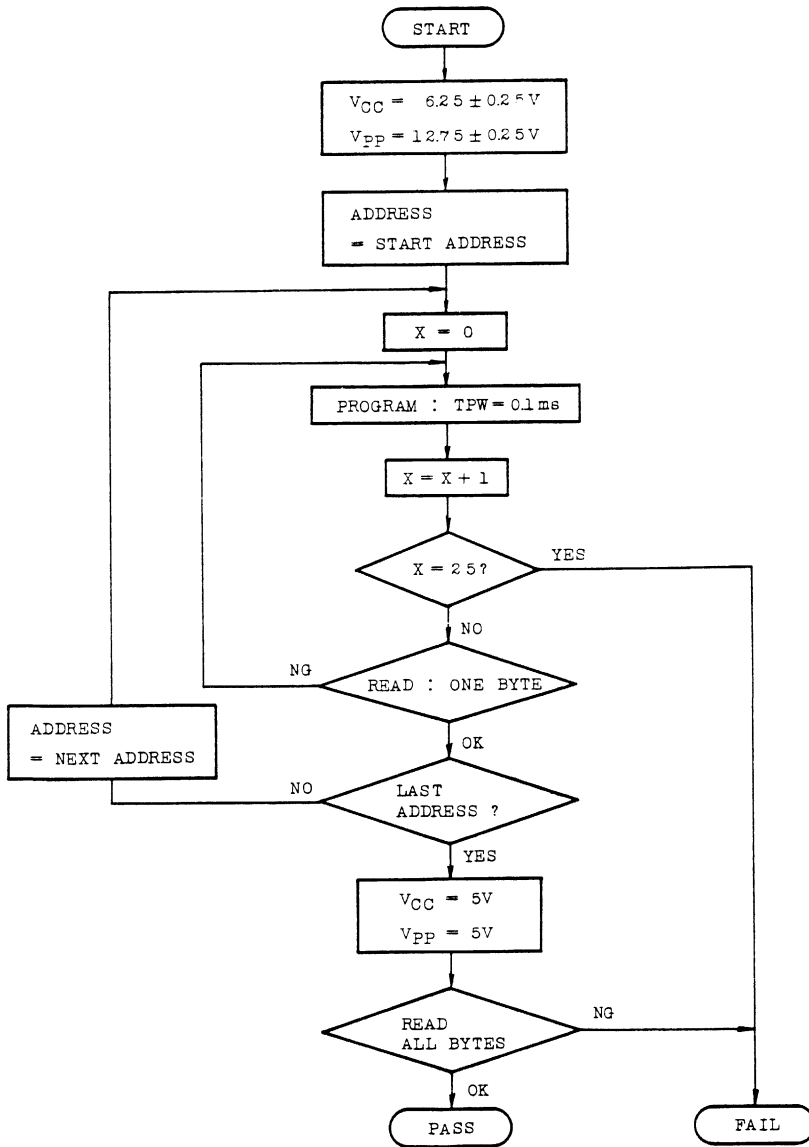
The programming is achieved by applying a single TTL low level 0.1 ms pulse the  $\overline{PGM}$  input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with  $V_{CC}=V_{pp}=5V$ .

**TC571000D-20, TC571000D-25**  
**TC571001D-20, TC571001D-25**

HIGH SPEED PROGRAM OPERATION  
FLOW CHART





**TC571000D-20, TC571000D-25**  
**TC571001D-20, TC571001D-25**

**ELECTRIC SIGNATURE MODE**

Electric signature mode allows to read out a code from TC571000D/TC571001D which identifies it's manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC571000D/TC571001D by using this mode before program operation and automatically set program voltage ( $V_{pp}$ ) and algorithm.

Electric Signature mode is set up when  $12V$  is applied to address line  $A_9$  and the rest of address lines is set to  $V_{IL}$  in read operation. Data output in this conditions is manufacturer code. Device code is identified when address  $A_0$  is set to  $V_{IH}$ . These two codes possess an odd parity with the parity bit of MSB ( $O_7$ ). The following table shows electric signature of TC571000D/TC571001D.

SIGNATURE		PINS									HEX. DATA
		$A_0$	$O_7$	$O_6$	$O_5$	$O_4$	$O_3$	$O_2$	$O_1$	$O_0$	
Manufacture Code		$V_{IL}$	1	0	0	1	1	0	0	0	98
Device Code	TC571000D	$V_{IH}$	1	0	0	0	0	1	1	0	86
	TC571001D		0	0	0	0	0	1	1	1	07

Notes:  $A_9=12V\pm 0.5V$

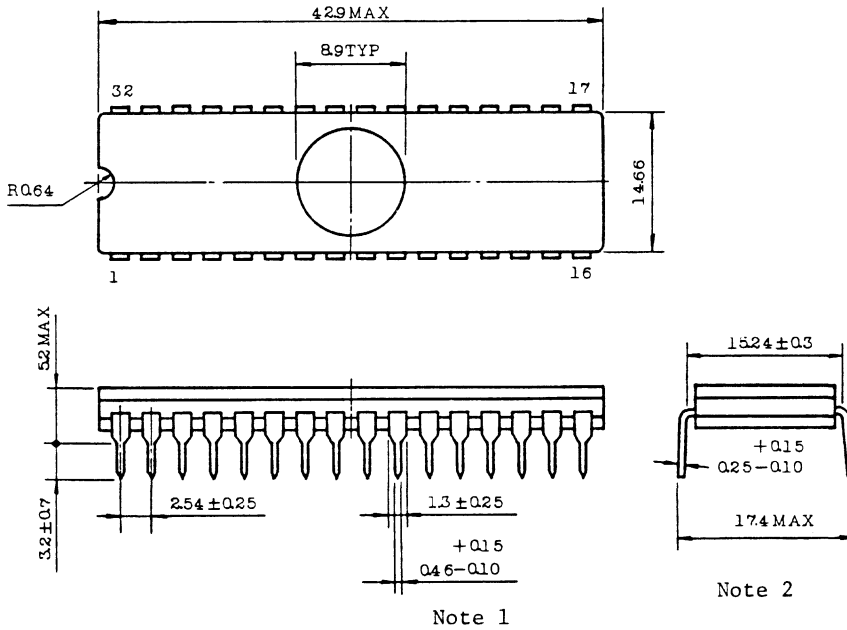
$A_1 \sim A_8, A_{10} \sim A_{16}, \overline{CE}, \overline{OE}=V_{IL}$

$\overline{PGM}=V_{IH}$

**TC571000D-20, TC571000D-25**  
**TC571001D-20, TC571001D-25**

**OUTLINE DRAWINGS**

Unit in mm



Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect NO.1 and No.32 leads.

2. This value is measured at the end of leads.

3. All dimensions are in millimeters.





## HIGH SPEED PROGRAMMING MODE

### FEATURES

The High Speed Programming I or High Speed Programming II Algorithms may be used to program 64K through 512K devices. The 1MEGABIT devices may be programmed using the High Speed Programming II Algorithm.

The High Speed Programming I Algorithm uses 1ms programming pulse and the flow chart is shown in Figure 1.

The High Speed Programming II Algorithm uses 0.1ms programming pulse and the flow chart is shown in Figure 2.

### APPLICABLE DEVICES

Device Name		Theoretical Programming Time	
EPROM	One Time PROM	I	II
TMM2764AD/ADI	TMM2464AP/AF	33 sec	0.8 sec
TMM27128AD/ADI	TMM24128AP/AF	66 sec	1.7 sec
TMM27256AD/ADI	TMM24256AP/AF	131 sec	3.3 sec
TC57256AD	TC54256AP/AF	131 sec	3.3 sec
TMM27512D/DI	TMM24512P	262 sec	7.0 sec
TC571000D	TC541000P	N/A	14 sec
TC571001D	TC541001P	N/A	14 sec

### IDENTIFICATION MODE

The identification mode allows the reading of an electrical signature from the device that will identify the manufacturer and device type. The identification mode is activated using the following conditions:

- For the Manufacturer Code:  
Set  $A_9=12V\pm 0.5V$ ,  $A_\phi=ViL$ , Other Addresses= $ViL$   
Note: The manufacturer code is consistent with the E.I.A. standard.
- For the Device Code:  
Set  $A_9=12V\pm 0.5V$ ,  $A_\phi=ViH$ , Other Addresses= $ViL$ .  
Note: The Device Code is manufacturer dependent.

The following table shows the Electrical Signatures of Toshiba devices.

### ELECTRICAL DEVICES

Device Name		Signature	
EPROM	One Time PROM	Manufacture Code	Device Code
TMM2764AD/ADI	TMM2464AP/AF	98	52
TMM27128AD/ADI	TMM24128AP/AF	98	D3
TMM27256AD/ADI	TMM24256AP/AF	98	54
TC57256AD	TC54256AP/AF	98	C4
TMM27512D/DI	TMM24512P	98	15
TC571000D	TC541000P	98	86
TC571001D	TC541001P	98	07

# TOSHIBA

Figure 1

## HIGH SPEED PROGRAM I FLOW CHART

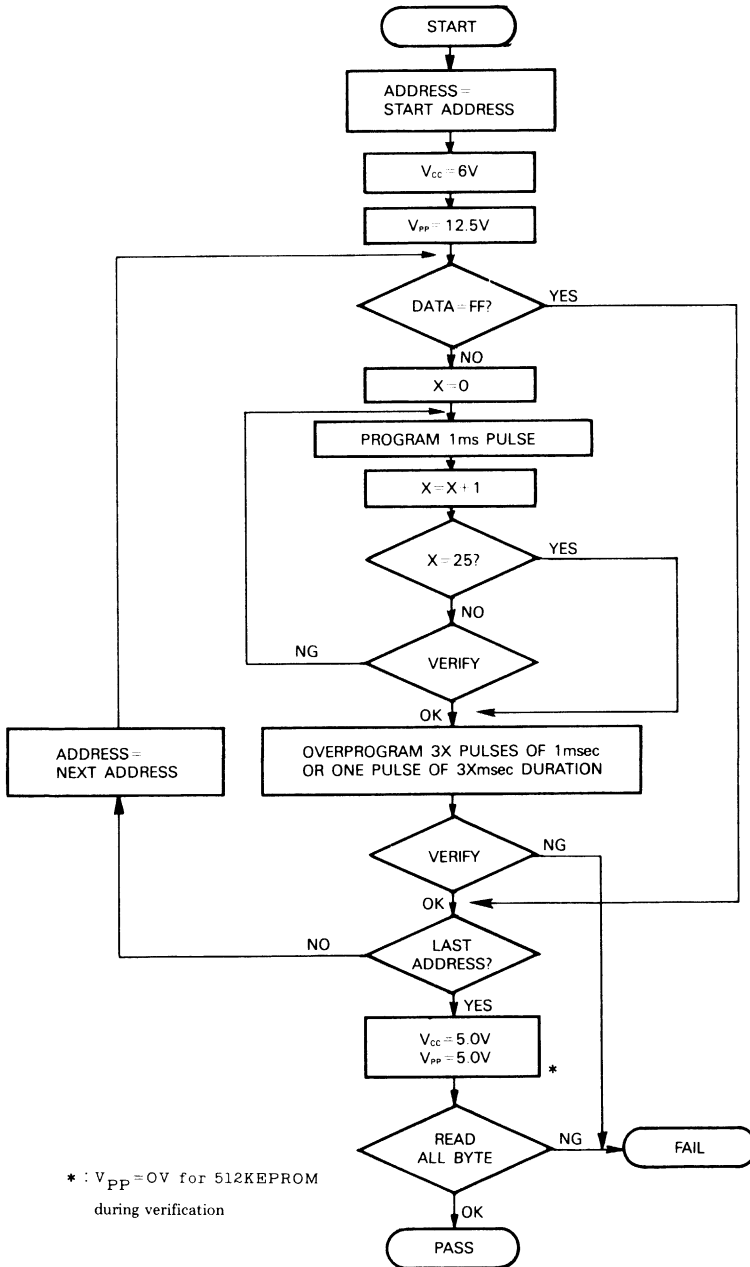
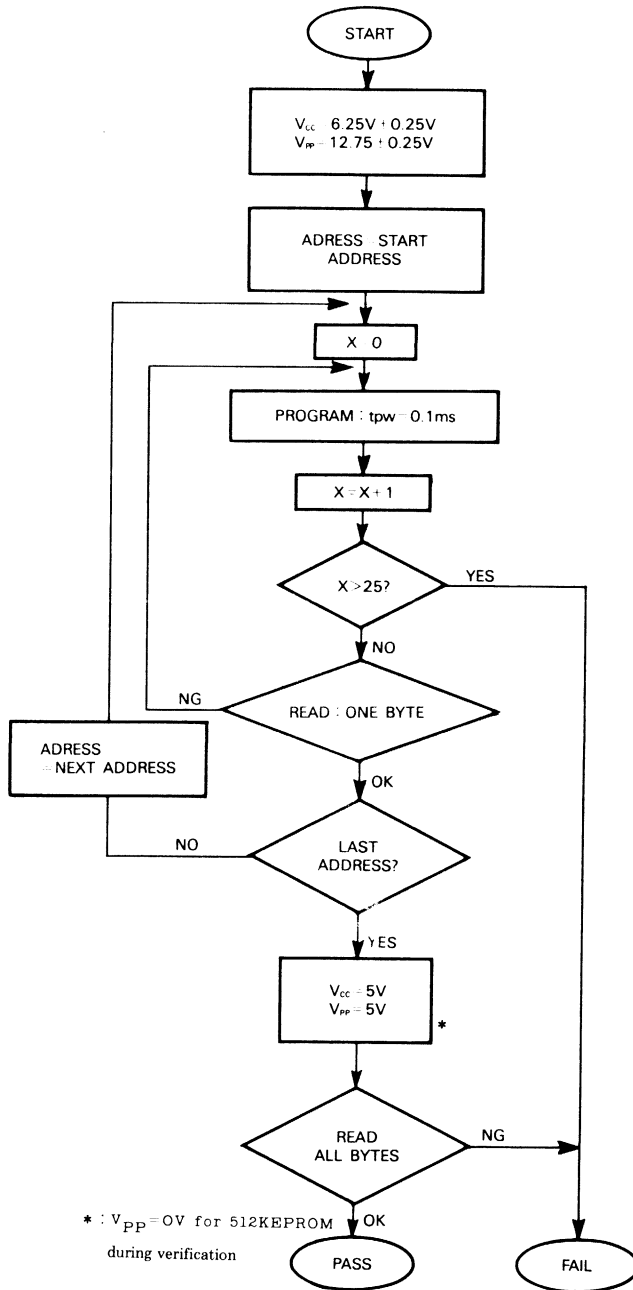


Figure 2

HIGH SPEED PROGRAM II FLOW CHART







# TOSHIBA MOS MEMORY PRODUCT

**TMM2464AP/AF 8,192 WORD × 8 BIT**  
**ONE TIME PROGRAMMABLE READ ONLY MEMORY**  
**N CHANNEL SILICON STACKED GATE MOS**

# TMM2464AP/AF

## DESCRIPTION

The TMM2464AP/AF is a 8,192 word × 8 bit one time programmable read only memory, and molded in a 28 pin plastic DIP.

The TMM2464AP/AF's access time is 200ns, and has low power standby mode which reduces the power dissipation without increasing access time.

The electrical characteristics and programming method are the same as U. V. EPROM TMM-2764AD's.

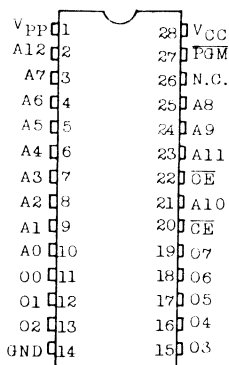
Once programmed, the TMM2464AP/AF can not be erased because of using plastic DIP without transparent window.

## FEATURES

- Single 5 volt power supply
- Fast access time: 200ns (Max.)
- Power dissipation : 100mA(active current) Max.  
: 30mA(standby current) Max.
- Low power standby mode :  $\overline{CE}$
- Output buffer control :  $\overline{OE}$
- Full static operation

- High speed programming mode
- Three state outputs
- Inputs and outputs TTL compatible
- Compatible with TMM2764AD and ROM TMM2365P, TC5365P.
- 28 PIN standard plastic package: TMM2464AP
- 28 PIN flat package : TMM2464AF

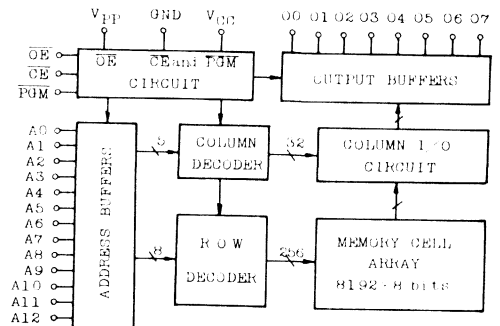
## PIN CONNECTION (TOP VIEW)



## PIN NAMES

$A_0 \sim A_{12}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
PGM	Program Control Input
N.C.	No Connection
$V_{PP}$	Program Supply Voltage
$V_{CC}$	$V_{CC}$ Supply Voltage (+ 5V)
GND	Ground

## BLOCK DIAGRAM



## MODE SELECTION

MODE	PIN	PGM (27)	CE (20)	OE (22)	$V_{PP}$ (1)	$V_{CC}$ (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER	
Read		H	L	L	5V	5V	Data Out	Active	
Output Deselect		*	*	H			High Impedance		
Standby		*	H	*	12.5V	6V	High Impedance	Standby	
Program		L	L	*			Data In		Active
Program Inhibit		*	H	*			High Impedance		
Program Verify		H	L	L	High Impedance	Data Out			

\* H or L.

# TMM2464AP/AF

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
$V_{CC}$	$V_{CC}$ Power Supply Voltage	-0.6~7.0	V
$V_{PP}$	Program Supply Voltage	-0.6~14.0	V
$V_{IN}$	Input Voltage	-0.6~7.0	V
$V_{OUT}$	Output Voltage	-0.6~7.0	V
$P_D$	Power Dissipation	1.5	W
$T_{SOLDER}$	Soldering Temperature · Time	260 · 10	°C·sec
$T_{STRG}$	Storage Temperature	-55~150	°C
$T_{OPR}$	Operating Temperature	0~70	°C

## READ OPERATION

### D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{IH}$	Input High Voltage	2.2	—	$V_{CC} + 1.0$	V
$V_{IL}$	Input Low Voltage	-0.3	—	0.8	
$V_{CC}$	$V_{CC}$ Power Supply Voltage	4.75	5.00	5.25	
$V_{PP}$	$V_{PP}$ Power Supply Voltage	2.2	$V_{CC}$	$V_{CC} + 0.6$	

### D. C. and OPERATING CHARACTERISTICS (Ta=0~70°C, Vcc=5V±5%, Unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$I_{IH}$	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	+10	μA
$I_{CC1}$	Supply Current (Standby)	$\overline{CE} = V_{IH}$	—	—	30	mA
$I_{CC2}$	Supply Current (Active)	$\overline{CE} = V_{IL}$	—	—	100	mA
$V_{OH}$	Output High Voltage	$I_{OH} = -400\mu A$	2.4	—	—	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2.1mA$	—	—	0.4	V
$I_{PP1}$	$V_{PP}$ Current	$V_{PP} = 0 \sim V_{CC} + 0.6V$	—	—	+10	μA
$I_{LO}$	Output Leakage Current	$V_{OUT} = 0.4V \sim V_{CC}$	—	—	+10	μA

# TMM2464AP/AF

## A. C. CHARACTERISTICS

( $T_a = 0 \sim 70^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 5\%$ ,  $V_{OL} = 2.0\text{V} \sim V_{CC} - 0.6\text{V}$ , Unless otherwise noted)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$t_{ACC}$	Address Access Time	—	200	ns
$t_{CE}$	CE to Output Valid	—	200	ns
$t_{OE}$	OE to Output Valid	—	70	ns
$t_{PGM}$	PGM to Output Valid	—	70	ns
$t_{DF1}$	CE to Output in High-Z	0	60	ns
$t_{DF2}$	OE to Output in High-Z	0	60	ns
$t_{DF3}$	PGM to Output in High-Z	0	60	ns
$t_{OH}$	Output Data Hold Time	0	—	ns

### A. C. TEST CONDITIONS

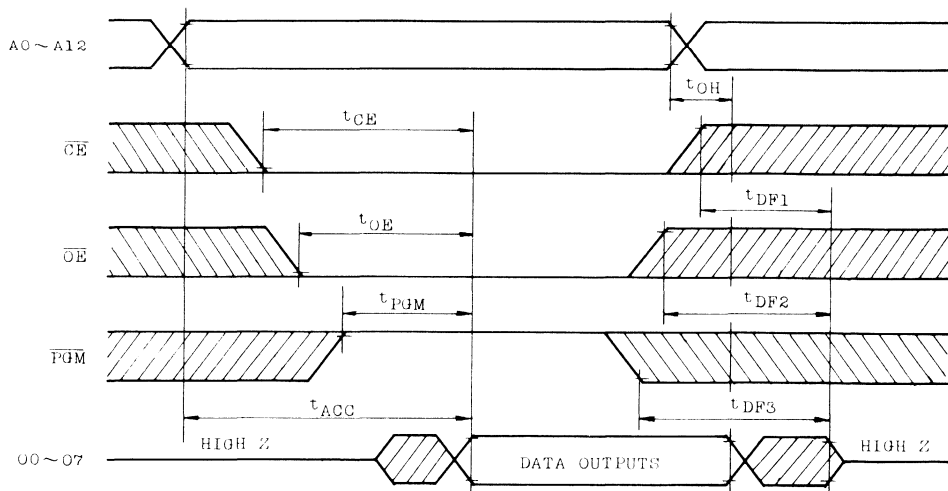
- Output Load : 1 TTL Gate and  $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

### CAPACITANCE \* ( $T_a = 25^\circ\text{C}$ , $f = 1\text{MHz}$ )

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$C_{IN}$	Input Capacitance	$V_{IN} = 0\text{V}$	—	4	6	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0\text{V}$	—	8	12	pF

\* This parameter is periodically sampled and is not 100% tested.

### TIMING WAVEFORMS



# TMM2464AP/AF

## HIGH SPEED PROGRAM OPERATION

### D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.0	—	V <sub>CC</sub> + 1.0	V
V <sub>IL</sub>	Input Low Voltage	0.3	—	0.8	V
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	5.75	6.0	6.25	V
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	12.0	12.5	13.0	V

### D. C. and OPERATING CHARACTERISTICS (T<sub>a</sub> = 25 ± 5°C, V<sub>CC</sub> = 6V ± 0.25V, V<sub>PP</sub> = 12.5V ± 0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>I1</sub>	Input Current	V <sub>IN</sub> = 0 ~ V <sub>CC</sub>	—	—	± 10	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400μA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA	—	—	0.4	V
I <sub>CC</sub>	V <sub>CC</sub> Supply Current	—	—	—	100	mA
I <sub>PP2</sub>	V <sub>PP</sub> Supply Current	V <sub>PP</sub> = 13.0V	—	—	50	mA

### A. C. PROGRAMMING CHARACTERISTICS (T<sub>a</sub> = 25 ± 5°C, V<sub>CC</sub> = 6V ± 0.25V, V<sub>PP</sub> = 12.5V ± 0.5V)

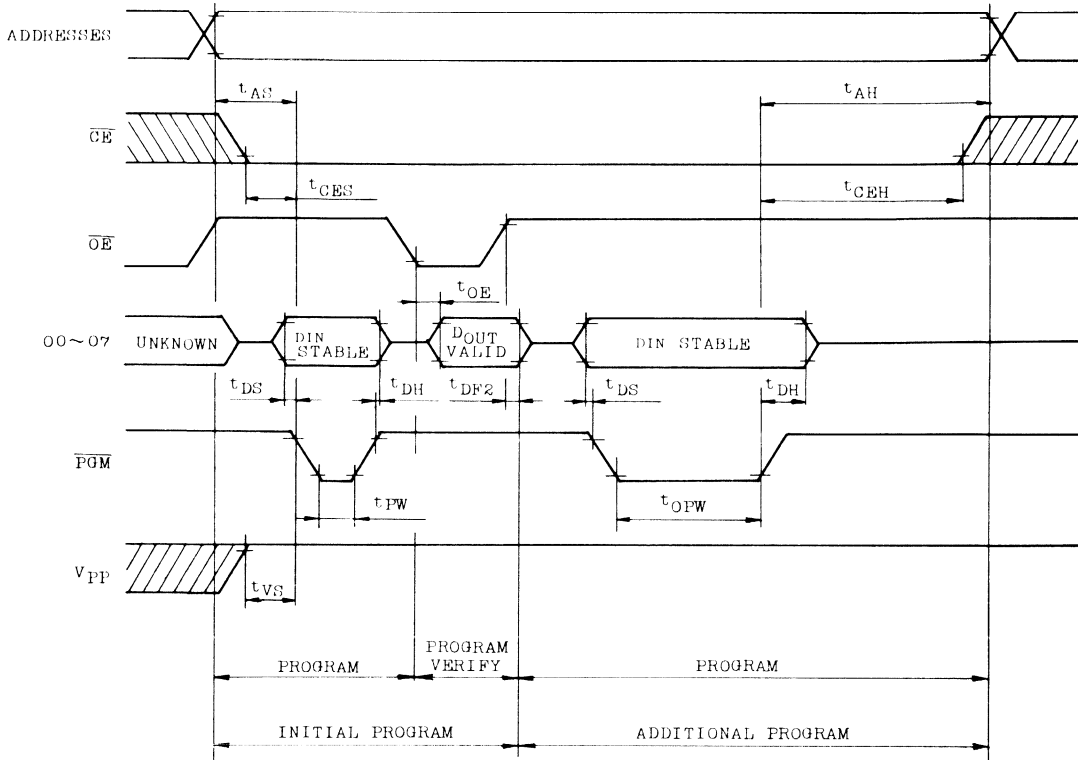
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t <sub>AS</sub>	Address Setup Time	—	2	—	—	μs
t <sub>AH</sub>	Address Hold Time	—	2	—	—	μs
t <sub>CE S</sub>	CE Setup Time	—	2	—	—	μs
t <sub>CE H</sub>	CE Hold Time	—	2	—	—	μs
t <sub>DS</sub>	Data Setup Time	—	2	—	—	μs
t <sub>DH</sub>	Data Hold Time	—	2	—	—	μs
t <sub>VS</sub>	V <sub>PP</sub> Setup Time	—	2	—	—	μs
t <sub>PW</sub>	Program Pulse Width	—	0.95	1.0	1.05	ms
t <sub>OPW</sub>	Additional Program Pulse Width	Note 1	2.85	3.0	78.75	ms
t <sub>of</sub>	OE to Output Valid	—	—	—	100	ns
t <sub>of2</sub>	OE to Output in High-Z	CE = V <sub>IL</sub>	—	—	90	ns

#### A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C<sub>L</sub>(100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note : 1. t<sub>OPW</sub> depend on the program pulse width which is required in the initial program.

## TIMING WAVEFORMS (HIGH SPEED PROGRAM)



- Note :
1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and cut off simultaneously or after  $V_{PP}$ .
  2. Removing the device from socket and setting the device in socket with  $V_{PP} = 12.5V$  may cause permanent damage to the device.
  3. The  $V_{PP}$  supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the  $V_{PP}$  terminal.  
When the switching pulse voltage is applied to the  $V_{PP}$  terminal, the overshoot voltage of its pulse should not be exceeded 14V.

# TMM2464AP/AF

## OPERATION INFORMATION

The TMM2464AP/AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs. In

the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

MODE		PIN NAMES(NUMBER)	PGM (27)	CE (20)	OE (22)	V <sub>PP</sub> (1)	V <sub>CC</sub> (28)	O <sub>0</sub> ~O <sub>7</sub> (11~13, 15~19)	POWER
Read Operation (Ta=0~70°C)	Read		H	L	L	5V	5V	Data Out	Active
	Output Deselect		*	*	H			High Impedance	Active
	Standby		*	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program		L	L	*	12.5V	6V	Data In	Active
	Program Inhibit		*	H	*			High Impedance	Active
	Program Verify		H	L	H			High Impedance	Active
			H	L	L			Data Out	Active

Note : H ; V<sub>IH</sub>, L ; V<sub>IL</sub>, \* ; V<sub>IH</sub> or V<sub>IL</sub>

### READ MODE

The TMM2464AP/AF has three control functions. The chip enable (CE) controls the operation power and should be used for device selection.

The output enable (OE) and the program control (PGM) control the output buffers, independent of device selection.

Assuming that  $\overline{CE} = \overline{OE} = V_{IL}$  and  $\overline{PGM} = V_{IH}$ , the output data is valid at the output after address access time from stabilizing of all addresses.

The  $\overline{CE}$  to output valid ( $t_{CE}$ ) is equal to the address access time ( $t_{ACC}$ ).

Assuming that  $\overline{CE} = V_{IL}$ ,  $\overline{PGM} = V_{IH}$  and all addresses are valid, the output data is valid at the outputs after  $t_{OE}$  from the falling edge of  $\overline{OE}$ .

And assuming that  $\overline{CE} = \overline{OE} = V_{IL}$  and all addresses are valid, the output data is valid at the outputs after  $t_{PGM}$  from the rising edge of  $\overline{PGM}$ .

### OUTPUT DESELECT MODE

Assuming that  $\overline{CE} = V_{IH}$  or  $\overline{OE} = V_{IH}$ , the outputs will be in a high impedance state. So two or more TMM2464AP/AF can be connected together on a

common bus line.

When  $\overline{CE}$  is decoded for device selection, all deselected devices are in low power standby mode.

### STANDBY MODE

The TMM2464AP/AF has a low power standby mode controlled by the CE signal. By applying a TTL high level to the CE input, the TMM2464AP/AF is placed in the standby mode which reduce the oper-

ating current from 100mA to 30mA, and then the outputs are in a high impedance state, independent of the OE and the PGM inputs.

### PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with  $\overline{OE}$  and  $\overline{CE}$  at V<sub>IL</sub> and  $\overline{PGM}$  at V<sub>IH</sub>.

### PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V<sub>PP</sub> terminal, a high level CE or PGM input inhibits the TMM2464AP/AF from being programmed. Programming of two or more TMM2464AP/AF in parallel with different data is

easily accomplished. That is, all inputs except for CE or PGM may be commonly connected, and a TTL low level program pulse is applied to the CE and PGM of the desired device only and TTL high level signal is applied to the other devices.

# TMM2464AP/AF

## HIGH SPEED PROGRAMMING MODE

The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the  $V_{PP}$  terminal with  $V_{CC}=6V$  and  $PGM=V_{IH}$ . The programming is achieved by applying a single TTL low level 1ms pulse the PGM input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then program-

med data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with  $V_{CC}=V_{PP}=5V$ .

## ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM2464AP/AF which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM2464AP/AF by using this mode before program operation and automatically set program voltage ( $V_{PP}$ ) and algorithm.

Electric signature mode is set up when 12V is

applied to address line A9 and the rest of address lines is set to  $V_{IL}$  in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to  $V_{IH}$ . These two codes possess an odd parity with the parity bit of MSB (O7).

The following table shows electric signature of TMM2464AP,AF

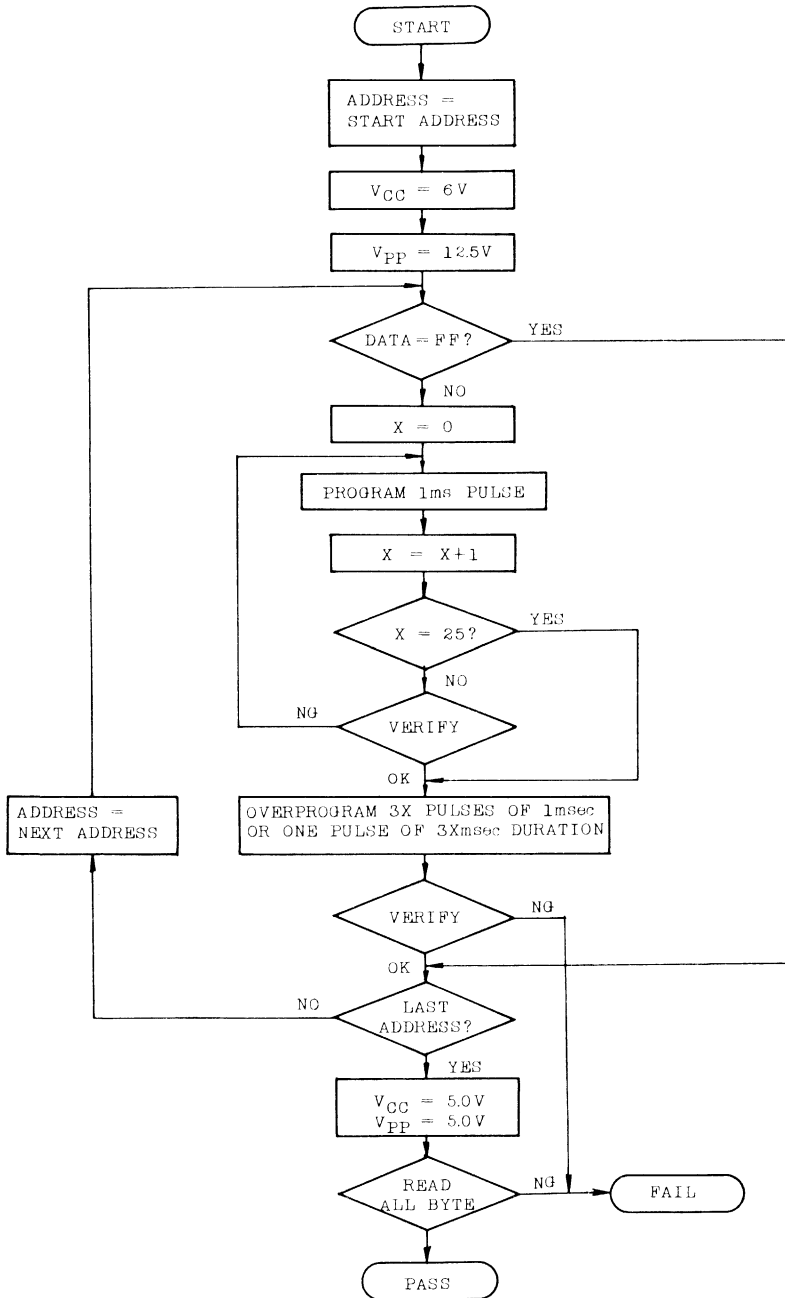
SIGNATURE	PINS	A <sub>0</sub>	O <sub>7</sub>	O <sub>6</sub>	O <sub>5</sub>	O <sub>4</sub>	O <sub>3</sub>	O <sub>2</sub>	O <sub>1</sub>	O <sub>0</sub>	HEX
	(10)	(19)	(18)	(17)	(16)	(15)	(13)	(12)	(11)	DATA	
Manufacture Code	$V_{IL}$	1	0	0	1	1	0	0	0	0	98
Device Code	$V_{IH}$	0	1	0	1	0	0	1	0	0	52

Notes: A9 = 12V ± 0.5V

A1 ~ A8, A10 ~ A12,  $\overline{CE}$ ,  $\overline{OE}$  =  $V_{IL}$  PGM =  $V_{IH}$

# TMM2464AP/AF

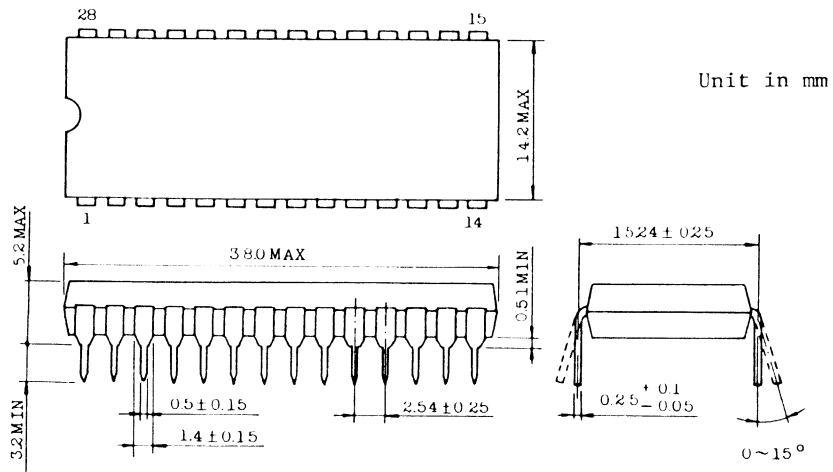
## HIGH SPEED PROGRAM MODE FLOW CHART





# TMM2464AP/AF

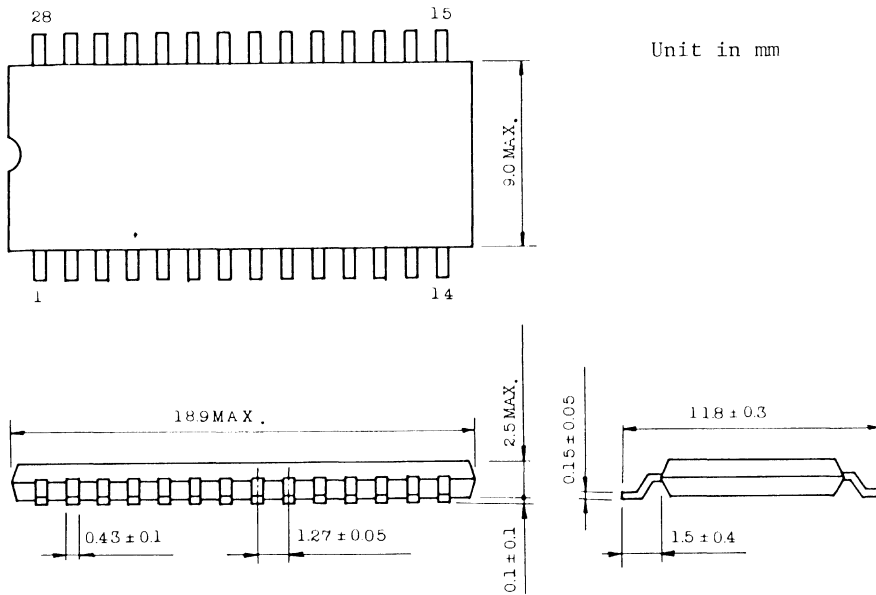
## OUTLINE DRAWINGS (TMM2464AP)



- Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.  
2. This value is measured at the end of leads.  
3. All dimensions are in millimeters.

# TMM2464AP/AF

## OUTLINE DRAWINGS (TMM2464AF)



Note : Lead pitch is 1.27 and tolerance is  $\pm 0.12$  against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.  
• April, 1987 Toshiba Corporation

# TOSHIBA MOS MEMORY PRODUCT

**TMM24128AP/AF 16,384 WORD × 8 BIT**  
**ONE TIME PROGRAMMABLE READ ONLY MEMORY**  
**N CHANNEL SILICON STACKED GATE MOS**

## TMM24128AP/AF

### DESCRIPTION

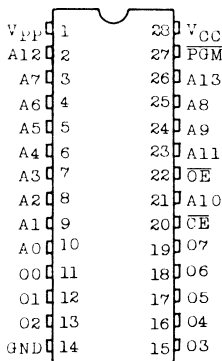
The TMM24128AP/AF is a 16,384 word × 8 bit one time programmable read only memory, and molded in a 28 pin plastic DIP. TMM24128AP/AF's access time is 200ns, and has low power standby mode which reduces the power dissipation without

increasing access time. The electrical characteristics and programming method are the same as U.V. EPROM TMM27128AD's. Once programed, the TMM24128AP/AF can not be erased because of using plastic DIP without transparent window.

### FEATURES

- Single 5 volt power supply
- Fast access time : 200ns(Max.)
- Power dissipation : 100mA(active current) Max.  
30mA(standby current) Max.
- Low power standby mode :  $\overline{CE}$
- Output buffer control :  $\overline{OE}$
- Full static operation
- High speed programming mode
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Compatible with TMM27128AD and MASK ROM TMM23128P
- 28 PIN standard plastic package: TMM24128AP
- 28 PIN flat package : TMM24128AF

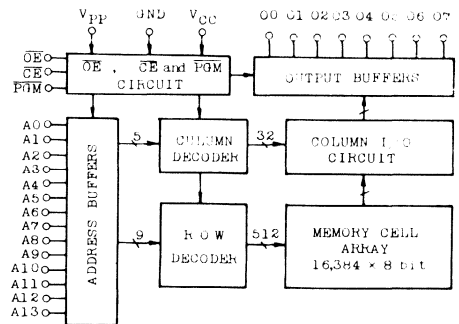
### PIN CONNECTION



### PIN NAMES

$A_0 \sim A_{13}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
PGM	Program Control Input
$V_{PP}$	Program Supply Voltage
$V_{CC}$	$V_{CC}$ Supply Voltage (+5V)
GND	Ground

### BLOCK DIAGRAM



### MODE SELECTION

MODE	PIN	PGM (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$V_{PP}$ (1)	$V_{CC}$ (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read		H	L	L	5V	5V	Data Out	Active
Output Deselect		*	*	H			High Impedance	
Standby		*	H	*			High Impedance	Standby
Program		L	L	*	12.5V	6V	Data In	Active
Program Inhibit		*	H	*			High Impedance	
		H	L	H			High Impedance	
Program Verify		H	L	L			Data Out	

\* H or L

# TMM24128AP/AF

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	-0.6~7.0	V
V <sub>PP</sub>	Program Supply Voltage	-0.6~14.0	V
V <sub>IN</sub>	Input Voltage	-0.6~7.0	V
V <sub>OUT</sub>	Output Voltage	-0.6~7.0	V
P <sub>D</sub>	Power Dissipation	1.5	W
T <sub>SOLDER</sub>	Soldering Temperature · Time	260 · 10	°C·sec
T <sub>STRG</sub>	Storage Temperature	-55~150	°C
T <sub>OPR</sub>	Operating Temperature	0~70	°C

## READ OPERATION

### D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.0	—	V <sub>CC</sub> + 1.0	V
V <sub>IL</sub>	Input Low Voltage	-0.3	—	0.8	V
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	4.75	5.00	5.25	V
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	2.0	V <sub>CC</sub>	V <sub>CC</sub> + 0.6	V

### D. C. and OPERATING CHARACTERISTICS (T<sub>a</sub> = 0~70 °C, V<sub>CC</sub> = 5V ± 5%, Unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>LI</sub>	Input Current	V <sub>IN</sub> = 0~V <sub>CC</sub>	—	—	±10	μA
I <sub>CC1</sub>	Supply Current (Standby)	CE = V <sub>IH</sub>	—	—	30	mA
I <sub>CC2</sub>	Supply Current (Active)	CE = V <sub>IH</sub>	—	—	100	mA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400 μA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA	—	—	0.4	V
I <sub>PP1</sub>	V <sub>PP</sub> Current	V <sub>PP</sub> = 0, V <sub>CC</sub> = 0.6V	—	—	±10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0.4V~V <sub>CC</sub>	—	—	±10	μA

# TMM24128AP/AF

## A. C. CHARACTERISTICS

( $T_a = 0 \sim 70^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 5\%$ ,  $V_{IH} = 2.0\text{V} \sim V_{CC} + 0.6\text{V}$ , Unless otherwise noted)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$t_{ACC}$	Address Access Time	—	200	ns
$t_{CE}$	CE to Output Valid	—	200	ns
$t_{OE}$	OE to Output Valid	—	70	ns
$t_{PGM}$	PGM to Output Valid	—	70	ns
$t_{DF1}$	CE to Output in High-Z	0	60	ns
$t_{DF2}$	OE to Output in High-Z	0	60	ns
$t_{DF3}$	PGM to Output in High-Z	0	60	ns
$t_{OH}$	Output Data Hold Time	0	—	ns

### A. C. TEST CONDITIONS

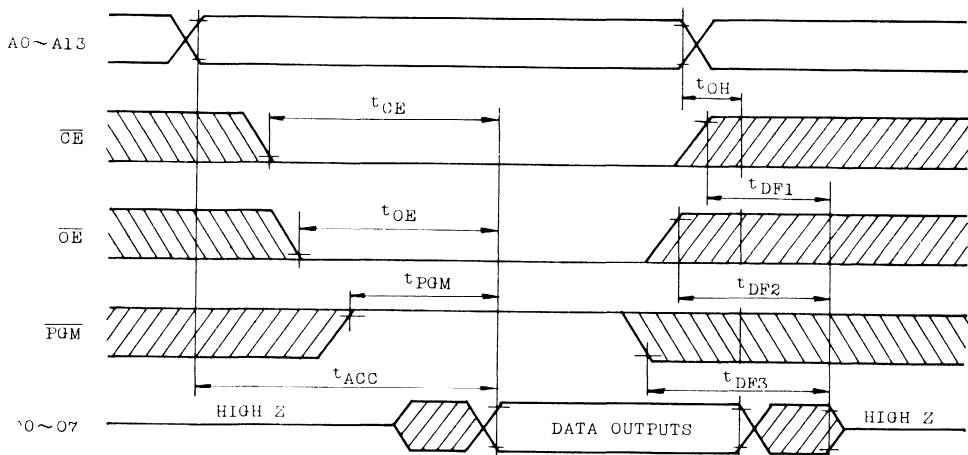
- Output Load : 1 TTL Gate and  $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

### CAPACITANCE \* ( $T_a = 25^\circ\text{C}$ , $f = 1\text{MHz}$ )

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$C_{IN}$	Input Capacitance	$V_{IN} = 0\text{V}$	—	4	6	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0\text{V}$	—	8	12	pF

\* This parameter is periodically sampled and is not 100% tested.

### TIMING WAVEFORMS



# TMM24128AP/AF

## HIGH SPEED PROGRAM OPERATION

### D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{IH}$	Input High Voltage	2.0	—	$V_{CC} + 1.0$	V
$V_{IL}$	Input Low Voltage	-0.3	—	0.8	V
$V_{CC}$	$V_{CC}$ Power Supply Voltage	5.75	6.0	6.25	V
$V_{PP}$	$V_{PP}$ Power Supply Voltage	12.0	12.5	13.0	V

### D. C. and OPERATING CHARACTERISTICS $(T_a = 25 \pm 5^\circ\text{C}, V_{CC} = 6V \pm 0.25V, V_{PP} = 12.5V \pm 0.5V)$

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$I_{IH}$	Input Current	$V_{IN} = 0 \sim V_{CC}$	—	—	$\pm 10$	$\mu\text{A}$
$V_{OH}$	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
$I_{CC}$	$V_{CC}$ Supply Current	—	—	—	100	mA
$I_{PP}$	$V_{PP}$ Supply Current	$V_{PP} = 13.0V$	—	—	50	mA

### A. C. PROGRAMMING CHARACTERISTICS $(T_a = 25 \pm 5^\circ\text{C}, V_{CC} = 6V \pm 0.25V, V_{PP} = 12.5V \pm 0.5V)$

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$t_{AS}$	Address Setup Time	—	2	—	—	$\mu\text{s}$
$t_{AH}$	Address Hold Time	—	2	—	—	$\mu\text{s}$
$t_{CES}$	$\overline{\text{CE}}$ Setup Time	—	2	—	—	$\mu\text{s}$
$t_{CEH}$	$\overline{\text{CE}}$ Hold Time	—	2	—	—	$\mu\text{s}$
$t_{DS}$	Data Setup Time	—	2	—	—	$\mu\text{s}$
$t_{DH}$	Data Hold Time	—	2	—	—	$\mu\text{s}$
$t_{VS}$	$V_{PP}$ Setup Time	—	2	—	—	$\mu\text{s}$
$t_{PW}$	Program Pulse Width	—	0.95	1.0	1.05	ms
$t_{OPW}$	Additional Program Pulse Width	Note 1	2.85	3.0	78.75	ms
$t_{OE}$	$\overline{\text{OE}}$ to Output Valid	—	—	—	100	ns
$t_{DFZ}$	$\overline{\text{OE}}$ to Output in High-Z	$\overline{\text{CE}} = V_{IL}$	—	—	90	ns

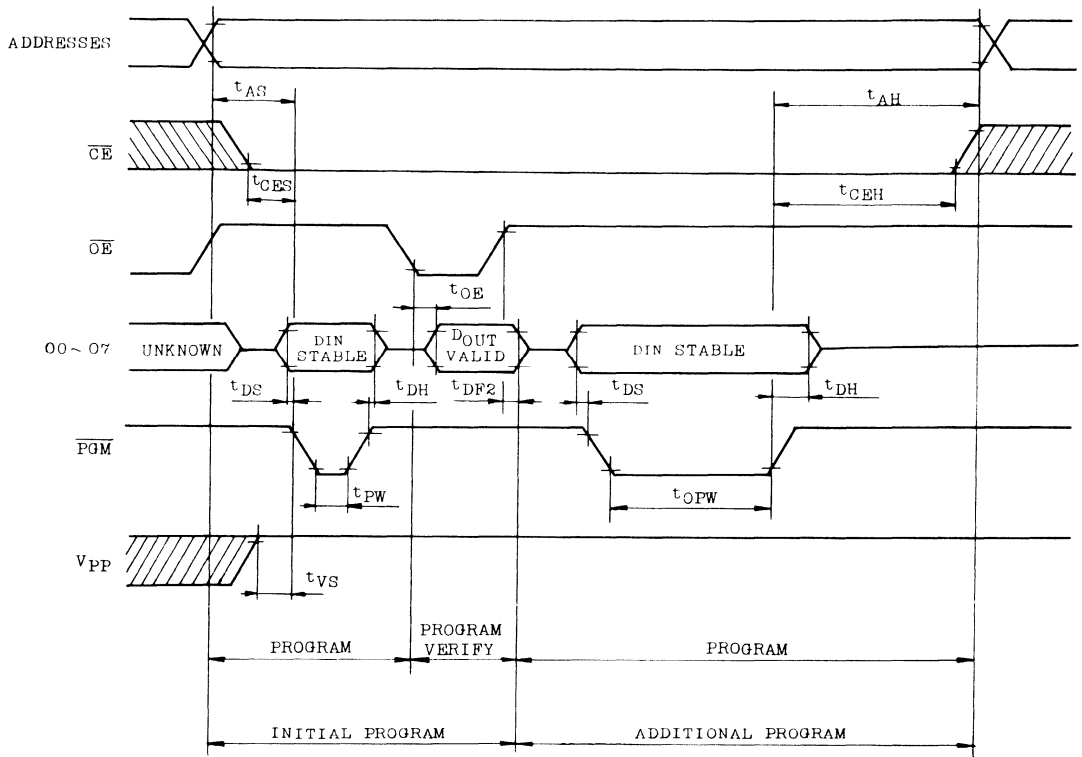
#### A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and  $C_L(100\text{pF})$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note : 1.  $t_{OPW}$  depend on the program pulse width which is required in the initial program.

# TMM24128AP/AF

## TIMING WAVEFORMS (HIGH SPEED PROGRAM)



- Note :
1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and cut off simultaneously or after  $V_{PP}$ .
  2. Removing the device from socket and setting the device in socket with  $V_{PP}=12.5V$  may cause permanent damage to the device.
  3. The  $V_{PP}$  supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the  $V_{PP}$  terminal.  
When the switching pulse voltage is applied to the  $V_{PP}$  terminal, the overshoot voltage of its pulse should not be exceeded 14V.

# TMM24128AP/AF

## OPERATION INFORMATION

The TMM24128AP/AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

MODE		PIN NAMES(NUMBER)	PGM (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$V_{PP}$ (1)	$V_{CC}$ (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read Operation ( $T_a = 0 \sim 70^\circ\text{C}$ )	Read		H	L	L	5V	5V	Data Out	Active
	Output Deselect		*	*	H			High Impedance	Active
	Standby		*	H	*			High Impedance	Standby
Program Operation ( $T_a = 25 \pm 5^\circ\text{C}$ )	Program		L	L	*	12.5V	6V	Data In	Active
	Program Inhibit		*	H	*			High Impedance	Active
			H	L	H			High Impedance	Active
	Program Verify		H	L	L			Data Out	Active

Note : H :  $V_{IH}$ , L :  $V_{IL}$ , \* :  $V_{IH}$  or  $V_{IL}$

### READ MODE

The TMM24128AP/AF has three control functions. The chip enable ( $\overline{CE}$ ) controls the operation power and should be used for device selection.

The output enable ( $\overline{OE}$ ) and the program control ( $\overline{PGM}$ ) control the output buffers, independent of device selection.

Assuming that  $\overline{CE} = \overline{OE} = V_{LL}$  and  $\overline{PGM} = V_{IH}$ , the output data is valid at the output after address access time from stabilizing of all addresses.

The  $\overline{CE}$  to output valid ( $t_{CE}$ ) is equal to the address access time ( $t_{ACC}$ ).

Assuming that  $\overline{CE} = V_{LL}$ ,  $\overline{PGM} = V_{IH}$  and all addresses are valid, the output data is valid at the outputs after  $t_{OE}$  from the falling edge of  $\overline{OE}$ .

And assuming that  $\overline{CE} = \overline{OE} = V_{IL}$  and addresses are valid, the output data is valid at the outputs after  $t_{PGM}$  from the rising edge of  $\overline{PGM}$ .

### OUTPUT Deselect MODE

Assuming that  $\overline{CE} = V_{IH}$  or  $\overline{OE} = V_{IH}$ , the outputs will be in a high impedance state. So two or more TMM24128AP/AF can be connected together on a

common bus line.

When  $\overline{CE}$  is decoded for device selection, all deselected devices are in low power standby mode.

### STANDBY MODE

The TMM24128AP/AF has a low power standby mode controlled by the  $\overline{CE}$  signal. By applying TTL high level to the  $\overline{CE}$  input, the TMM24128AP/AF is placed in the standby mode which reduce the oper-

ating current from 100mA to 30mA, and then the outputs are in a high impedance state, independent of the  $\overline{OE}$  and the  $\overline{PGM}$  inputs.

### PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with  $\overline{OE}$  and  $\overline{CE}$  at  $V_{IL}$  and  $\overline{PGM}$  at  $V_{IH}$ .

### PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to  $V_{PP}$  terminal, a high level  $\overline{CE}$  or  $\overline{PGM}$  input inhibits the TMM24128AP/AF from being programmed. Programming of two or more TMM24128AP/AF in parallel with different data is

easily accomplished. That is, all inputs except for  $\overline{CE}$  or  $\overline{PGM}$  may be commonly connected, and a TTL low level program pulse is applied to the  $\overline{CE}$  and  $\overline{PGM}$  of the desired device only and TTL high level signal is applied to the other devices.



# TMM24128AP/AF

## HIGH SPEED PROGRAMMING MODE

The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the  $V_{PP}$  terminal with  $V_{CC}=6V$  and  $\overline{PGM}=V_{IH}$ . The programming is achieved by applying a single TTL low level 1ms pulse the  $\overline{PGM}$  input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then pro-

grammed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with  $V_{CC}=V_{PP}=5V$ .

## ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM24128AP/AF which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM24128AP/AF by using this mode before program operation and automatically set program voltage ( $V_{PP}$ ) and algorithm.

Electric signature mode is set up when 12V is

applied to address line A9 and the rest of address lines is set to  $V_{IL}$  in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to  $V_{IH}$ . These two codes possess an odd parity with the parity bit of MSB (O7).

The following table shows electric signature of TMM24128AP/AF.

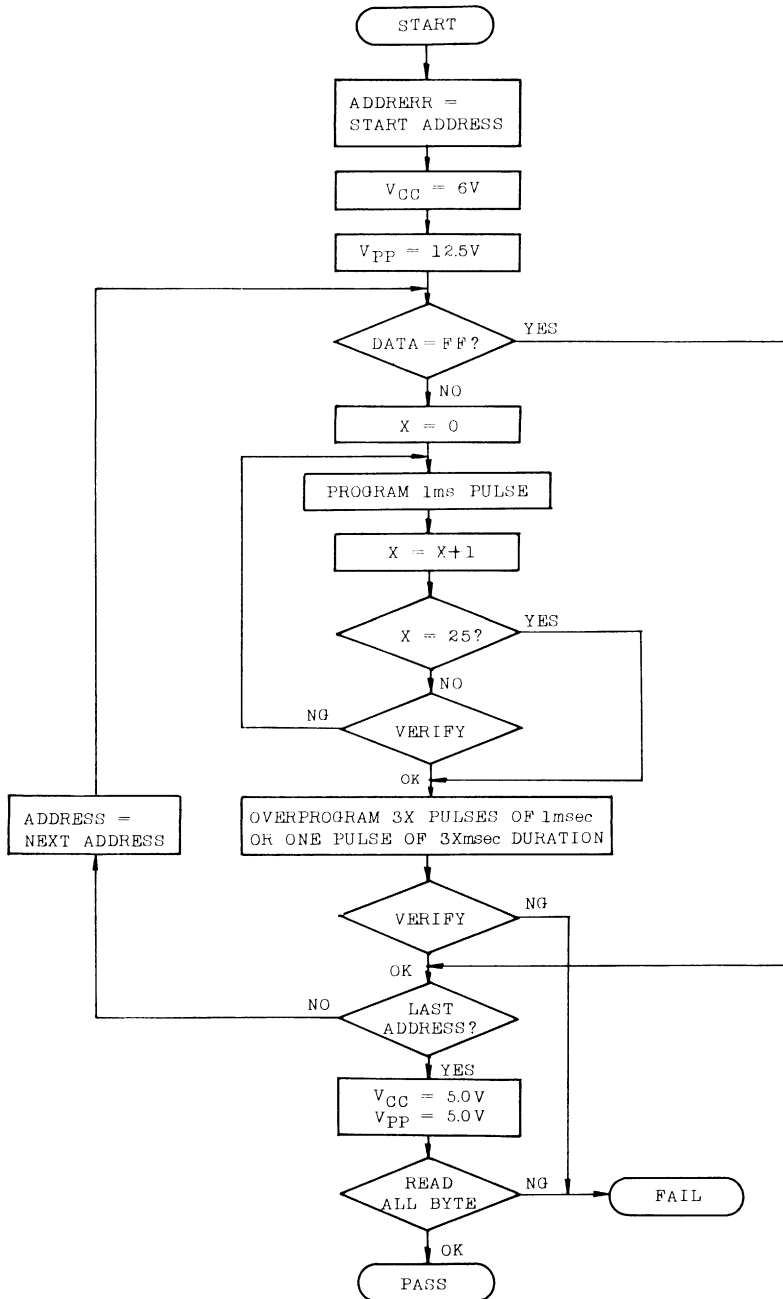
SIGNATURE	PINS	A <sub>9</sub> (10)	O <sub>7</sub> (19)	O <sub>6</sub> (18)	O <sub>5</sub> (17)	O <sub>4</sub> (16)	O <sub>3</sub> (15)	O <sub>2</sub> (13)	O <sub>1</sub> (12)	O <sub>0</sub> (11)	HEX. DATA
Manufacture Code	$V_{IL}$	1	0	0	1	1	0	0	0	0	98
Device Code	$V_{IH}$	1	1	0	1	0	0	0	1	1	D3

Notes: A9=12V±0.5V

A1~A8, A10~A13,  $\overline{CE}$ ,  $\overline{OE}=V_{IL}$ ,  $\overline{PGM}=V_{IH}$

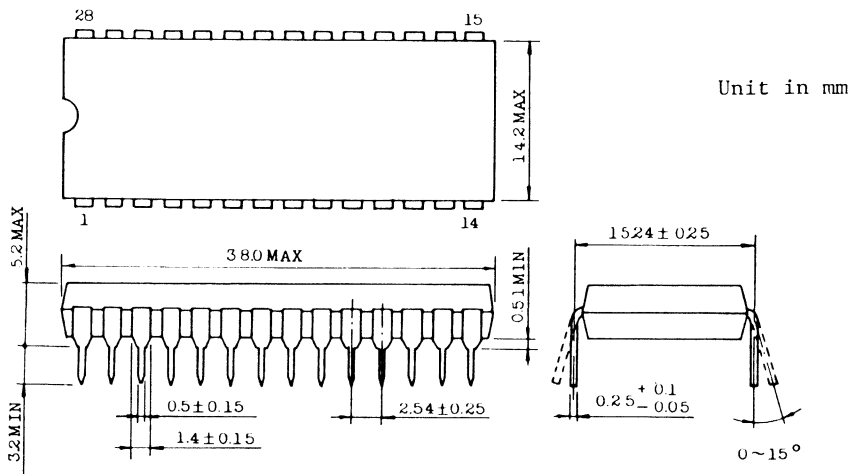
# TMM24128AP/AF

## HIGH SPEED PROGRAM MODE FLOW CHART



# TMM24128AP/AF

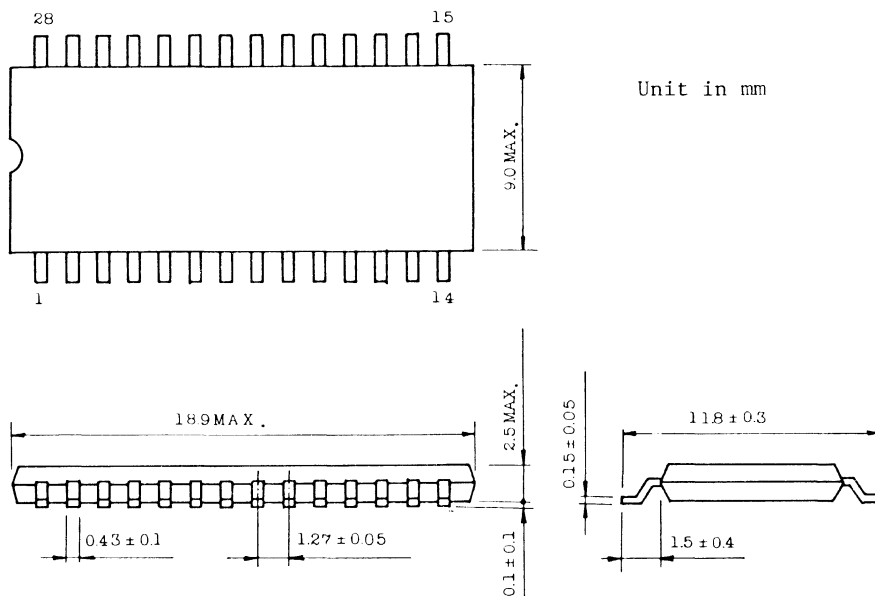
## OUTLINE DRAWINGS (TMM24128AP)



- Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.  
2. This value is measured at the end of leads.  
3. All dimensions are in millimeters.

# TMM24128AP/AF

## OUTLINE DRAWINGS (TMM24128AF)



Note: Lead pitch is 1.27 and tolerance is  $\pm 0.12$  against theoretical center of each lead that is obtained on the basis of No. 1 and No. 28 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.  
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# TOSHIBA MOS MEMORY PRODUCT

**TMM24256AP/AF 32,768 WORD × 8 BIT**  
**ONE TIME PROGRAMMABLE READ ONLY MEMORY**  
**SILICON STACKED GATE MOS**

## TMM24256AP/AF

### DESCRIPTION

The TMM24256AP/AF is a 32,768 word × 8 bit one time programmable read only memory, and molded in a 28 pin plastic Package.

The TMM24256AP/AF's access time is 200ns and has low power standby mode which reduces the power dissipation without increasing access time.

### FEATURES

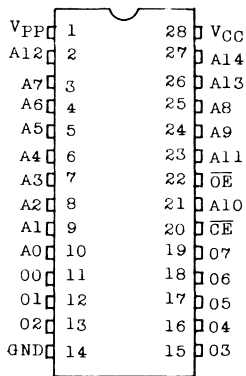
- Fast access time : 200ns
- Low power dissipation  
Active : 100mA  
Standby : 30mA
- Single 5V power supply
- Full static operation
- High speed programming mode

The electrical characteristics and programming method are the same as U.V. EPROM TMM27256AD's.

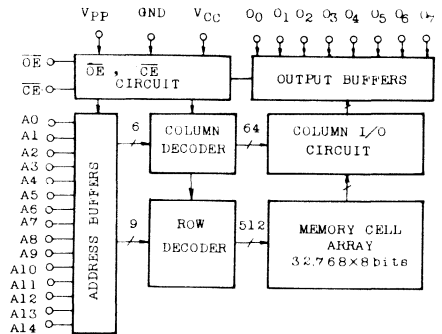
Once programmed, the TMM24128AP/AF can not be erased because of using plastic DIP without transparent window.

- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, EPROM TMM27256D/AD and TC57256D
- Standard 28 pin DIP plastic package : TMM24256AP
- Plastic Flat Package : TMM24256AF

### PIN CONNECTION



### BLOCK DIAGRAM



### MODE SELECTION

MODE \ PIN	CE (20)	OE (22)	V <sub>PP</sub> (1)	V <sub>CC</sub> (28)	O <sub>0</sub> ~O <sub>7</sub> (11~13, 15~19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V	6V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

\* H or L

### PIN NAMES

A <sub>0</sub> ~A <sub>14</sub>	Address Inputs
O <sub>0</sub> ~O <sub>7</sub>	Outputs (Inputs)
CE	Chip Enable Input
OE	Output Enable Input
V <sub>PP</sub>	Program Supply Voltage
V <sub>CC</sub>	V <sub>CC</sub> Supply Voltage (+5V)
GND	Ground

# TC54256AP/AF

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	-0.6~7.0	V
V <sub>PP</sub>	Program Supply Voltage	-0.6~14.0	V
V <sub>IN</sub>	Input Voltage	-0.6~7.0	V
V <sub>OUT</sub>	Output Voltage	-0.6~7.0	V
P <sub>D</sub>	Power Dissipation	1.5	W
T <sub>SOLDER</sub>	Soldering Temperature · Time	260 · 10	°C·sec
T <sub>STG</sub>	Storage Temperature	-55~150	°C
T <sub>OPR</sub>	Operating Temperature	0~70	°C

## READ OPERATION

### D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.0	—	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input Low Voltage	-0.3	—	0.8	V
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	4.75	5.00	5.25	V
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	2.0	V <sub>CC</sub>	V <sub>CC</sub> +0.6	V

### D. C. and OPERATING CHARACTERISTICS (Ta=0~70°C, V<sub>CC</sub>=5V±5%.)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>LI</sub>	Input Current	V <sub>IN</sub> =0~V <sub>CC</sub>	—	—	±10	μA
I <sub>CC1</sub>	Supply Current (Standby)	$\overline{CE}=V_{IH}$	—	—	30	mA
I <sub>CC2</sub>	Supply Current (Active)	$\overline{CE}=V_{IL}$	—	—	100	mA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> =-400μA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> =2.1mA	—	—	0.4	V
I <sub>PP1</sub>	V <sub>PP</sub> Current	V <sub>PP</sub> =0~V <sub>CC</sub> +0.6V	—	—	±10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> =0.4V~V <sub>CC</sub>	—	—	±10	μA

# TMM24256AP/AF

## A. C. CHARACTERISTICS

( $T_a = 0 \sim 70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$ ,  $V_{FP} = 2.0V - V_{CC} + 0.6V$ )

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
$t_{ACC}$	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	—	200	ns
$t_{CF}$	CE to Output Valid	$\overline{OE} = V_{IL}$	—	200	ns
$t_{OE}$	OE to Output Valid	$\overline{CE} = V_{IL}$	—	70	ns
$t_{DF1}$	CE to Output in High-Z	$\overline{OE} = V_{IL}$	0	60	ns
$t_{DF2}$	OE to Output in High-Z	$\overline{CE} = V_{IL}$	0	60	ns
$t_{OH}$	Output Data Hold Time	$\overline{CE} = \overline{OE} = V_{IL}$	0	—	ns

### A. C. TEST CONDITIONS

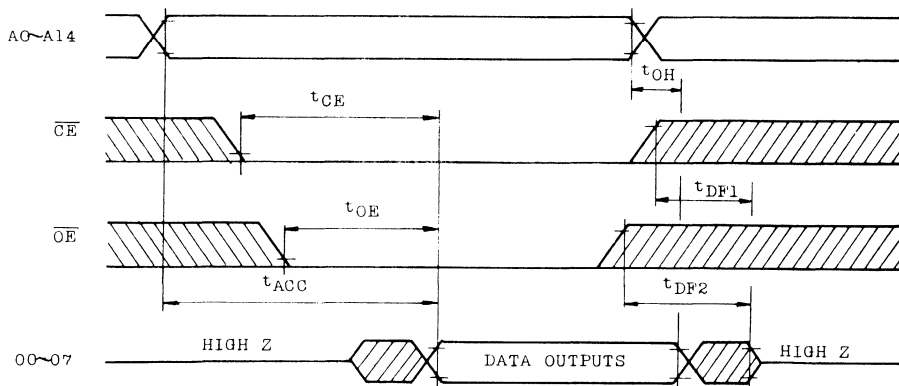
- Output Load : 1 TTL Gate and  $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

### CAPACITANCE \* ( $T_a = 25^\circ\text{C}$ , $f = 1\text{MHz}$ )

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	—	4	6	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V$	—	8	12	pF

\* This parameter is periodically sampled and is not 100% tested.

### TIMING WAVEFORMS (READ)



# TMM24256AP/AF

## High speed PROGRAM OPERATION

### D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.0		V <sub>CC</sub> + 1.0	V
V <sub>IL</sub>	Input Low Voltage	-0.3		0.8	V
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	5.75	6.0	6.25	V
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	12.0	12.5	13.0	V

### D. C. and OPERATING CHARACTERISTICS (T<sub>a</sub> = 25±5°C, V<sub>CC</sub> = 6V±0.25V, V<sub>PP</sub> = 12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>IH</sub>	Input Current	V <sub>IN</sub> = 0 - V <sub>CC</sub>	---	---	+10	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400μA	2.4	---	---	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA	---	---	0.4	V
I <sub>CC</sub>	V <sub>CC</sub> Supply Current	---	---	---	120	mA
I <sub>PP2</sub>	V <sub>PP</sub> Supply Current	V <sub>PP</sub> = 13.0V	---	---	50	mA
V <sub>ID</sub>	A <sub>9</sub> Auto Select Voltage	---	11.5	12.0	12.5	V

### A. C. PROGRAMMING CHARACTERISTICS (T<sub>a</sub> = 25±5°C, V<sub>CC</sub> = 6V±0.25V, V<sub>PP</sub> = 12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t <sub>AS</sub>	Address Setup Time	---	2	---	---	μS
t <sub>AH</sub>	Address Hold Time	---	2	---	---	μS
t <sub>CE S</sub>	CE Setup Time	---	0	---	---	ns
t <sub>CE H</sub>	CE Hold Time	---	0	---	---	ns
t <sub>OE S</sub>	OE Setup Time	---	2	---	---	μS
t <sub>DS</sub>	Data Setup Time	---	2	---	---	μS
t <sub>DH</sub>	Data Hold Time	---	2	---	---	μS
t <sub>VPS</sub>	V <sub>PP</sub> Setup Time	---	2	---	---	μS
t <sub>VCS</sub>	V <sub>CC</sub> Setup Time	---	2	---	---	μS
t <sub>PW</sub>	Initial Program Pulse Width	CE = V <sub>IL</sub> , OE = V <sub>IH</sub>	0.95	1.0	1.05	ms
t <sub>OPW</sub>	Overprogram Pulse Width	Note 1	2.85	3.0	78.75	ms
t <sub>OZ</sub>	OE to Output Valid	CE = V <sub>IH</sub>	---	---	150	ns
t <sub>OH</sub>	OE to Output in High-Z	CE = V <sub>IH</sub>	---	---	130	ns

#### A. C. TEST CONDITIONS

- Output load : 1 TTL Gate and C<sub>L</sub>(100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

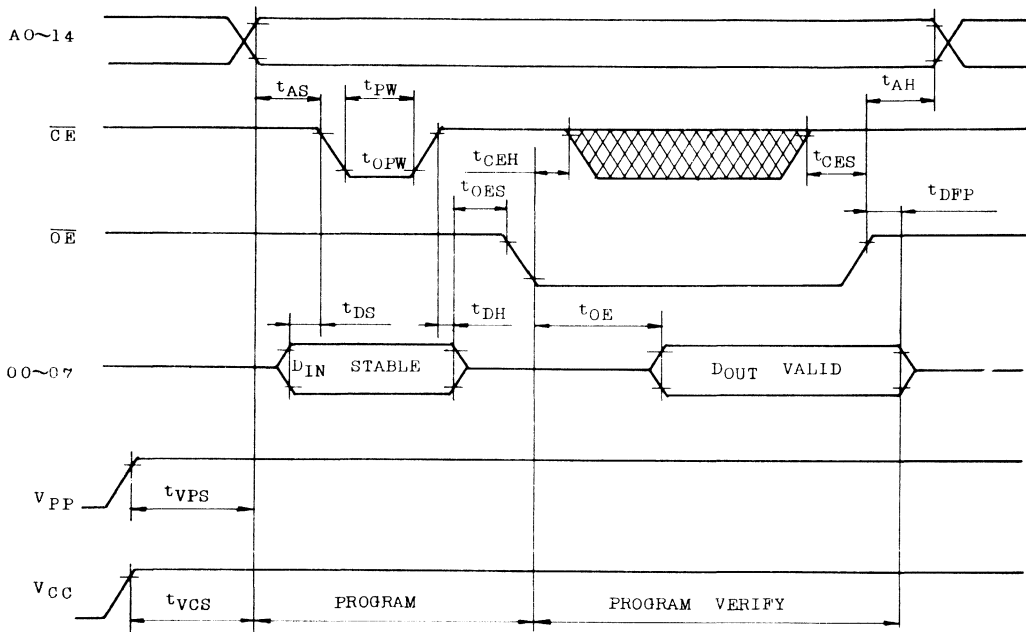
Note 1 : The length of the overprogram pulse may vary as a function of the counter value X.



# TMM24256AP/AF

## TIMING WAVEFORMS(PROGRAM)

( $V_{CC} = 6V \pm 0.25V$ ,  $V_{PP} = 12.5V \pm 0.5V$ )



- Note :
1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and cut off simultaneously or after  $V_{PP}$ .
  2. Removing the device from socket and setting the device in socket with  $V_{PP} = 12.5V$  may cause permanent damage to the device.
  3. The  $V_{PP}$  supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the  $V_{PP}$  terminal.  
When the switching pulse voltage is applied to the  $V_{PP}$  terminal, the overshoot voltage of its pulse should not be exceeded 14V.

# TMM24256AP/AF

## OPERATION INFORMATION

The TMM24256AP/AF's six operation modes are listed in the following table. Mode selection can be

achieved by applying TTL level signal to all inputs.

MODE		PIN NAMES(NUMBER)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$V_{PP}$ (1)	$V_{CC}$ (28)	$O_6 \sim O_7$ (11~13, 15~19)	POWER
Read Operation ( $T_a = 0 \sim 70^\circ\text{C}$ )	Read		L	L	5V	5V	Data Out	Active
	Output Deselect		*	H			High Impedance	Active
	Standby		H	*			High Impedance	Standby
Program Operation ( $T_a = 25 \pm 5^\circ\text{C}$ )	Program		L	H	12.5V	6V	Data In	Active
	Program Inhibit		H	H			High Impedance	Active
	Program Verify		*	L			Data Out	Active

Note : H ;  $V_{IH}$ , L ;  $V_{IL}$ , \* ;  $V_{IH}$  or  $V_{IL}$

### READ MODE

The TMM24256AP/AF has two control functions. The chip enable ( $\overline{CE}$ ) controls the operation power and should be used for device selection.

The output enable ( $\overline{OE}$ ) control the output buffers, independent of device selection.

Assuming the  $\overline{CE} = \overline{OE} = V_{IL}$ , the output data is valid at the outputs after address access time from

stabilizing of all addresses.

The  $\overline{CE}$  to output valid ( $t_{CE}$ ) is equal to the address access time ( $t_{ACC}$ ).

Assuming that  $\overline{CE} = V_{IL}$  and all addresses are valid, the output data is valid at the outputs after  $t_{OE}$  from the falling edge of  $\overline{OE}$ .

### OUTPUT Deselect MODE

Assuming that  $\overline{CE} = V_{IH}$  or  $\overline{OE} = V_{IH}$ , the outputs will be in a high impedance state. So two or more TMM24256AP/AF's can be connected together on a

common bus line.

When  $\overline{CE}$  is decoded for device selection, all deselected devices are in low power standby mode.

### STANDBY MODE

The TMM24256AP/AF has a low power standby mode controlled by the  $\overline{CE}$  signal. By applying a high level to the  $\overline{CE}$  input, the TMM24256AP/AF is placed in the standby mode which reduce the oper-

ating current to 30mA from 100mA (about 70% reduction) and then the outputs are in a high impedance state, independent of the  $\overline{OE}$  inputs.

### PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with  $\overline{OE}$  at  $V_{IL}$  and  $\overline{CE}$  at  $V_{IH}$  or  $V_{IL}$ .

### PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to  $V_{PP}$  terminal, a TTL high level  $\overline{CE}$  input inhibits the TMM24256AP/AF from being programmed.

Programming of two or more TMM24256AP/AF's in parallel with different data is easily accom-

plished. That is, all inputs except for  $\overline{CE}$  and  $\overline{OE}$  may be commonly connected, and a TTL low level program pulse is applied to the  $\overline{CE}$  of the desired device only and TTL high level signal is applied to the other devices.

# TMM24256AP/AF

## HIGH SPEED PROGRAMMING MODE

The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the  $V_{PP}$  terminal with  $V_{CC}=6V$ .

The programming is achieved by applying a single TTL low level 1ms pulse the  $\overline{CE}$  input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then pro-

grammed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width equal to that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with  $V_{CC}=V_{PP}=5V$ .

## ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM24256AP/AF which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM24256AP/AF by using this mode before program operation and automatically set program voltage ( $V_{PP}$ ) and algorithm.

Electric Signature mode is set up when 12V is

applied to address line A9 and the rest of address lines is set to  $V_{IL}$  in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to  $V_{IH}$ . These two codes possess an odd parity with the parity bit of MSB (O7).

The following table shows electric signature of TMM24256AP/AF.

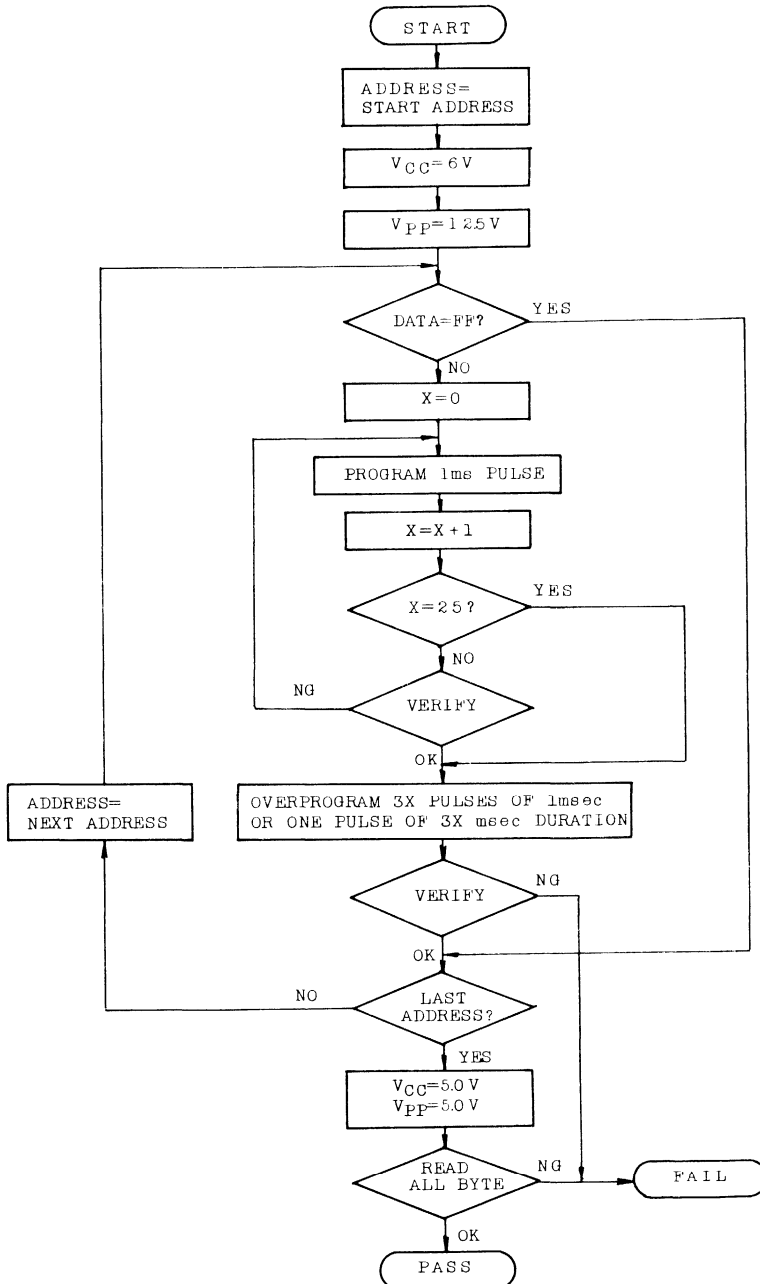
SIGNATURE	PINS	A <sub>0</sub>	O <sub>7</sub>	O <sub>6</sub>	O <sub>5</sub>	O <sub>4</sub>	O <sub>3</sub>	O <sub>2</sub>	O <sub>1</sub>	O <sub>0</sub>	HEX. DATA
		(10)	(19)	(18)	(17)	(16)	(15)	(13)	(12)	(11)	
Manufacture Code	$V_{IL}$	1	0	0	0	1	1	0	0	0	98
Device Code	$V_{IH}$	0	1	0	0	1	0	1	0	0	54

Notes: A9 = 12V ± 0.5V

A1 ~ A8, A10 ~ A14,  $\overline{CE}$ ,  $\overline{OE} = V_{IL}$

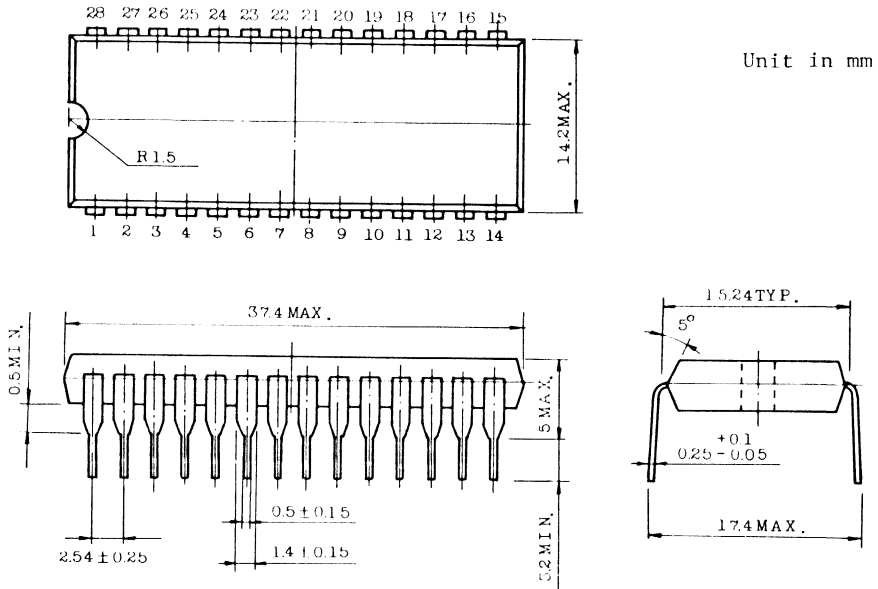
# TMM24256AP/AF

## HIGH SPEED PROGRAM MODE FLOW CHART



# TMM24256AP/AF

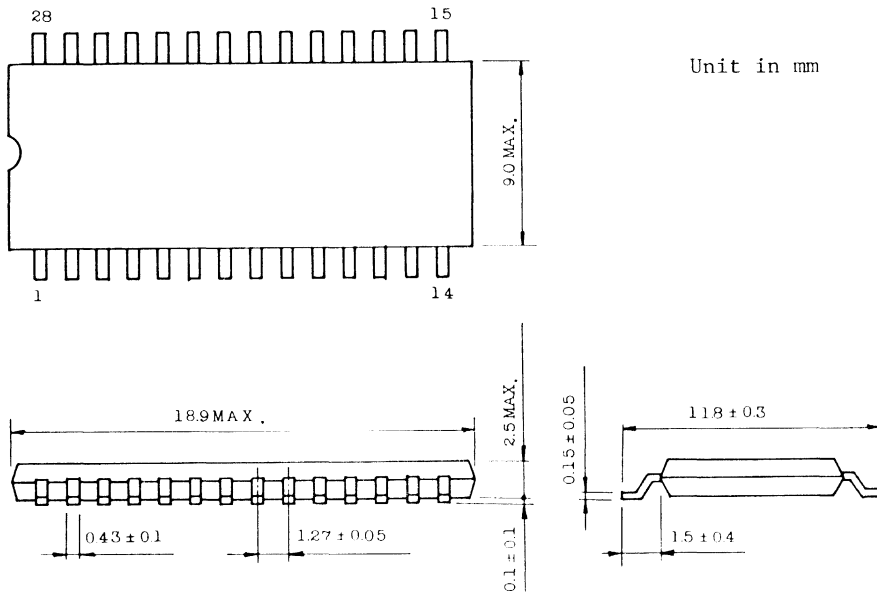
## OUTLINE DRAWINGS (TMM24256AP)



- Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

# TMM24256AP/AF

## OUTLINE DRAWINGS (TMM24256AF)



Note: Lead pitch is 1.27 and tolerance is  $\pm 0.12$  against theoretical center of each lead that is obtained on the basis of No. 1 and No. 28 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described: no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.  
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# TOSHIBA MOS MEMORY PRODUCT

## TC54256AP/AF

32,768 WORD x 8 BIT COMS ONE TIME PROGRAMMABLE READ ONLY MEMORY

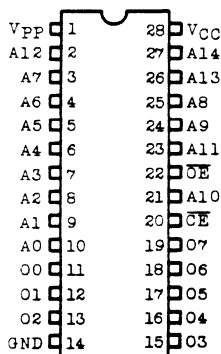
### DESCRIPTION

The TC54256AP/AF is a 32,768 word x 8 bit one time programmable read only memory, and molded in a 28 pin plastic package. The TC54256AP/AF's access time is 200ns and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as U.V. EPROM TC57256AD's. Once programed, the TC54256AP/AF can not be erased because of using plastic DIP without transparent window.

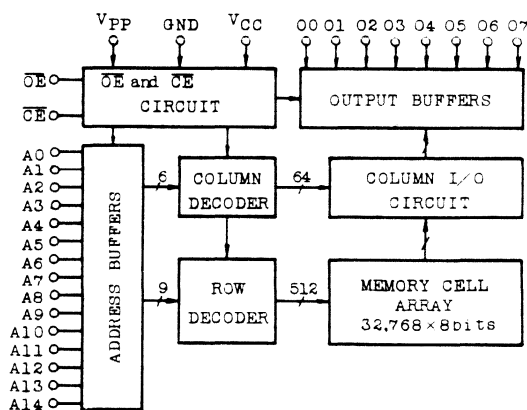
### FEATURES

- Peripheral circuit: CMOS
- Memory cell : N-MOS
- Low power dissipation
  - Active : 40mA/6.7mHz
  - Standby: 100µA
- Fast access time: 200ns
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, EPROM TMM27256D/AD, TC57256D/AD, One time PROM TMM24256P/AP and TC54256P
- Standard 28 pin DIP plastic package: TC54256AP
- Plastic Flat Package : TC54256AF

### PIN CONNECTION (TOP VIEW)



### BLOCK DIAGRAM



### PIN NAMES

A0 ~ A14	Address Inputs
00 ~ 07	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
VPP	Program Supply Voltage
VCC	VCC Supply Voltage (+5V)
GND	Ground

### MODE SELECTION

MODE	PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	VPP (1)	VCC (28)	00 ~ 07 (11 ~ 13, 15 ~ 19)	POWER
Read		L	L	5V	5V	Data Out	Active
Output Deselect	*	H	High Impedance				
Standby	H	*	High Impedance			Standby	
Program		L	H	12.5V	6V	Data In	Active
Program Inhibit	H	H	High Impedance				
Program Verify	*	L	Data Out				

\*: H or L

# TC54256AP/AF

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	-0.6 ~ 7.0	V
V <sub>PP</sub>	Program Supply Voltage	-0.6 ~ 14.0	V
V <sub>IN</sub>	Input Voltage	-0.6 ~ 7.0	V
V <sub>I/O</sub>	Input/Output Voltage	-0.6 ~ V <sub>CC</sub> +0.5	V
P <sub>D</sub>	Power Dissipation	1.5	W
T <sub>SOLDER</sub>	Soldering Temperature Time	260 · 10	°C · sec
T <sub>STRG</sub>	Storage Temperature	-65 ~ 125	°C
T <sub>OPR</sub>	Operating Temperature	-40 ~ 85	°C

## READ OPERATION

### D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	-	0.8	
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	4.75	5.00	5.25	
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	V <sub>CC</sub> -0.6	V <sub>CC</sub>	V <sub>CC</sub> +0.6	

### D.C. and OPERATING CHARACTERISTICS (T<sub>a</sub> = -40 ~ 85°C, V<sub>CC</sub> = 5V ± 5%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I <sub>LI</sub>	Input Current	V <sub>IN</sub> = 0V ~ V <sub>CC</sub>	-	-	±10	μA	
I <sub>CCO1</sub>	Operating Current	$\overline{CE}$ = 0V	f = 6.7MHz	-	-	40	mA
I <sub>CCO2</sub>			f = 1MHz	-	-	10	
I <sub>CCS1</sub>	Standby Current	$\overline{CE}$ = V <sub>IH</sub>	-	-	1	mA	
I <sub>CCS2</sub>		$\overline{CE}$ = V <sub>CC</sub> - 0.2V	-	-	100	μA	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400μA	2.4	-	-	V	
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA	-	-	0.4	V	
I <sub>PP1</sub>	V <sub>PP</sub> Current	V <sub>PP</sub> = V <sub>CC</sub> ± 0.6V	-	-	±10	μA	
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0.4V ~ V <sub>CC</sub>	-	-	±10	μA	



# TC54256AP/AF

A.C. CHARACTERISTICS (Ta=-40~85°C, V<sub>CC</sub>=5V±5%, V<sub>pp</sub>=V<sub>CC</sub>±0.6V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
t <sub>ACC</sub>	Address Access Time	$\overline{CE}=\overline{OE}=V_{IL}$	-	200	ns
t <sub>CE</sub>	$\overline{CE}$ to Output Valid	$\overline{OE}=V_{IL}$	-	200	
t <sub>OE</sub>	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IL}$	-	70	
t <sub>DF1</sub>	$\overline{CE}$ to Output in High-Z	$\overline{OE}=V_{IL}$	0	60	
t <sub>DF2</sub>	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	0	60	
t <sub>OH</sub>	Output Data in Hold Time	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	

## A.C. TEST CONDITIONS

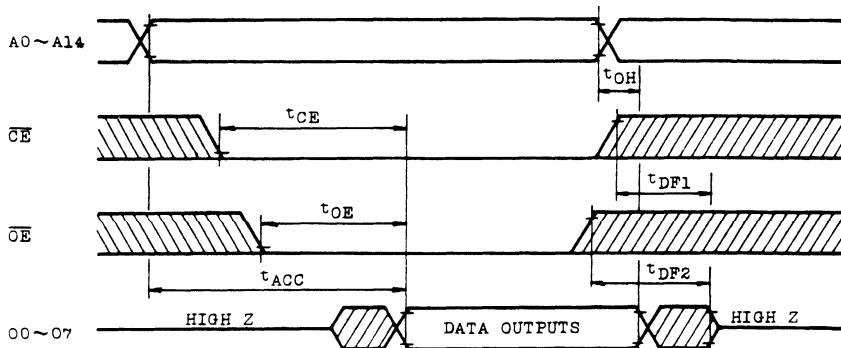
- Output Load : 1 TTL Gate and C<sub>L</sub>=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE \* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =0V	-	4	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> =0V	-	8	12	

\* This parameter is periodically sampled and is not 100% tested.

## TIMING WAVEFORMS (READ)



# TC54256AP/AF

## PROGRAM OPERATION

### D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input Low Voltage	-0.3	-	0.8	
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	5.75	6.0	6.25	
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	12.0	12.5	13.0	

### D.C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V<sub>CC</sub>=6V±0.25V, V<sub>PP</sub>=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>LI</sub>	Input Current	V <sub>IN</sub> =0 ~ V <sub>CC</sub>	-	-	±10	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> =-400μA	2.4	-	-	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> =2.1mA	-	-	0.4	V
I <sub>CC</sub>	V <sub>CC</sub> Supply Current	-	-	-	40	mA
I <sub>PP2</sub>	V <sub>PP</sub> Supply Current	V <sub>PP</sub> =13.0V	-	-	50	mA
V <sub>ID</sub>	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

### A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V<sub>CC</sub>=6V±0.25V, V<sub>PP</sub>=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t <sub>AS</sub>	Address Setup Time	-	2	-	-	μs
t <sub>AH</sub>	Address Hold Time	-	2	-	-	μs
t <sub>CES</sub>	$\overline{CE}$ Setup Time	-	0	-	-	ns
t <sub>CEH</sub>	$\overline{CE}$ Hold Time	-	0	-	-	ns
t <sub>OES</sub>	$\overline{OE}$ Setup Time	-	2	-	-	μs
t <sub>DS</sub>	Data Setup Time	-	2	-	-	μs
t <sub>DH</sub>	Data Hold Time	-	2	-	-	μs
t <sub>VPS</sub>	V <sub>PP</sub> Setup Time	-	2	-	-	μs
t <sub>VCS</sub>	V <sub>CC</sub> Setup Time	-	2	-	-	μs
t <sub>PW</sub>	Initial Program Pulse Width	$\overline{CE}=V_{IL}$ , $\overline{OE}=V_{IH}$	0.95	1	1.05	ms
t <sub>OPW</sub>	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t <sub>OE</sub>	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	-	-	150	ns
t <sub>DFP</sub>	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	-	-	130	ns

### A.C. TEST CONDITIONS

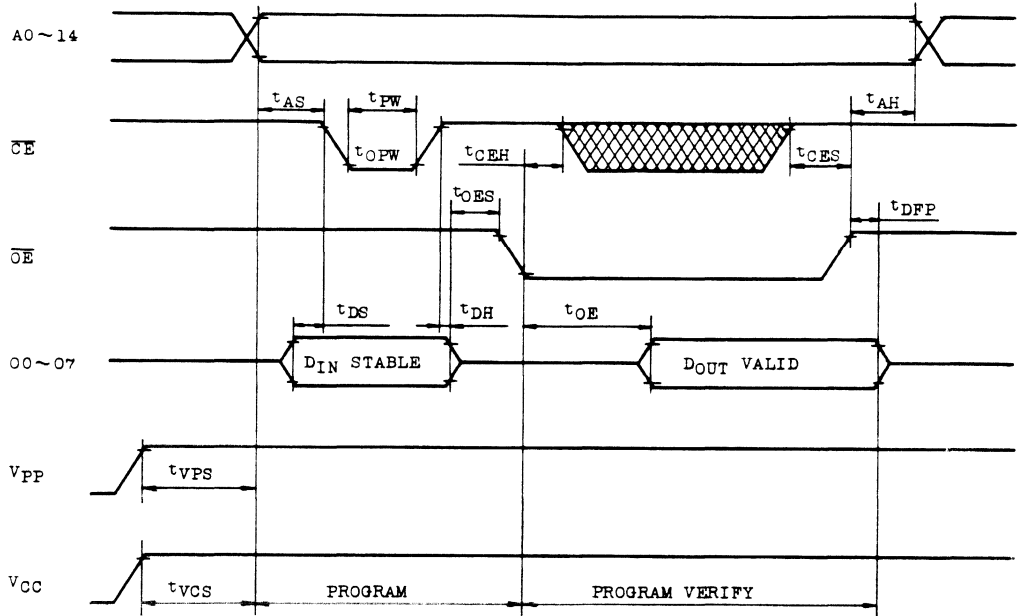
- Output Load : 1 TTL Gate and C<sub>L</sub> (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

# TC54256AP/AF

## TIMING WAVEFORMS (PROGRAM)

( $V_{CC}=6V\pm 0.25V$ ,  $V_{pp}=12.5V\pm 0.5V$ )



- Note 1.  $V_{CC}$  must be applied simultaneously or before  $V_{pp}$  and cut off simultaneously or after  $V_{pp}$ .
2. Removing the device from socket and setting the device in socket with  $V_{pp}=12.5V$  may cause permanent damage to the device.
  3. The  $V_{pp}$  supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the  $V_{pp}$  terminal. When the switching pulse voltage is applied to the  $V_{pp}$  terminal, the overshoot voltage of its pulse should not be exceeded 14V.

# TC54256AP/AF

## OPERATION INFORMATION

The TC54256AP/AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE		PIN NAMES (NUMBER)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$V_{PP}$ (1)	$V_{CC}$ (28)	00 ~ 07 (11 ~ 13, 15 ~ 19)	POWER
Read Operation ( $T_a = -40 \sim 85^\circ\text{C}$ )	Read		L	L	5V	5V	Data Out	Active
	Output Deselect	*	H	High Impedance				
	Standby	H	*	High Impedance			Standby	
Program Operation ( $T_a = 25 \pm 5^\circ\text{C}$ )	Program		L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	H	High Impedance				
	Program Verify	*	L	Data Out				

Note: H;  $V_{IH}$ , L;  $V_{IL}$ , \*;  $V_{IH}$  or  $V_{IL}$

## READ MODE

The TC54256AP/AF has two control functions. The chip enable ( $\overline{CE}$ ) controls the operation power and should be used for device selection. The output enable ( $\overline{OE}$ ) controls the output buffers, independent of device selection. Assuming that  $\overline{CE} = \overline{OE} = V_{IL}$ , the output data is valid at the outputs after address access time from stabilizing of all addresses. The  $\overline{CE}$  to output valid ( $t_{CE}$ ) is equal to the address access time ( $t_{ACC}$ ). Assuming that  $\overline{CE} = V_{IL}$  and all addresses are valid, the output data is valid at the outputs after  $t_{OE}$  from the falling edge of  $\overline{OE}$ .

## OUTPUT DESELECT MODE

Assuming that  $\overline{CE} = V_{IH}$  or  $\overline{OE} = V_{IH}$ , the outputs will be in a high impedance state. So two or more TC54256AP/AF's can be connected together on a common bus line. When  $\overline{CE}$  is decoded for device selection, all deselected devices are in low power standby mode.

## STANDBY MODE

The TC54256AP/AF has a low power standby mode controlled by the  $\overline{CE}$  signal. By applying a high level to the  $\overline{CE}$  input, the TC54256AP/AF is placed in the standby mode which reduce the operating current to 100 $\mu\text{A}$  by applying MOS-high level ( $V_{CC}$ ) and then the outputs are in a high impedance state, independent of the  $\overline{OE}$  inputs.

# TC54256AP/AF

## PROGRAM MODE

Initially, when received by customers, all bits of the TC54256AP/AF are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming. The TC54256AP/AF is in the programming mode when the  $V_{pp}$  input is at 12.5V and  $\overline{CE}$  is at TTL-Low level under  $\overline{OE}=V_{IH}$ . The TC54256AP/AF can be programmed any location at anytime either individually, sequentially, or at random.

## PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with  $\overline{OE}$  at  $V_{IL}$  and  $\overline{CE}$  at  $V_{IH}$  or  $V_{IL}$ .

## PROGRAM INHIBIT MODE

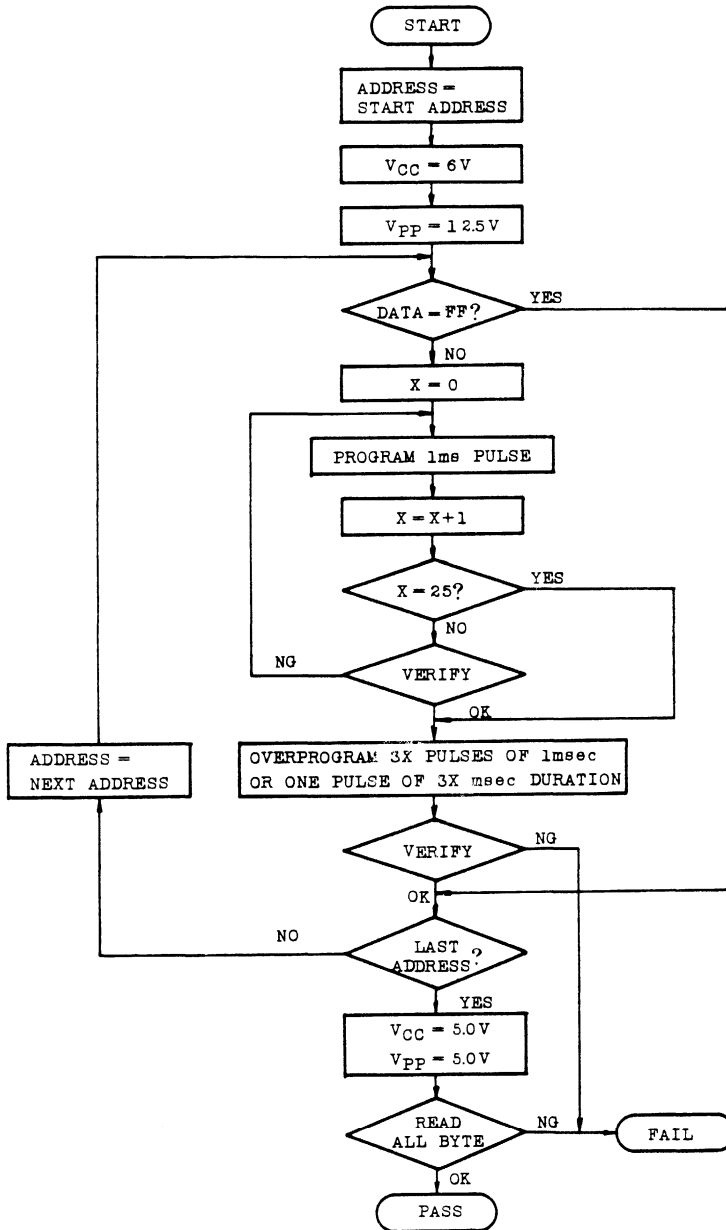
Under the condition that the program voltage (+12.5V) is applied to  $V_{pp}$  terminal, a TTL high level  $\overline{CE}$  input inhibits the TC54256AP/AF from being programmed. Programming of two or more TC54256AP/AF's in parallel with different data is easily accomplished. That is, all inputs except for  $\overline{CE}$  and  $\overline{OE}$  may be commonly connected, and a TTL Low level program pulse is applied to the  $\overline{CE}$  of the desired device only and TTL high level signal is applied to the other devices.

## HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the  $V_{pp}$  terminal with  $V_{CC}=6V$ . The programming is achieved by applying a single TTL low level lms pulse to the  $\overline{CE}$  input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of lms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times). After correctly programming the selected address, the additional program pulse with width of 3 times more than that needed for initial programming is applied. When programming has been completed, the data in all addresses should be verified with  $V_{CC}=V_{pp}=5V$ .

# TC54256AP/AF

## HIGH SPEED PROGRAM MODE FLOW CHART



# TC54256AP/AF

## ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC54256AP/AF which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC54256AP/AF by using this mode before program operation and automatically set program voltage ( $V_{pp}$ ) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to  $V_{IL}$  in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to  $V_{IH}$ . These two codes possess an odd parity with the parity bit of MSB (07). The following table shows electric signature of TC54256AP/AF.

SIGNATURE \ PINS	A0 (10)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	HEX. DATA
Manufacture Code	$V_{IL}$	1	0	0	1	1	0	0	0	98
Device Code	$V_{IH}$	1	1	0	0	0	1	0	0	C4

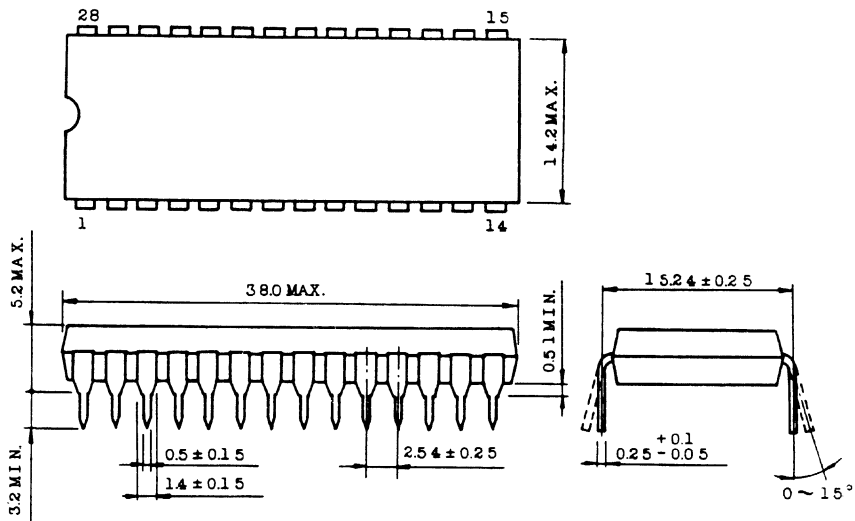
Notes: A9=12V±0.5V

A1 ~ A8, A10 ~ A14,  $\overline{CE}$ ,  $\overline{OE}$ = $V_{IL}$

# TC54256AP/AF

## OUTLINE DRAWINGS (TC54256AP)

Unit in mm



Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.

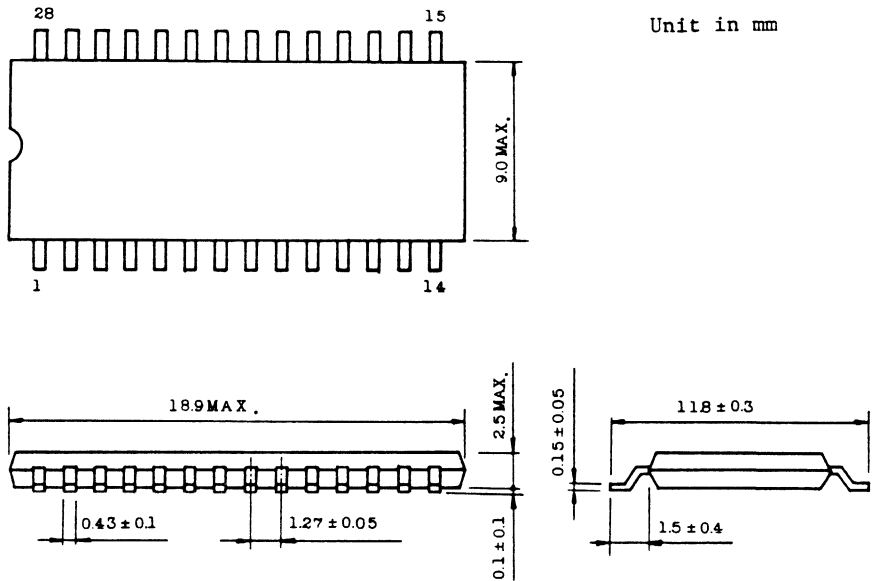
2. This value is measured at the end of leads.

3. All dimensions are in millimeters.



# TC54256AP/AF

## OUTLINE DRAWINGS (TC54256AF)



Note: Lead pitch is 1.27 and tolerance is  $\pm 0.12$  against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.



# TOSHIBA MOS MEMORY PRODUCT

## TMM24512P/F

TMM24512P/F 65,536 WORD x 8 BIT ONE TIME PROGRAMMABLE READ ONLY MEMORY

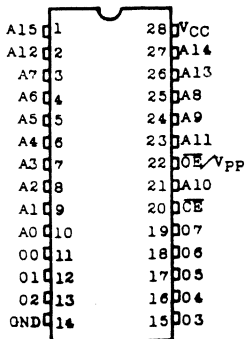
### DESCRIPTION

The TMM24512P/F is a 65,536 word x 8 bit one time programmable read only memory, and molded in a 28 pin plastic package. The TMM24512P/F's access time is 250ns, and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as U.V. EPROM TMM27512D's. Once programed, the TMM24512P/F can not be erased because of using plastic DIP without transparent window.

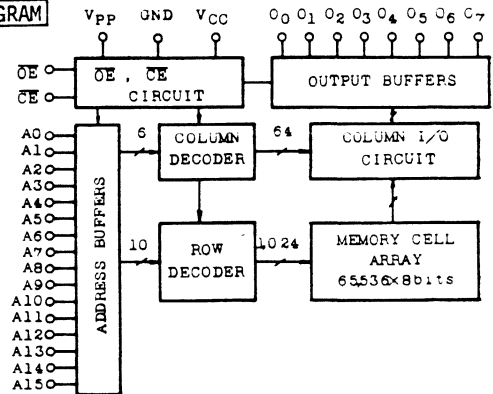
### FEATURES

- Fast access time: 250ns
- Low power dissipation
  - Active : 120mA
  - Standby: 35mA
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with TMM27512D
- Standard 28 pin DIP plastic package: TMM24512P
- Plastic Flat Package : TMM24512F

### PIN CONNECTION (TOP VIEW)



### BLOCK DIAGRAM



### PIN NAMES

A0 ~ A15	Address Inputs
00 ~ 07	Outputs (Inputs)
CE	Chip Enable Input
OE/Vpp	Output Enable / Program Supply Voltage
VCC	Power Supply Voltage (+5V)
GND	Ground

### MODE SELECTION

MODE	PIN CE (20)	OE/Vpp (22)	VCC (28)	00 ~ 07 (11 ~ 13, 15 ~ 19)	POWER
Read	L	L	5V	Data Out	Active
Output Deselect	*	H		High Impedance	
Standby	H	*	6V	High Impedance	Standby
Program	L	Vpp		Data In	Active
Program Inhibit	H	Vpp		High Impedance	
Program Verify	L	L		Data Out	

\* H or L

# TMM24512P/F

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	-0.6 ~ 7.0	V
V <sub>PP</sub>	Program Supply Voltage	-0.6 ~ 14.0	V
V <sub>IN</sub>	Input Voltage	-0.6 ~ 7.0	V
V <sub>I/O</sub>	Input/Output Voltage	-0.6 ~ 7.0	V
P <sub>D</sub>	Power Dissipation	1.5	W
T <sub>SOLDER</sub>	Soldering Temperature	260 · 10	°C·sec
T <sub>STG</sub>	Storage Temperature	-55 ~ 150	°C
T <sub>OPR</sub>	Operating Temperature	0 ~ 70	°C

## READ OPERATION

### D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.0	-	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input low Voltage	-0.3	-	0.8	
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	4.75	5.00	5.25	

### D.C. and OPERATING CHARACTERISTICS (T<sub>a</sub>=0 ~ 70°C, V<sub>CC</sub>=5V±5%)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>LI</sub>	Input Current	V <sub>IN</sub> =0 ~ V <sub>CC</sub>	-	-	±10	μA
I <sub>CC1</sub>	Supply Current (Standby)	$\bar{CE}=V_{IH}$	-	-	35	mA
I <sub>CC2</sub>	Supply Current (Active)	$\bar{CE}=V_{IL}$	-	-	120	mA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> =-400μA	2.4	-	-	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> =2.1mA	-	-	0.4	V
I <sub>PP1</sub>	V <sub>pp</sub> Current	V <sub>PP</sub> =0 ~ V <sub>CC</sub> +0.6V	-	-	±10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> =0.4V ~ V <sub>CC</sub>	-	-	±10	μA

# TMM24512P/F

A.C. CHARACTERISTICS ( $T_a=0 \sim 70^\circ\text{C}$ ,  $V_{CC}=5V \pm 5\%$ ,  $V_{PP}=2.0V \sim V_{CC}+0.6V$ )

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	UNIT
$t_{ACC}$	Address Access Time	$\overline{CE}=\overline{OE}=V_{IL}$	-	250	ns
$t_{CE}$	$\overline{CE}$ to Output Valid	$\overline{OE}=V_{IL}$	-	250	
$t_{OE}$	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IL}$	-	100	
$t_{DF1}$	$\overline{CE}$ to Output in High-Z	$\overline{OE}=V_{IL}$	0	90	
$t_{DF2}$	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	0	90	
$t_{OH}$	Output Data in Hold Time	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	

## A.C. TEST CONDITIONS

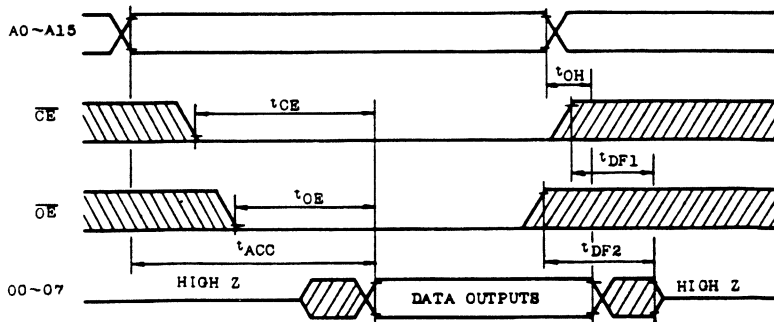
- Output Load : 1 TTL Gate and  $C_L=100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V  $\sim$  2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE \* ( $T_a=25^\circ\text{C}$ ,  $f=1\text{MHz}$ )

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$C_{IN1}$	Input Capacitance	$V_{IN}=0V$	-	4	6	pF
$C_{IN2}$	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN}=0V$	-	50	60	
$C_{OUT}$	Output Capacitance	$V_{OUT}=0V$	-	8	12	

\* This parameter is periodically sampled and is not 100% tested.

## TIMING WAVEFORMS (READ)



# TMM24512P/F

## PROGRAM OPERATION

### D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	2.0	-	V <sub>CC</sub> +1.0	V
V <sub>IL</sub>	Input Low Voltage	-0.3	-	0.8	
V <sub>CC</sub>	V <sub>CC</sub> Power Supply Voltage	5.75	6.0	6.25	
V <sub>PP</sub>	V <sub>PP</sub> Power Supply Voltage	12.0	12.5	13.0	

### D.C. and OPERATING CHARACTERISTICS (T<sub>a</sub>=25±5°C, V<sub>CC</sub>=6V±0.25V, V<sub>PP</sub>=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>LI</sub>	Input Current	V <sub>IN</sub> =0 ~ V <sub>CC</sub>	-	-	±10	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> =-400μA	2.4	-	-	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> =2.1mA	-	-	0.4	V
I <sub>CC</sub>	V <sub>CC</sub> Supply Current	-	-	-	130	mA
I <sub>PP2</sub>	V <sub>PP</sub> Supply Current	V <sub>PP</sub> =13.0V	-	-	50	mA
V <sub>ID</sub>	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

### A.C. PROGRAMMING CHARACTERISTICS (T<sub>a</sub>=25±5°C, V<sub>CC</sub>=6V±0.25V, V<sub>PP</sub>=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t <sub>AS</sub>	Address Setup Time	-	2	-	-	μs
t <sub>AH</sub>	Address Hold Time	-	2	-	-	μs
t <sub>OES</sub>	$\overline{OE}/V_{PP}$ Setup Time	-	2	-	-	μs
t <sub>OEH</sub>	$\overline{OE}/V_{PP}$ Hold Time	-	2	-	-	μs
t <sub>PRT</sub>	$\overline{OE}/V_{PP}$ Pulse Rise Time	-	50	-	-	μs
t <sub>DS</sub>	Data Setup Time	-	2	-	-	μs
t <sub>DH</sub>	Data Hold Time	-	2	-	-	μs
t <sub>VR</sub>	$\overline{OE}/V_{PP}$ Recovery Time	-	2	-	-	μs
t <sub>VCS</sub>	V <sub>CC</sub> Setup Time	-	2	-	-	μs
t <sub>PW</sub>	Initial Program Pulse Width	$\overline{CE}=V_{IL}$ , $\overline{OE}/V_{PP}=V_{PP}$	0.95	1	1.05	ms
t <sub>OPW</sub>	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t <sub>DV</sub>	Data Valid from $\overline{CE}$	$\overline{OE}/V_{PP}=V_{IL}$	-	-	1	μs
t <sub>DF</sub>	$\overline{CE}$ to Output in High-Z	$\overline{OE}/V_{PP}=V_{IL}$	-	-	130	ns

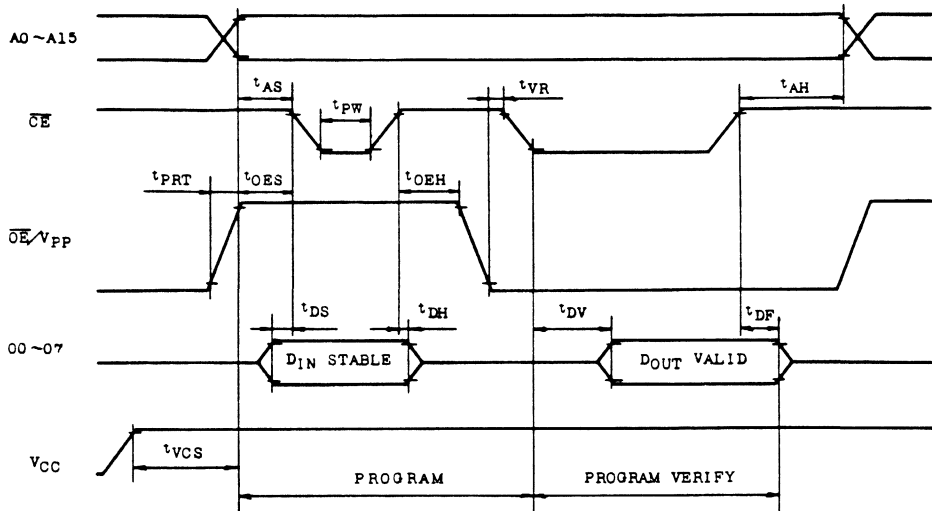
### A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C<sub>L</sub> (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

## TIMING WAVEFORMS (PROGRAM)

( $V_{CC}=6V\pm 0.25V$ ,  $V_{PP}=12.5V\pm 0.5V$ )



- Note 1.  $V_{CC}$  must be applied simultaneously or before  $V_{pp}$  and cut off simultaneously or after  $V_{pp}$ .
2. Removing the device from socket and setting the device in socket with  $V_{pp}=12.5V$  may cause permanent damage to the device.
  3. The  $V_{pp}$  supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the  $V_{pp}$  terminal. When the switching pulse voltage is applied to the  $V_{pp}$  terminal, the overshoot voltage of its pulse should not be exceeded 14V.

# TMM24512P/F

## OPERATION INFORMATION

The TMM24512P/F's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE		PIN NAMES (NUMBER)	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	$V_{CC}$ (28)	00 ~ 07 (11 ~ 13, 15 ~ 19)	POWER
Read Operation ( $T_a=0 \sim 70^\circ\text{C}$ )	Read		L	L	5V	Data Out	Active
	Output Deselect		*	H		High Impedance	
	Standby		H	*		High Impedance	Standby
Program Operation ( $T_a=25 \pm 5^\circ\text{C}$ )	Program		L	$V_{PP}$	6V	Data In	Active
	Program Inhibit		H	$V_{PP}$		High Impedance	
	Program Verify		L	L		Data Out	

Note: H;  $V_{IH}$ , L;  $V_{IL}$ , \*;  $V_{IH}$  or  $V_{IL}$

### READ MODE

The TMM24512P/F has two control functions. The chip enable ( $\overline{CE}$ ) controls the operation power and should be used for device selection. The output enable ( $\overline{OE}$ ) control the output buffers, independent of device selection. Assuming the  $\overline{CE}=\overline{OE}=V_{IL}$ , the output data is valid at the outputs after address access time from stabilizing of all addresses. The  $\overline{CE}$  to output valid ( $t_{CE}$ ) is equal to the address access time ( $t_{ACC}$ ). Assuming that  $\overline{CE}=V_{IL}$  and all addresses are valid, the output data is valid at the outputs after  $t_{OE}$  from the falling edge of  $\overline{OE}$ .

### OUTPUT DESELECT MODE

Assuming that  $\overline{CE}=V_{IH}$  or  $\overline{OE}=V_{IH}$ , the outputs will be in a high impedance state. So two or more TMM24512P/F's can be connected together on a common bus line. When  $\overline{CE}$  is decoded for device selection, all deselected devices are in low power standby mode.

### STANDBY MODE

The TMM24512P/F has a low power standby mode controlled by the  $\overline{CE}$  signal. By applying a high level to the  $\overline{CE}$  input, the TMM24512P/F is placed in the standby mode which reduce the operating current to 35mA from 120mA (about 70% reduction) by applying MOS-high level ( $V_{CC}$ ) and then the outputs are in a high impedance state, independent of the  $\overline{OE}$  inputs.



# TMM24512P/F

## PROGRAM MODE

Initially, when received by customers, all bits of the TMM24512P/F are in the "1" state which is erased state. Therefore the program operation is to introduce "0" data into the desired bit locations by electrically programming. The TMM24512P/F is in the programming mode when the  $\overline{OE}/V_{pp}$  input is at 12.5V and  $\overline{CE}$  is at TTL-Low level. The TMM24512P/F can be programmed any location at anytime either individually, sequentially, or at random.

## PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with  $\overline{CE}$  at  $V_{IL}$  and  $\overline{OE}/V_{pp}$  at  $V_{IL}$ .

## PROGRAM INHIBIT MODE

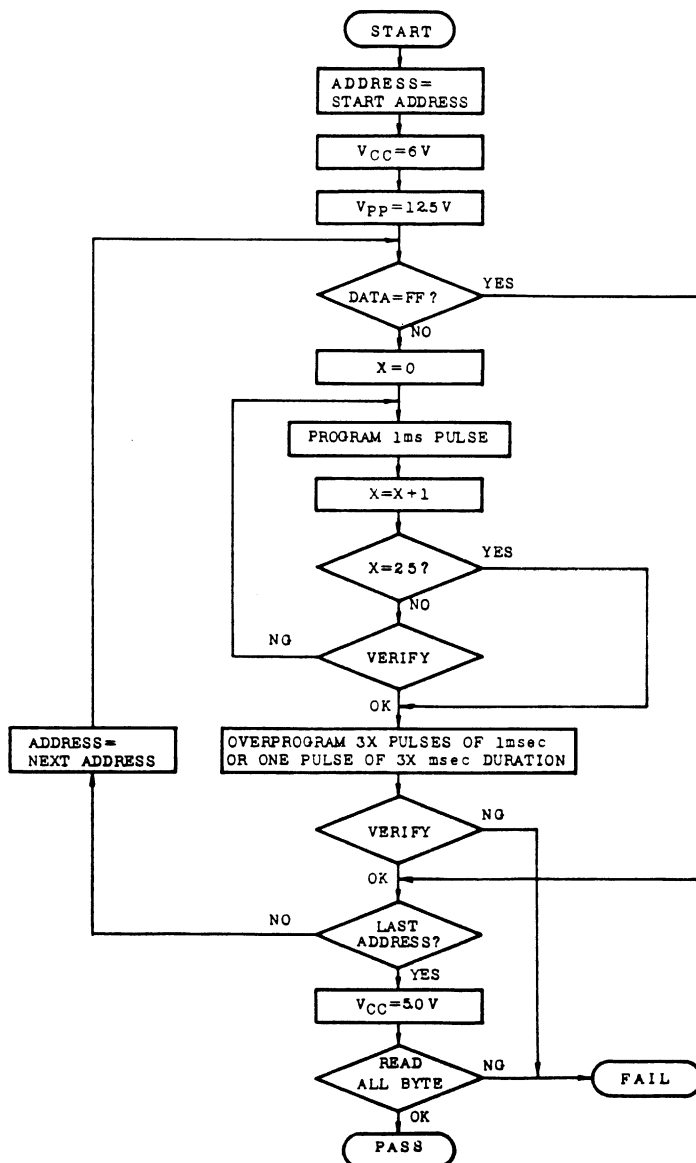
Under the condition that the program voltage (+12.5V) is applied to  $V_{pp}$  terminal, a TTL high level  $\overline{CE}$  input inhibits the TMM24512P/F from being programmed. Programming of two or more TMM24512P/F's in parallel with different data is easily accomplished. That is, all inputs except for  $\overline{CE}$  and  $\overline{OE}$  may be commonly connected, and a TTL Low level program pulse is applied to the  $\overline{CE}$  of the desired device only and TTL high level signal is applied to the other devices.

## HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the  $V_{pp}$  terminal with  $V_{CC}=6V$ . The programming is achieved by applying a single TTL low level 1ms pulse to the  $\overline{CE}$  input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times). After correctly programming the selected address, the additional program pulse with width equal to that needed for initial programming is applied. When programming has been completed, the data in all addresses should be verified with  $V_{CC}=5V$ .

# TMM24512P/F

## HIGH SPEED PROGRAM MODE FLOW CHART



# TMM24512P/F

## ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM24512P/F which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM24512P/F by using this mode before program operation and automatically set program voltage ( $V_{pp}$ ) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to  $V_{IL}$  in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to  $V_{IH}$ . These two codes possess an odd parity with the parity bit of MSB (07).

The following table shows electric signature of TMM24512P/F.

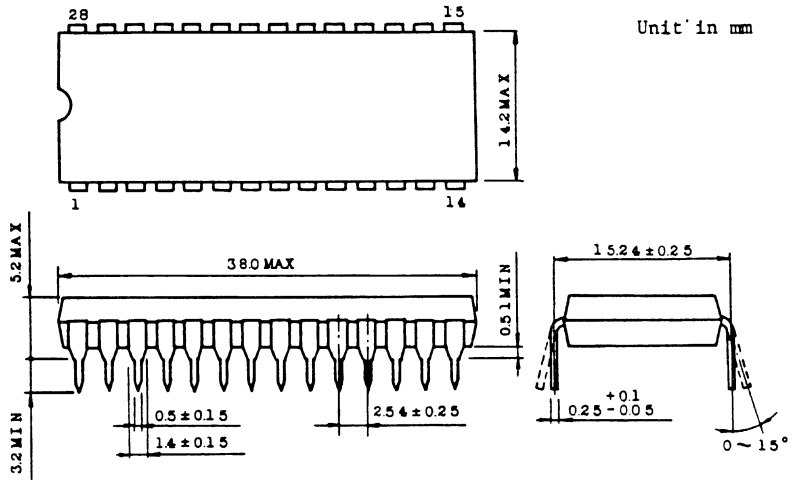
SIGNATURE	PINS	A0	07	06	05	04	03	02	01	00	HEX.
		(10)	(19)	(18)	(17)	(16)	(15)	(13)	(12)	(11)	DATA
Manufacture Code	$V_{IL}$	1	0	0	1	1	0	0	0	0	98
Device Code	$V_{IH}$	0	0	0	1	0	1	0	1	1	15

Notes: A9=12V±0.5V

A1 ~ A8, A10 ~ A15,  $\overline{CE}$ ,  $\overline{OE}$ = $V_{IL}$

# TMM24512P/F

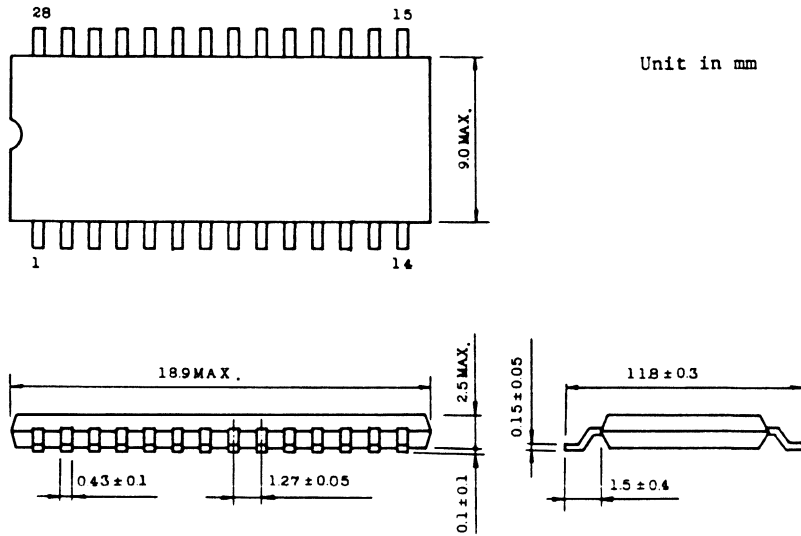
## OUTLINE DRAWINGS (TMM24512P)



- Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

# TMM24512P/F

## OUTLINE DRAWINGS (TMM24512F)



Note: Lead pitch is 1.27 and tolerance is  $\pm 0.12$  against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.



**Read Only Memories**





# TOSHIBA MOS MEMORY PRODUCT

256K BIT (32K WORD × 8 BIT) CMOS MASK ROM  
SILICON GATE MOS

TC53257P  
TC53257F

## DESCRIPTION

The TC53257P/F is a 262,144 bit read only memory organized as 32,768 words by 8 bits with a low bit cost, this being suitable for use in program memory of microprocessor, and in character generator. The TC53257P/F using CMOS technology is most suitable for low power applications where bat-

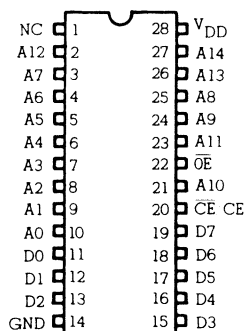
tery operation is required.

The TC53257P/F has one programmable chip enable input  $\overline{CE}/CE$ , for device selection and one output enable input ( $\overline{OE}$ ) for fast memory access and output control.

## FEATURES

- Single 5V Power Supply
- Access Time : 200ns(Max.)
- Power Dissipation  
Operating Current : 25mA(Max.)  
Standby Current : 20 $\mu$ A(Max.)
- Pin Compatible with 256K EPROM TC57256D
- Full Static Operation
- Programmable Chip Enable
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- Package  
Plastic DIP : TC53257P  
Plastic FP : TC53257F

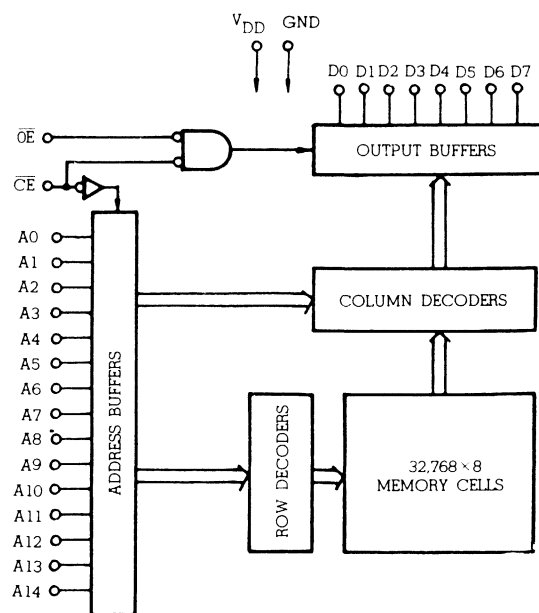
## PIN CONNECTION (TOP VIEW)



## PIN NAMES

A <sub>0</sub> ~A <sub>14</sub>	Address Inputs
D <sub>0</sub> ~D <sub>7</sub>	Data Outputs
NC	No connection
$\overline{CE}/CE$	Chip enable input
$\overline{OE}$	Output enable input
V <sub>DD</sub>	Power supply
GND	Ground

## BLOCK DIAGRAM



# TC53257P

# TC53257F

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V <sub>DD</sub>	Power Supply Voltage	-0.5~7.0	V
V <sub>IN</sub>	Input Voltage	-0.5~7.0	V
V <sub>OUT</sub>	Output Voltage	0~V <sub>DD</sub>	V
P <sub>D</sub>	Power Dissipation	1.0 0.6*	W
T <sub>STG</sub>	Storage Temperature	-55~150	°C
T <sub>OPR</sub>	Operating Temperature	-40~85	°C
T <sub>SOLDER</sub>	Soldering Temperature·Time	260·10	°C·sec

Note : \*Plastic FP

## D. C. OPERATING CONDITINS (Ta = -40~85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	—	0.8	V

## D. C. and OPERATING CHARACTERISTICS (Ta = -40~85°C, V<sub>DD</sub> = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0V ~ V <sub>DD</sub>	—	±1.0	μA
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ V <sub>OUT</sub> = 0V ~ V <sub>DD</sub>	—	±5.0	μA
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4V	-1.0	—	mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4V	3.2	—	mA
I <sub>DD</sub> S1	Standby Current	$\overline{CE} = V_{IH}$ CE = V <sub>IL</sub>	—	2	mA
I <sub>DD</sub> S2	Standby Current	$\overline{CE} = V_{DD} - 0.2V$ , CE = 0.2V	—	20	μA
I <sub>DD</sub> O1	Operating Current	V <sub>IH</sub> = V <sub>IH VIL</sub> , t <sub>CYCLE</sub> = 200ns	—	40	mA
I <sub>DD</sub> O2		V <sub>IN</sub> = V <sub>DD</sub> - 0.2V ~ 0.2V, t <sub>CYCLE</sub> = 200ns	—	25	mA

## CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	f = 1MHz, Ta = 25 C	—	8	pF
C <sub>OUT</sub>	Output Capacitance	f = 1MHz, Ta = 25 C	—	10	pF

Note : This parameter is periodically sampled and is not 100% tested.

# TC53257P TC53257F

## A. C. CHARACTERISTICS (Ta = -40~85°C, V<sub>DD</sub> = 5V ± 10%)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t <sub>CYC</sub>	Cycle Time	200	—	ns
t <sub>ACC</sub>	Access Time	—	200	ns
t <sub>CE</sub>	Chip Enable Access Time from CE/ $\overline{\text{CE}}$	—	200	ns
t <sub>OE</sub>	Output Enable Access Time from $\overline{\text{OE}}$	—	70	ns
t <sub>CED</sub> , t <sub>OED</sub>	Output Disable Time from CE/ $\overline{\text{CE}}$ , $\overline{\text{OE}}$	0	60	ns
t <sub>OH</sub>	Output Hold Time	0	—	ns

### A. C. TEST CONDITIONS

Output Load : 100pF + 1TTL

Input Levels : 0.6V, 2.4V

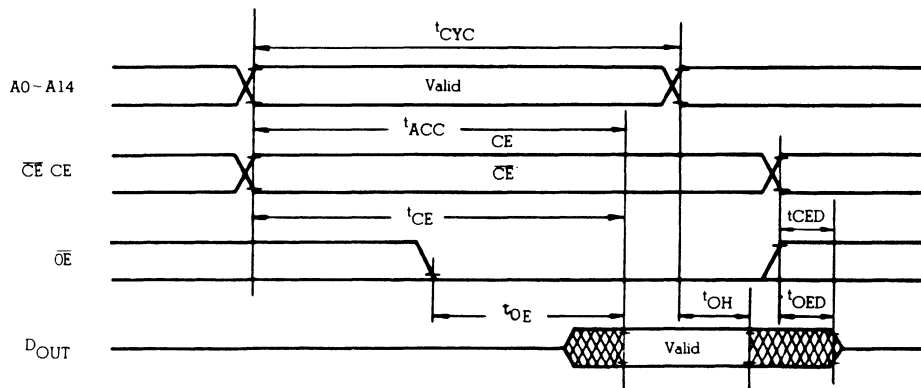
Timing Measurement Reference Levels

Input : 0.8V, 2.2V

Output : 0.8V, 2.2V

Input Rise and Fall Time : 5ns

### TIMING WAVEFORMS



### OPERATION MODE H : V<sub>IH</sub>, L : V<sub>IL</sub>, \* : V<sub>IH</sub> or V<sub>IL</sub>

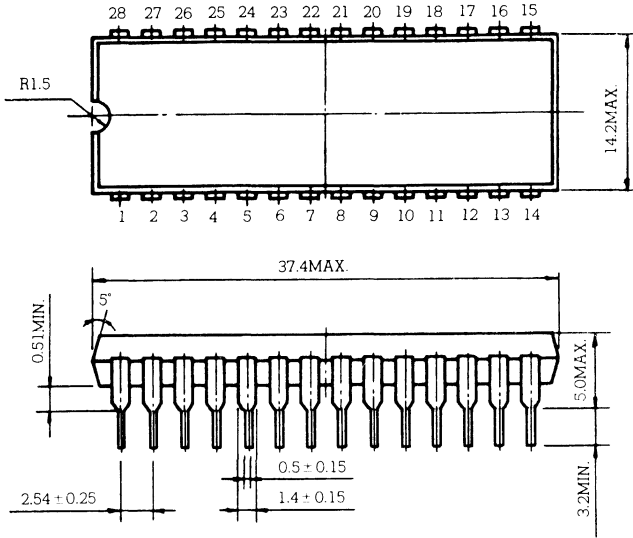
MODE	$\overline{\text{CE}}$ (CE)	$\overline{\text{OE}}$	A <sub>0</sub> ~14	Outputs	Power
Read	L(H)	L	Valid	Data out	Operating
Output Deselect	L(H)	H	*	High-Z	Operating
	H(L)	*	*		Standby

# TC53257P

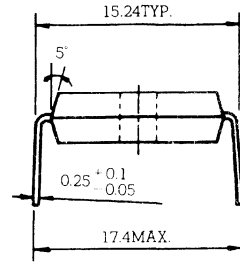
# TC53257F

## OUTLINE DRAWINGS

- Plastic DIP



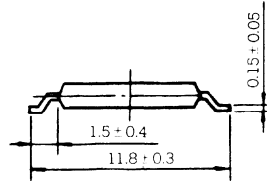
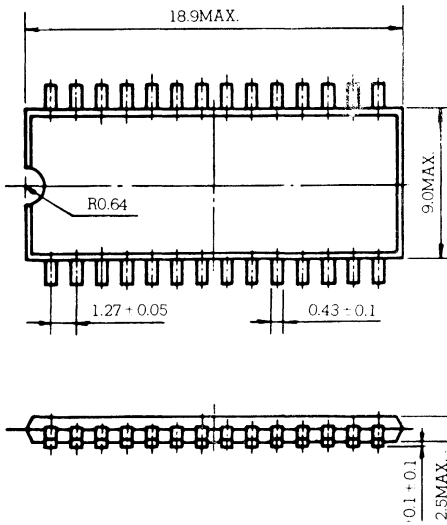
Unit: mm



NOTE : Each lead pitch is 2.54mm.

All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.

- Plastic FP



NOTE : Each lead pitch is 1.27mm.

All leads are located within 0.12mm of their true longitudinal position with respect to No. 1 and No. 28 leads.

# TOSHIBA MOS MEMORY PRODUCT

1M BIT (128K WORD × 8 BIT)  
CMOS MASK ROM  
SILICON GATE CMOS

TC531000AP  
TC531000AF

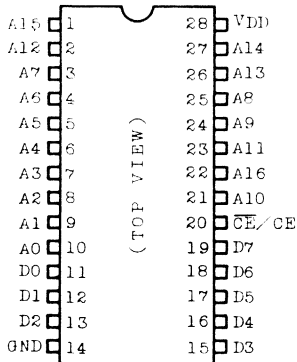
## DESCRIPTION

The TC531000AP/AF is a 1,048,576 bits read only memory organized as 131,072 words by 8 bits with a low bit cost, thus being suitable for use in program memory of microprocessor, especially character generator. The TC531000AP/AF using CMOS technology is most suitable for low power applications where battery operation are required. The TC531000AP/AF has one chip enable input  $\overline{CE}/CE$ , programmable for device selection.

## FEATURES

- Single 5V Power Supply
- Access Time: 150ns (Max.)
- Power Dissipation
  - Operating Current: 40mA (Max.)
  - Standby Current : 20 $\mu$ A (Max.)
- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- Fully Static Operation
- Programmable Chip Enable
- Package     Plastic DIP: TC531000AP  
              Plastic FP : TC531000AF

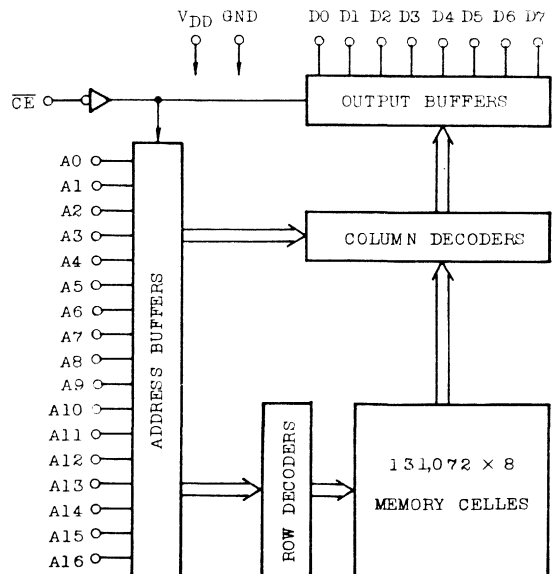
## PIN CONNECTION



## PIN NAMES

A0 ~ A16	Address Inputs
D0 ~ D7	Data Outputs
$\overline{CE}/CE$	Chip Enable Input
VDD	Power Supply
GND	Ground

## BLOCK DIAGRAM



# TC531000AP

# TC531000AF

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.5 ~ 7.0	V
V <sub>IN</sub>	Input Voltage	-0.5 ~ V <sub>DD</sub>	V
V <sub>OUT</sub>	Output Voltage	0 ~ V <sub>DD</sub>	V
P <sub>D</sub>	Power Dissipation	1.0/0.6*	W
T <sub>STG</sub>	Storage Temperature	-55 ~ 150	°C
T <sub>OPR</sub>	Operating Temperature	-40 ~ 70	°C
T <sub>SOLDER</sub>	Soldering Temperature • Time	260 • 10	°C • sec

Note: \* Plastic FP

## D.C. OPERATING CONDITIONS (Ta=-40 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	-	0.8	V

## D.C. and OPERATING CHARACTERISTICS (Ta=-40 ~ 70°C, V<sub>DD</sub>=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> =0 ~ V <sub>DD</sub>	-	±1.0	μA
I <sub>LO</sub>	Output Leakage Current	$\overline{C}E=V_{IH}$ , V <sub>OUT</sub> =0 ~ V <sub>DD</sub>	-	±5.0	μA
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> =2.4V	-1.0	-	mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> =0.4V	2.0	-	mA
I <sub>DDS1</sub>	Standby Current	$\overline{C}E=V_{IH}$	-	2	mA
I <sub>DDS2</sub>	Standby Current	$\overline{C}E=V_{DD}$ and V <sub>IN</sub> =0V (V <sub>DD</sub> )	-	20	μA
I <sub>DDO1</sub>	Operating Current	V <sub>IN</sub> =V <sub>IH</sub> /V <sub>IL</sub> , t <sub>cycle</sub> =150ns	-	50	mA
I <sub>DDO2</sub>		V <sub>IN</sub> =V <sub>DD</sub> /0V, t <sub>cycle</sub> =150ns	-	40	

## CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	f=1MHz, Ta=25°C	-	10	pF
C <sub>OUT</sub>	Output Capacitance	f=1MHz, Ta=25°C	-	10	

Note: This parameter is periodically sampled and is not 100% tested.

# TC531000AP TC531000AF

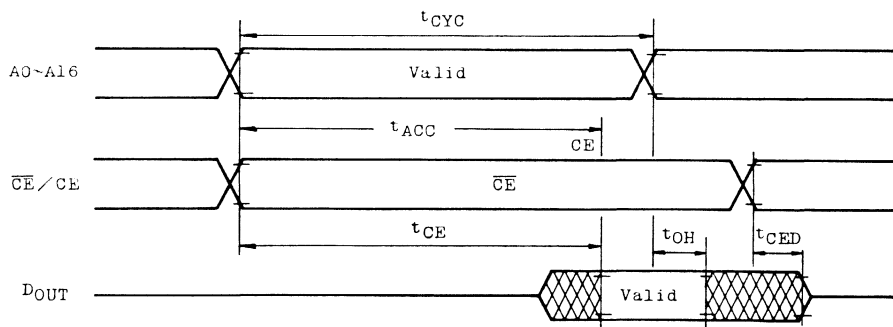
## A.C. CHARACTERISTICS ( $V_{DD}=5V\pm 10\%$ , $T_a=-40\sim 70^\circ\text{C}$ )

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$t_{CYC}$	Cycle Time	150	-	ns
$t_{ACC}$	Access Time	-	150	ns
$t_{CE}$	Chip Enable Access Time	-	150	ns
$t_{CED}$	Output Disable Time	-	50	ns
$t_{OH}$	Output Hold Time	0	-	ns

## AC TEST CONDITIONS

- Output Load : 100pF + 1TTL
- Input Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels  
Input : 0.8V, 2.2V  
Output: 0.8V, 2.0V
- Input Rise and Fall Time : 5ns

## TIMING WAVEFORMS



## OPERATION MODE

MODE	$\overline{CE}$ (CE)	A0 ~ 16	Outputs	Power
Read	L(H)	Valid	Data Out	Operating
Output Deselect	H(L)	*	High-Z	Standby

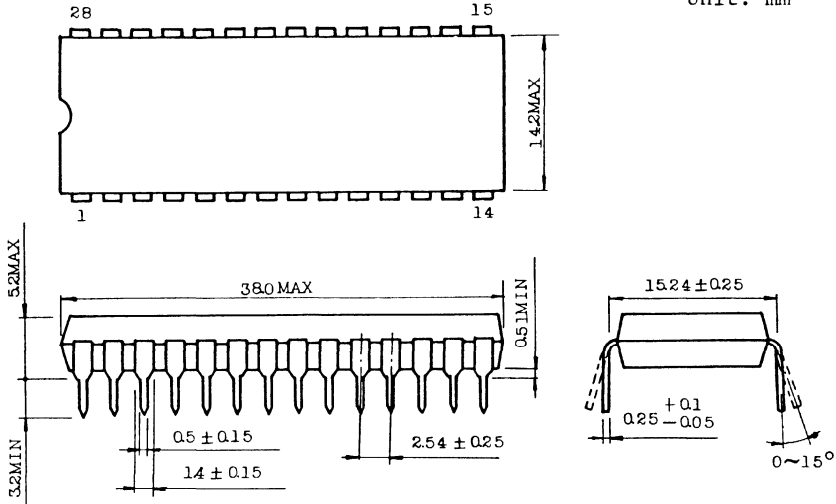
H:  $V_{IH}$ , L:  $V_{IL}$ , \*:  $V_{IH}$  or  $V_{IL}$

# TC531000AP TC531000AF

## OUTLINE DRAWINGS

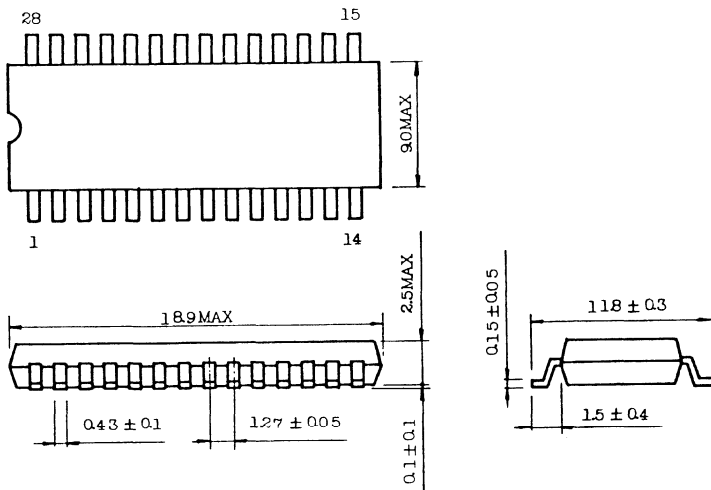
### Plastic DIP

Unit: mm



Note: Each lead pitch is 2.54mm.  
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

### Plastic FP



Note: Each lead pitch is 1.27mm.  
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.



# TOSHIBA MOS MEMORY PRODUCT

2M BIT (256K WORD×8 BIT) CMOS MASK ROM  
SILICON GATE CMOS

# TC532000P

## DESCRIPTION

The TC532000P is a 2,097, 152 bits read only memory organized as 262, 144 words by 8 bits with a low bit cost thus being suitable for use in program memory of microprocessor, especially character generator. The TC532000P using CMOS technology is most suitable for low power applications where

battery operation is required.

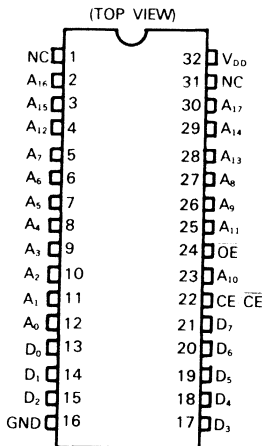
The TC532000P has one programmable chip enable input  $\overline{CE}/\overline{CE}$  for device selection, and one output enable input  $\overline{OE}$  for fast memory access and output control.

The TC532000P is moulded in a 32 pin standard plastic package, 0.6 inch in width.

## FEATURES

- Single 5V Power Supply
- Access Time: 200ns(Max.)
- Power Dissipation
  - Operating Current : 30mA(Max.)
  - Standby Current : 20uA(Max.)
- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- 32pin 600mil width Plastic DIP
- Fully Static Operation
- Programmable Chip Enable

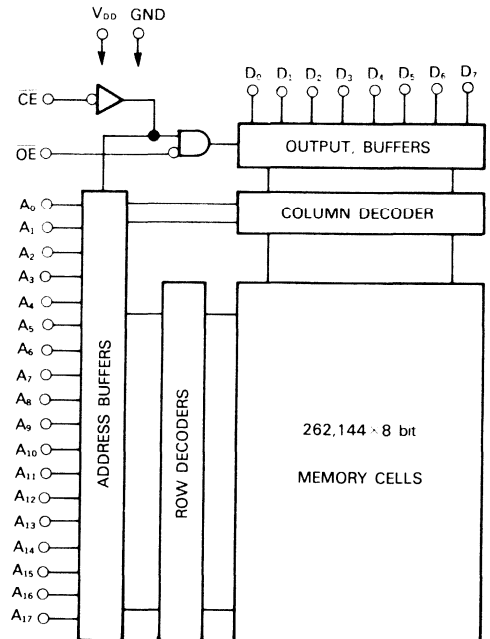
## PIN CONNECTION



## PIN NAMES

A <sub>0</sub> ~A <sub>17</sub>	Address inputs
D <sub>0</sub> ~D <sub>7</sub>	Data outputs
$\overline{OE}$	Output Enable input
$\overline{CE}/\overline{CE}$	Chip enable input
N.C.	No Connection
V <sub>DD</sub>	Power supply
GND	Ground

## BLOCK DIAGRAM



# TC53200P

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.5~7.0	V
V <sub>IN</sub>	Input Voltage	-0.5~V <sub>DD</sub>	V
V <sub>OUT</sub>	Output Voltage	0~V <sub>DD</sub>	V
P <sub>D</sub>	Power Dissipation	1.0	W
T <sub>STG</sub>	Storage Temperature	-55~150	°C
T <sub>ORR</sub>	Operating Temperature	-40~85	°C
T <sub>SOLDER</sub>	Soldering Temperature · Time	260 · 10	°C · sec

Note: \*Plastic FP

## D. C. OPERATING CONDITIONS

(T<sub>a</sub> = -40~85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT.
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	—	0.8	V

## D. C. and OPERATING CHARACTERISTICS

(T<sub>a</sub> = -40~85°C, V<sub>DD</sub> = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0~V <sub>DD</sub>	—	±1.0	μA
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ , V <sub>OUT</sub> = 0V~V <sub>DD</sub>	—	±5.0	μA
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4V	-1.0	—	mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4V	2.0	—	mA
I <sub>DDS1</sub>	Standby Current	$\overline{CE} = V_{IH}$	—	5	mA
I <sub>DDS2</sub>	Standby Current	$\overline{CE} = V_{DD}$ and V <sub>IN</sub> = 0V (V <sub>DD</sub> )	—	20	μA
I <sub>DDO1</sub>	Operating Current	V <sub>IN</sub> = V <sub>IH</sub> /V <sub>IL</sub> , t <sub>cycle</sub> = 200ns, I <sub>OUT</sub> = 0mA	—	40	mA
I <sub>DDO2</sub>		V <sub>IN</sub> = V <sub>DD</sub> /OV, t <sub>cycle</sub> = 200ns, I <sub>OUT</sub> = 0mA	—	30	mA

## CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	f = 1MHz, T <sub>a</sub> = 25°C	—	8	pF
C <sub>OUT</sub>	Output Capacitance	f = 1MHz, T <sub>a</sub> = 25°C	—	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

# TC53200P

## A.C. CHARACTERISTICS

( $T_a = -40 \sim 85^\circ\text{C}$ ,  $V_{DD} = 5V \pm 10\%$ )

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$t_{cyc}$	Cycle Time	200	—	ns
$t_{ACC}$	Access Time	—	200	ns
$t_{CE}$	Chip Enable Access Time	—	200	ns
$t_{OE}$	Output Enable Access Time	—	70	ns
$t_{CED}, t_{OED}$	Output Disable Time	0	60	ns
$t_{OH}$	Output Hold Time	0	—	ns

## AC TEST CONDITIONS

Output Load : 100pF + 1TTL

Input Levels : 0.6V, 2.4V

Timing Measurement Reference Levels

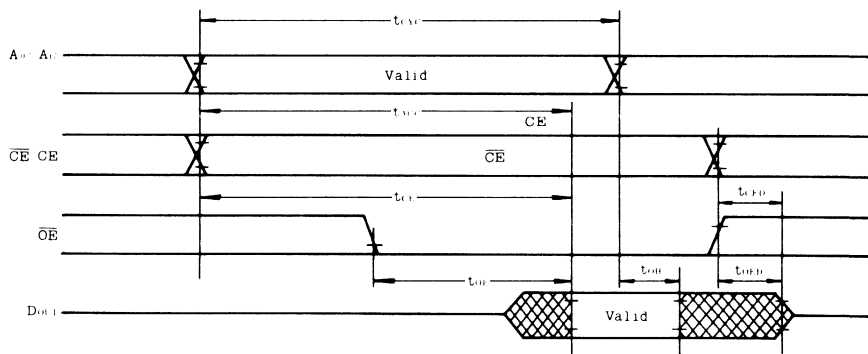
Input : 0.8V, 2.2V

Output : 0.8V, 2.0V

Input Rise and Fall Time

: 5ns

## TIMING WAVEFORMS



## OPERATION MODE

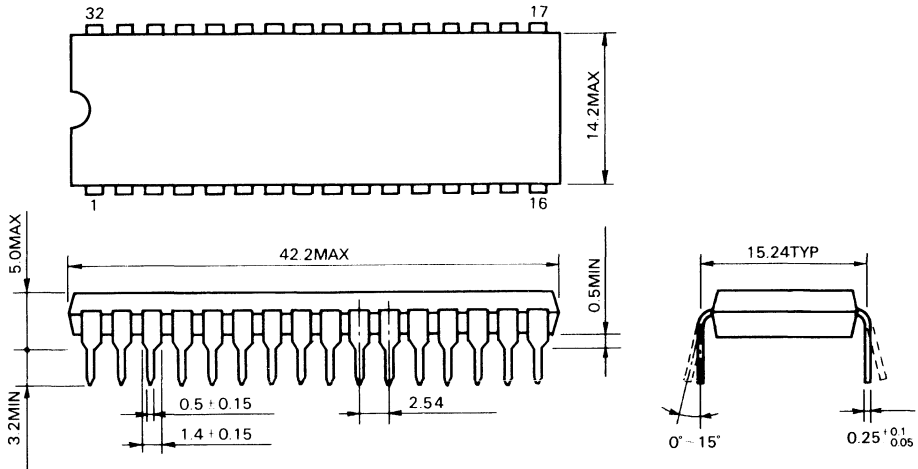
MODE	$\overline{CE}$ (CE)	$\overline{OE}$	$A_0-A_{17}$	Outputs	Power
Read	L(H)	L	Valid	Data out	Operating
Standby	H(L)	*	*	High-Z	Standby
Output Deselect	L(H)	H	*	High-Z	Operating

H:  $V_{IH}$ , L:  $V_{IL}$ , \*:  $V_{IH}$  or  $V_{IL}$

# TC532000P

## OUTLINE DRAWINGS

Unit : mm



Note: Each lead pitch is 2.54mm.

All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.32 leads.

**Note: Toshiba does not assume any responsibility for use of any circuitry described: no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.**  
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# TOSHIBA MOS MEMORY PRODUCT

**4M BIT (512K WORD × 8 BIT) CMOS MASK ROM**  
SILICON GATE CMOS

**TC534000P**

## DESCRIPTION

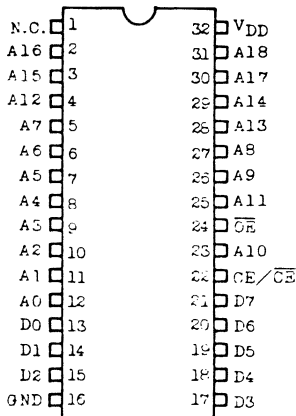
The TC534000P is a 4,194,304 bits read only memory organized as 524,288 words by 8 bits with a low bit cost, thus being suitable for use in program memory of micro-processor, and data memory, especially character generator. The TC534000P using CMOS technology is most suitable for low power applications where battery operations are required.

The TC534000P has one programmable chip enable input  $\overline{CE}/CE$  for device selection. The TC534000P is moulded in a 32 pin standard plastic package, 0.6 inch in width.

## FEATURES

- Single 5V Power Supply
- Access Time: 250ns (Max.)
- Power Dissipation
  - Operating Current: 30mA (Max.)
  - Standby Current : 20 $\mu$ A (Max.)
- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- 32 pin 600 mil width Plastic DIP
- Fully Static Operation
- Programmable Chip Enable

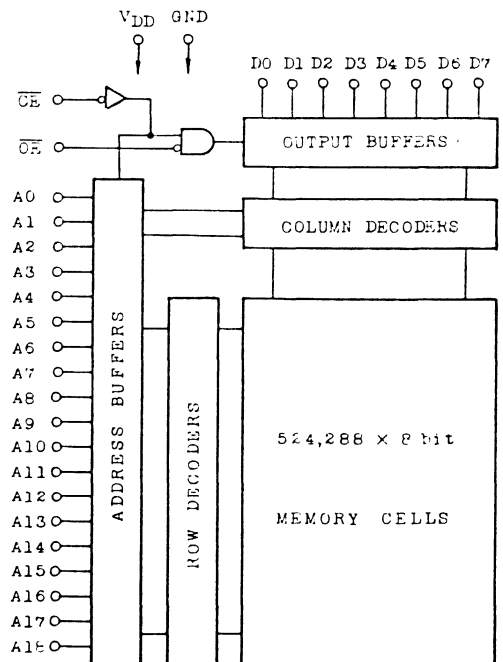
## PIN CONNECTION



## PIN NAMES

A0 ~ A18	Address Inputs
D0 ~ D7	Data Outputs
$\overline{OE}$	Output Enable Input
CE/ $\overline{CE}$	Chip Enable Input
VDD	Power Supply
GND	Ground
N.C.	No Connection

## BLOCK DIAGRAM



# TC53400P

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.5 ~ 7.0	V
V <sub>IN</sub>	Input Voltage	-0.5 ~ V <sub>DD</sub>	V
V <sub>OUT</sub>	Output Voltage	0 ~ V <sub>DD</sub>	V
P <sub>D</sub>	Power Dissipation	1.0	W
T <sub>STG</sub>	Storage Temperature	-55 ~ 150	°C
T <sub>OPR</sub>	Operating Temperature	-40 ~ 85	°C
T <sub>SOLDER</sub>	Soldering Temperature · Time	260 · 10	°C·sec

## D.C. OPERATING CONDITIONS (Ta=-40 ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>DD</sub> +0.3	
V <sub>IL</sub>	Input Low Voltage	-0.3	-	0.8	

## D.C. and OPERATING CHARACTERISTICS (Ta=-40 ~ 85°C, V<sub>DD</sub>=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> =0 ~ V <sub>DD</sub>	-	±1.0	μA
I <sub>LO</sub>	Output Leakage Current	$\overline{CE}=V_{IH}$ , V <sub>OUT</sub> =0V ~ V <sub>DD</sub>	-	±5.0	μA
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> =2.4V	-1.0	-	mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> =0.4V	2.0	-	mA
I <sub>DD</sub> S1	Standby Current	$\overline{CE}=V_{IH}$	-	2	mA
I <sub>DD</sub> S2	Standby Current	$\overline{CE}=V_{DD}$ and V <sub>IN</sub> =0V(V <sub>DD</sub> )	-	20	μA
I <sub>DD</sub> O1	Operating Current	V <sub>IN</sub> =V <sub>IH</sub> /V <sub>IL</sub> , t <sub>cycle</sub> =250ns	-	40	mA
I <sub>DD</sub> O2		V <sub>IN</sub> =V <sub>DD</sub> /0V, t <sub>cycle</sub> =250ns	-	30	

## CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	f=1MHz, Ta=25°C	-	8	pF
C <sub>OUT</sub>	Output Capacitance	f=1MHz, Ta=25°C	-	10	

Note: This parameter is periodically sampled and is not 100% tested.

# TC534000P

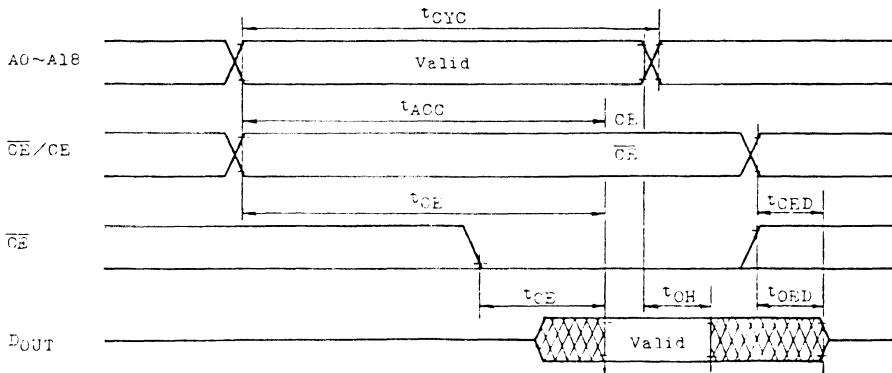
## A.C. CHARACTERISTICS (Ta=-40 ~ 85°C, V<sub>DD</sub>=5V±10%)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t <sub>CYC</sub>	Cycle Time	250	-	ns
t <sub>ACC</sub>	Access Time	-	250	
t <sub>CE</sub>	Chip Enable Access Time	-	250	
t <sub>OE</sub>	Output Enable Access Time	-	100	
t <sub>CED</sub>	Output Disable Time	0	80	
t <sub>OED</sub>	Output Disable Time from $\overline{OE}$	-	80	
t <sub>OH</sub>	Output Hold Time	20	-	

## AC TEST CONDITIONS

Output Load : 100pF + 1TTL  
 Input Levels : 0.6V, 2.4V  
 Timing Measurement Reference Levels Input : 0.8V, 2.2V  
 Output: 0.8V, 2.0V  
 Input Rise and Fall Time : 5ns

## TIMING WAVEFORMS



## OPERATION MODE

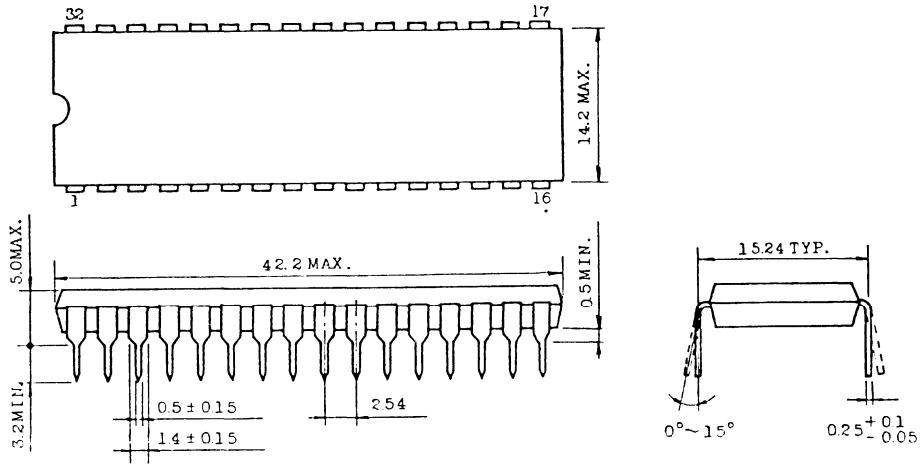
MODE	$\overline{CE}$ (CE)	$\overline{OE}$	A0 ~ 18	Outputs	Power
Read	L(H)	L	Valid	Data Out	Operating
Standby	H(L)	*	*	High-Z	Standby
Output Deselect	L(H)	H	*	High-Z	Operating

H: V<sub>IH</sub>, L: V<sub>IL</sub>, \*: V<sub>IH</sub> or V<sub>IL</sub>

# TC53400P

## OUTLINE DRAWINGS

Unit: mm



Note: Each lead pitch is 2.54mm.

All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.32 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.



# MEMO

A series of horizontal dotted lines for writing.

# MEMO

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# MEMO

A series of horizontal dotted lines for writing.

# MEMO

A series of horizontal dotted lines for writing.